National Semiconductor®

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National Discrete DMOS Power MOSFET Products Databook

Discrete POWER and Signal Technologies

National Discrete
DMOS Power MOSFET Products Databook

Introduction to the National Semiconductor DMOS Power MOSFET Databook

National Semiconductor supplies surface mount and through-hole power MOSFETs ideal for the wide ranging computer, automotive, industrial, and consumer electronics market places. Exciting advances have occurred in Discrete POWER & Signal Technologies resulting in National Semiconductor being recognized as one of the leaders in high performance surface mount Power MOSFETs. Aggressive focus on low on-resistance and reduced package height and size has resulted in continuous new product releases.

Our expertise in advanced package and silicon technology has enabled introduction of products with increased output current for a given power dissipation. Product development emphasizes increased power handling, maximized thermal conductance by reducing package resistance, reduction of Rds (on), and increased cell density, thereby reducing package size, allowing for smaller footprints. National Semiconductor's Power MOSFETs are fabricated utilizing vertical DMOS process technology resulting in increased cell density and decreased Rds (on). Package redesign has focused on reducing thermal resistance and increasing current handling. Surface mount high performance Power MOSFETs are ideal for Low Voltage/Low Power Portable Equipment, Personal Systems, Cellular Phone, Automotive and Consumer Electronics applications.

This volume contains electrical and mechanical specifications of N-Channel, P-Channel and Complementary DMOS based power and small signal products in a wide range of surface mount and leaded package options.

National Semiconductor Power MOSFETs products included in this databook:

- N-Channel, P-Channel and Complementary SuperSOT™ -3, -6, -8
- Complementary SO-16
- N-Channel and P-Channel Power SOT (SOT-223)
- N-Channel, P-Channel and Complementary SO-8
- N-Channel and P-Channel SOT-23
- N-Channel TO-220 / TO-263
- N-Channel and P-Channel TO-92

The selection guide in this databook is designed to provide an easy reference to the many standard parts offered by National Semiconductor. The Diode, Bipolar Transistor and JFET Products Databook contains electrical and mechanical specifications for a broad range of diode, bipolar transistor, and JFET products in a vast array of leaded and surface mount package options, and includes datasheets applicable to the preferred part types within the categories. If you have any further questions, please contact the National Semiconductor Customer Support Center in your area, your local sales office, or the factory for other options or special selections available.

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National Semiconductor™

Discrete POWER & Signal Technologies

DISCRETE SEMICONDUCTOR PRODUCTS

DMOS Power MOSFET DATABOOK

July 1996 Edition

DMOS Discrete Product Line
Alphanumeric List of Available Parts

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Note 1: Data sheet is available upon request.

* Preliminary information; samples available; full production release pending reliability completion.

** Advanced information; please contact Discrete POWER & Signal Technologies Marketing for updated information.

Alphanumeric List of Available Parts (continued)

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Note 1: Data sheet is available upon request.

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** Advanced information; please contact Discrete POWER & Signal Technologies Marketing for updated information.

Quality and Reliability Statement

National Semiconductor is dedicated to bringing the highest level of quality and reliability to its customers on a continuing basis. The discrete operation has been supplying, and will continue to supply, discrete components with quality second to none in the most demanding applications, including those requiring guaranteed parametric limits at temperatures other than 25°C.

Most discrete products from National Semiconductor are available in two forms:

1) Industrial/Commercial identified by a standard part number having various commonly-known prefixes and tested to a published National Semiconductor, JEDEC, Proelection or other specification.

2) Customer-specific identified by an assigned "stamp-off" number, and tested and marked as determined by the customer for their specific requirements. This may range from a custom-marked industrial/commercial part to product meeting various additional/special electrical needs specified at -40°C and +125°C.

Device lots are subjected to 100% processing at final test to the datasheet or other applicable electrical specifications refelected on internal documentation. All products are then transferred to QA where they are subjected to sample electrical testing, usually to the same electrical specifications, and additional mechanical inspection requirements.

Discrete Power & Signal Techologies utilizes two programs to insure reliability performance of various products delivered to our customers. They are the **1) Reliability Qualification Program** for new product and product manufacturing variations/locations, and the **2) Reliability Audit Program** applicable to existing qualified products, with the goal of continuous improvement. Addtional information regarding these programs can be found in Section 10 of this databook.

Section 1

Selection Guide

National Semiconductor™

National Power MOSFET Selection Guide

SuperSOT™-3 (SOT-23)

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)			I_D (A)	P_D (W)	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V	V_{GS} @ 2.7V				
N-Channel							
20		0.11	0.14	1.7	0.5	NDS335N	3-14
		0.16	0.21	1.3	0.5	NDS331N	3-2
30	0.085	0.125		1.6	0.5	NDS355N	3-44
	0.16	0.25		1.1	0.5	NDS351N	3-26
P-Channel							
-20		0.2	0.27	-1.2	0.5	NDS336P	3-20
		0.3	0.41	-1	0.5	NDS332P	3-8
	0.21	0.3		-1.1	0.5	NDS356P	3-56
	0.35	0.5		-0.85	0.5	NDS352P	3-38
-30	0.2	0.3		-11	0.5	NDS356AP	3-50
	0.3	0.5		-0.9	0.5	NDS352AP	3-32

SuperSOT™-6

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)			I_D (A)	P_D (W)	Config	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V	V_{GS} @ 2.7V					
N-Channel								
20		0.06	0.075	4.1	1.6	Single	NDC631N	3-62
30	0.06	0.09		3.2	1.6	Single	NDC651N	3-74
50	2			0.51	0.7	Dual	NDC7002N	3-95
P-Channel								
-20		0.14	0.2	-2.7	1.6	Single	NDC632P	3-68
-30	0.11	0.18		-2.4	1.6	Single	NDC652P	3-80
-50	5			-0.34	0.7	Dual	NDC7003P	3-101
Complementary N-P Channel								
50	2			0.51	0.7	N-Ch	NDC7001C	3-86
-50	5			-0.34	0.7	P-Ch		

* Preliminary information; samples available; full production release pending reliability completion.
** Advance information; please contact Discrete POWER & Signal Technologies Marketing for updated information.
Package Scale 1 : 1 on letter size paper

SuperSOT™-8

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)			I_D (A)	P_D (W)	Config	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V	V_{GS} @ 2.7V					
N-Channel								
20		0.03	0.04	5.8	1.8	Single	NDH831N	3-107
		0.06	0.075	3	0.9	Dual	NDH8301N**	3-119
30	0.03	0.045		5.8	1.8	Single	NDH8436	3-123
P-Channel								
-20		0.06	0.08	-4.2	1.8	Single	NDH832P	3-113
		0.13	0.19	-2	0.9	Dual	NDH8302P**	3-121
-30	0.053	0.095		-4.4	1.8	Single	NDH8447	3-129
	0.11	0.18		-2.3	0.9	Dual	NDH8502P**	3-135

* Preliminary information; samples available; full production release pending reliability completion.
** Advance information; please contact Discrete POWER & Signal Technologies Marketing for updated information.
Package Scale 1 : 1 on letter size paper

SO-8 

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)			I_D (A)	P_D (W)	Config	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V	V_{GS} @ 2.7V					
N Channel								
20		0.015	0.02	9.9	2.5	Single	NDS8426	4-10
		0.025	0.03	7.4	2.5	Single	NDS8425**	4-8
		0.035	0.045	5.5	2	Dual	NDS8926	4-58
		0.06	0.075	4.5	2	Dual	NDS9925A**	4-136
30	0.015	0.02		10	2.5	Single	NDS8410	4-2
	0.028	0.042		7.3	2.5	Single	NDS9410A	4-118
	0.035	0.05		5.3	2	Dual	NDS8936	4-79
	0.05	0.08		5	2	Dual	NDS9936	4-146
	0.08	0.11		3.7	2	Dual	NDS9956A	4-207
50	0.13	0.2		3	2	Dual	NDS9955	4-201
	0.3	0.5		2	2	Dual	NDS9959	4-227
60	0.1	0.2		3.5	2	Dual	NDS9945	4-168
	0.16	0.25		2.6	2	Dual	NDS9957	4-213
P Channel								
-20		0.035	0.05	-6.5	2.5	Single	NDS8434	4-22
		0.055	0.075	-5.2	2.5	Single	NDS8433	4-16
		0.07	0.1	-3.8	2	Dual	NDS8934	4-73
		0.11	0.19	-3.2	2	Dual	NDS9933	4-138
		0.13	0.19	-3.1	2	Dual	NDS9933A**	4-144
	0.06	0.115		-5.3	2.5	Single	NDS9430	4-124
	0.1	0.16		-4.3	2.5	Single	NDS9405	4-106
	0.1	0.19		-3.5	2	Dual	NDS9947	4-174
-30	0.028	0.045		-7	2.5	Single	NDS8435	4-28
	0.05	0.09		-5.3	2.5	Single	NDS9435A	4-130
	0.065	0.1		-4	2	Dual	NDS8947	4-85
	0.13	0.2		-3.4	2.5	Single	NDS9400A	4-100
	0.13	0.2		-2.9	2	Dual	NDS9953A	4-195
-60	0.15	0.24		-3.3	2.5	Single	NDS9407	4-112
	0.25	0.5		-2.3	2	Dual	NDS9948	4-180

* Preliminary information; samples available; full production release pending reliability completion.
** Advance information; please contact Discrete POWER & Signal Technologies Marketing for updated information.
Package Scale 1 : 1 on letter size paper

SO-8 Continued

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)			I_D (A)	P_D (W)	Config	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V	V_{GS} @ 2.7V					
Complementary N-P Channel								
20		0.035	0.045	5.5	2	N-Ch	NDS8928	4-64
-20		0.07	0.1	-3.8	2	P-Ch		
20	0.1	0.15		3.5	2	N-Ch	NDS9958	4-219
-20	0.1	0.19		-3.5	2	P-Ch		
20	0.125	0.25		3	2	N-Ch	NDS9943	4-160
-20	0.16	0.3		-2.8	2	P-Ch		
20	0.125	0.25		3	2	N-Ch	NDS9942	4-152
-20	0.2	0.4		-2.5	2	P-Ch		
30	0.035	0.05		5.3	2	N-Ch	NDS8958	4-91
-30	0.065	0.1		-4	2	P-Ch		
30	0.08	0.11		3.7	2	N-Ch	NDS9952A	4-186
-30	0.13	0.2		-2.9	2	P-Ch		
Complementary MOSFET Half Bridge								
30	0.035	0.05		6.3	2.5	N-Ch	NDS8858H	4-50
-30	0.065	0.1		-4.8		P-Ch		
30	0.045	0.075		5.7	2.5	N-Ch	NDS8839H	4-34
-30	0.09	0.15		-4		P-Ch		
30	0.08	0.11		4.3	2.5	N-Ch	NDS8852H	4-42
-30	0.13	0.2		-3.4		P-Ch		

* Preliminary information; samples available; full production release pending reliability completion.
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Package Scale 1 : 1 on letter size paper

Power SOT (SOT-223) 

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V				
N-Channel						
30	0.015	0.02	11.5	3	NDT455N	5-56
	0.028	0.042	8	3	NDT453N	5-44
	0.035	0.05	7.2	3	NDT451AN	5-20
	0.05	0.08	5.5	3	NDT451N	5-26
60	0.1		4	3	NDT3055	5-74
		0.12	3.7	3	NDT3055L	5-80
	0.16	0.2	2.6	3	NDT014L *	5-8
	0.2		2.7	3	NDT014	5-2
100		0.25 @5V	2.1	3	NDT410EL	5-14
P-Channel						
-30	0.03	0.045	-7.5	3	NDT456P	5-62
	0.05	0.09	-5.9	3	NDT454P	5-50
	0.075	0.11	-5	3	NDT452AP	5-32
	0.18	0.32	-3	3	NDT452P	5-38
-60	0.3	0.5	-2.5	3	NDT2955	5-68

SOIC-16 

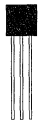
V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)	Config	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V					
3 Phase Brushless Motor Driver							
30	0.08	0.12	±3.4	3	N-Ch	NDM3000	6-2
-30	0.16	0.25			P-Ch		

* Preliminary information; samples available; full production release pending reliability completion.
** Advance information; please contact Discrete POWER & Signal Technologies Marketing for updated information.
Package Scale 1 : 1 on letter size paper

SOT-23

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V				
N-Channel						
50	3.5	6	0.22	0.36	BSS138	7-28
60	2	3 @ 5V	0.28	0.3	NDS7002A	7-2
	5		0.5	0.3	MMBF170	7-8
	7.5		0.115	0.2	2N7002	7-2
100	6	10	0.17	0.36	BSS123	7-23
P-Channel						
-50	10		-0.13	0.3	BSS84	7-18
-60	5	7.5	-0.18	0.36	NDS0605	7-38
	10	20	-0.12	0.36	NDS0610	7-33

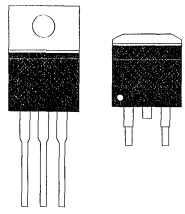
TO-92



V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 4.5V				
N-Channel						
60	2	3	0.4	0.625	BS270	7-13
	5	5.3	0.2	0.4	2N7000	7-2
	5		0.5	0.83	BS170	7-8
100	6	10	0.22	0.63	BSS100	7-23
P-Channel						
-50	10		-0.17	0.8	BSS110	7-18
-60	10	20	-0.18	0.8	NDF0610	7-33

* Preliminary information; samples available; full production release pending reliability completion.
** Advance information; please contact Discrete POWER & Signal Technologies Marketing for updated information.
Package Scale 1 : 1 on letter size paper

TO-220 / TO-263AB



NDP Series NDB Series

V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	P_D (W)	Part Number	Page
	V_{GS} @ 10V	V_{GS} @ 5V				
N-Channel						
30	0.022	0.04 @ 4.5V	25	50	NDP603AL	8-14
	0.0135	0.02 @ 4.5V	52	75	NDP6030L	8-43
50	0.01		75	150	NDP7052**	8-87
	0.016		64	130	NDP7051	8-79
	0.022		48	100	NDP6051	8-61
	0.025		48	100	NDP6050	8-49
	0.1		15	50	NDP4050	8-19
	0 .0075	0.01	75	150	NDP7052L**	8-89
	0.01	0.014	68	130	NDP7051L**	8-85
	0.02	0.025	48	100	NDP6050L	8-55
	0.08	0.1	15	50	NDP4050L	8-25
60	0.013		75	150	NDP7060	8-91
	0.016		64	130	NDP7061	8-103
	0.025		48	100	NDP6060	8-67
	0.05		26	60	NDP506A	8-2
	0.1		15	50	NDP4060	8-31
	0.01	0.013	75	150	NDP7060L	8-97
	0.013	0.018	60	130	NDP7061L	8-109
	0.02	0.025	48	100	NDP6060L	8-73
	0.035	0.05	26	60	NDP506AL	8-8
	0.08	0.1	15	50	NDP4060L	8-37
80	0.022		60	150	NDP708A	Note 1
	0.042		36	100	NDP608A	Note 1
	0.08		19	75	NDP508A	Note 1
	0.16		12	50	NDP408A	Note 1
100	0.038		42	150	NDP710A	Note 1
	0.065		26	100	NDP610A	Note 1
	0.12		15	75	NDP510A	Note 1
	0.25		9	50	NDP410A	Note 1

Note 1: Data sheet is available upon request.
Avalanche rating part is also available, Please consult Marketing for details.
NDB Series for TO-263AB packages.
* Preliminary information; samples available; full production release pending reliability completion.
** Advance information; please contact Discrete POWER & Signal Technologies Marketing for updated information.
Package Scale 1 : 1 on letter size paper

Upgrades for New Designs

SuperSOT™-3

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	Configuration
		V_{GS} @ 10V	V_{GS} @ 4.5V		
NDS352P	-20	0.35	0.5	-0.85	P-Channel
Upgrade **NDS352AP**	**-30**	**0.3**	**0.5**	**-0.9**	**P-Channel**
NDS356P	-20	0.21	0.3	-1.1	P-Channel
Upgrade **NDS356AP**	**-30**	**0.2**	**0.3**	**-1.1**	**P-Channel**

SO-8

Part Number	V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	Configuration
		V_{GS} @ 10V	V_{GS} @ 4.5V		
NDS9400	-20	0.25	0.4	-2.5	Single P-Channel
Upgrade **NDS9400A**	**-30**	**0.13**	**0.2**	**-3.4**	**Single P-Channel**
NDS9410	30	0.03	0.05	7.2	Single N-Channel
Upgrade **NDS9410A**	**30**	**0.028**	**0.042**	**7.3**	**Single N-Channel**
NDS9405	-20	0.1	0.16	-4.3	Single P-Channel
NDS9430	-20	0.06	0.115	-5.3	Single P-Channel
NDS9435	-30	0.07	0.13	-4.6	Single P-Channel
Upgrade **NDS9435A**	**-30**	**0.05**	**0.09**	**-5.3**	**Single P-Channel**
NDS9936	30	0.05	0.08	5	Dual N-Channel
Upgrade **NDS8936**	**30**	**0.035**	**0.05**	**5.3**	**Dual N-Channel**
NDS9947	-20	0.1	0.19	-3.5	Dual P-Channel
Upgrade **NDS8947**	**-30**	**0.065**	**0.1**	**-4**	**Dual P-Channel**
NDS9942	20 / -20	0.125 / 0.2	0.25 / 0.4	3 / -2.5	Dual N / P-Channel
NDS9943	20 / -20	0.125 / 0.16	0.25 / 0.3	3 / -2.8	Dual N / P-Channel
NDS9952	25 / -25	0.1 / 0.25	0.15 / 0.4	3 / -2.3	Dual N / P-Channel
Upgrade **NDS9952A**	**30 / -30**	**0.08 / 0.13**	**0.11 / 0.20**	**3.7 / -2.9**	**Dual N / P-Channel**

SO-8 Continued

Part Number		V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	Configuration
			V_{GS} @ 10V	V_{GS} @ 4.5V		
	NDS9953	-20	0.25	0.4	-2.3	Dual P-Channel
Upgrade	**NDS9953A**	**-30**	**0.13**	**0.2**	**-2.9**	**Dual P-Channel**
	NDS9956	20	0.1	0.2	2	Dual N-Channel
Upgrade	**NDS9956A**	**30**	**0.08**	**0.11**	**3.7**	**Dual N-Channel**
	NDS9958	20 / -20	0.1 / 0.1	0.15 / 0.19	3.5 / -3.5	Dual N / P-Channel
Upgrade	**NDS8958**	**30 / -30**	**0.035 / 0.065**	**0.05 / 0.10**	**5.3 / -4**	**Dual N / P-Channel**

Power SOT (SOT-223)

Part Number		V_{DS} (V)	$R_{DS(ON)}$ Max (Ω)		I_D (A)	Configuration
			V_{GS} @ 10V	V_{GS} @ 4.5V		
	NDT451N	30	0.05	0.08	5.5	N-Channel
Upgrade	**NDT451AN**	**30**	**0.035**	**0.05**	**7.2**	**N-Channel**
	NDT452P	-30	0.18	0.32	-3	N-Channel
Upgrade	**NDT452AP**	**-30**	**0.075**	**0.11**	**-5**	**N-Channel**

Section 2

Cross Reference Guide

DMOS Cross Reference

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2N7008	2N7000	TO-92	7-2
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BSS100	BSS100	TO-92	7-23
BSS110	BSS110	TO-92	7-18
BSS123	BSS123	SOT-23	7-23
BSS138	BSS138	SOT-23	7-28
BSS84	BSS84	SOT-23	7-18
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BUK452-60A	NDP4060	TO-220	8-31
BUK452-60B	NDP4060	TO-220	8-31
BUK453-50A	NDP506A	TO-220	8-2
BUK453-50B	NDP4060	TO-220	8-31
BUK453-60A	NDP506A	TO-220	8-2
BUK453-60B	NDP4060	TO-220	8-31
BUK455-50A	NDP6060	TO-220	8-67
BUK455-50A	NDP506A	TO-220	8-2
BUK456-50A	NDP6060	TO-220	8-67
BUK456-50B	NDP6060	TO-220	8-67
BUK456-60A	NDP6060	TO-220	8-67
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BUK552-50A	NDP4060L	TO-220	8-37
BUK552-50B	NDP4060L	TO-220	8-37
BUK552-60A	NDP4060L	TO-220	8-37
BUK552-60B	NDP4060L	TO-220	8-37
BUK553-50A	NDP506AL	TO-220	8-8
BUK553-50B	NDP4060L	TO-220	8-37
BUK553-60A	NDP506AL	TO-220	8-8
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HAT1025R	NDS9933	SO-8	4-138
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HAT1008F	NDS9400A	SO-8	4-100
HAT1001F	NDS8934	SO-8	4-73
HAT1020R	NDS8947	SO-8	4-85
HAT1023R	NDS8434	SO-8	4-22
HAT1024R	NDS9953A	SO-8	4-195
HAT2002F	NDS8936	SO-8	4-79
HAT2004F	NDS8926	SO-8	4-58
HAT2005F	NDS8926	SO-8	4-58
HAT2007F	NSD9936	SO-8	4-146
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IRF7306	NDS8947	SO-8	4-85
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** Advanced information; Please contact Discrete POWER & Signal Technologies Marketing for updated information.

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Si6447	NDH8447	SuperSOT™-8	3-129
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Si9405	NDS9405	SO-8	4-106
Si9407	NDS9407	SO-8	4-112
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Si9410	NDS9410A	SO-8	4-118
Si9430	NDS9430	SO-8	4-124
Si9434	NDS8434	SO-8	4-22
Si9435	NDH8447	SuperSOT™-8	3-129
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Si9928	NDS8928	SO-8	4-64
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Si9936	NDS9936	SO-8	4-146
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SSD2002	NDS9952A	SO-8	4-186
SSD2003	NDS9956A	SO-8	4-207
SSD2005	NDS9953A	SO-8	4-195
SSD2007	NDS9958	SO-8	4-219
SSD2009	NDS9955	SO-8	4-201
SSD2101	NDS9410A	SO-8	4-118
SSD2101	NDS9410A	SO-8	4-118
SSD2102	NDS9430	SO-8	4-124
VN0610LL	2N7000	TO-92	7-2
VN10KE	BS170	TO-92	7-8
VN10KM	BS170	TO-92	7-8
VN2222L	BS170	TO-92	7-8
XN0610L	BS170	TO-92	7-8
ZVN3302A	BS170	TO-92	7-8
ZVN3304A	BS170	TO-92	7-8
ZVN3308	BS170	TO-92	7-8
NDS352P	NDS 352AP	SuperSOT™-3	3-38
NDS356P	NDS356AP	SuperSOT™-3	3-56

80V, 100V, and avalanche rated TO-220/TO-263AB DMOS products are available. Please consult Discrete POWER & Signal Technologies Marketing for details.

Section 3

SuperSOT™ -3 / -6 / -8 Data Sheets

National Semiconductor™

July 1996

NDS331N

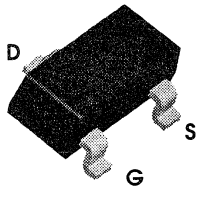
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

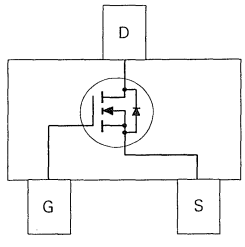
These N-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.3 A, 20 V. $R_{DS(ON)}$ = 0.21 Ω @ V_{GS}=2.7 V
  $R_{DS(ON)}$ = 0.16 Ω @ V_{GS}=4.5 V.
- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	NDS331N	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage - Continuous	8	V
I_D	Maximum Drain Current - Continuous (Note 1a)	1.3	A
	- Pulsed	10	
P_D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J =125°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.5	0.7	1	V
		T_J =125°C	0.3	0.53	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 2.7 V, I_D = 1.3A		0.15	0.21	Ω
		T_J =125°C		0.24	0.4	
		V_{GS} = 4.5 V, I_D = 1.5 A		0.11	0.16	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 2.7 V, V_{DS} = 5 V	3			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	4			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.3 A,		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz		162		pF
C_{oss}	Output Capacitance			85		pF
C_{rss}	Reverse Transfer Capacitance			28		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GS} = 5 V, R_{Gen} = 6Ω		5	20	ns
t_r	Turn - On Rise Time			25	40	ns
$t_{d(off)}$	Turn - Off Delay Time			10	20	ns
t_f	Turn - Off Fall Time			5	20	ns
Q_g	Total Gate Charge	V_{DS} = 5 V, I_D = 1.3 A, V_{GS} = 4.5 V		3.5	5	nC
Q_{gs}	Gate-Source Charge			0.3		nC
Q_{gd}	Gate-Drain Charge			1		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S =0.42A (Note 2)		0.8	1.2	V

Notes:

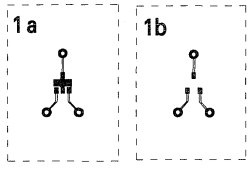
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

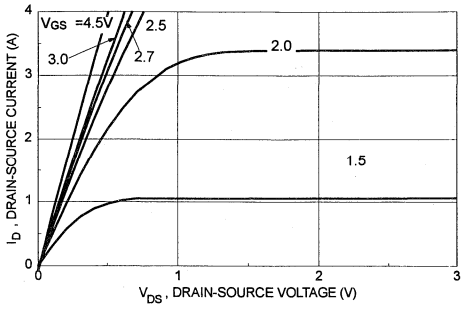


Figure 1. On-Region Characteristics

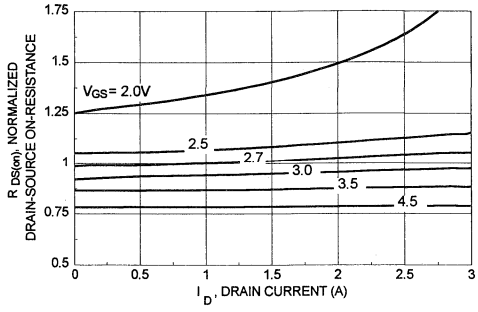


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

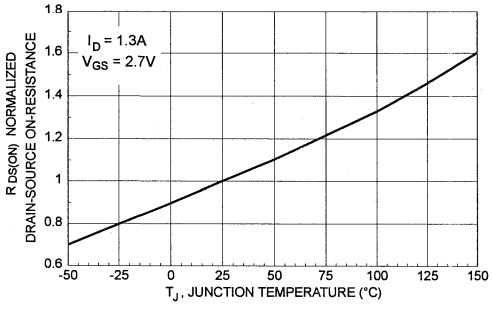


Figure 3. On-Resistance Variation with Temperature

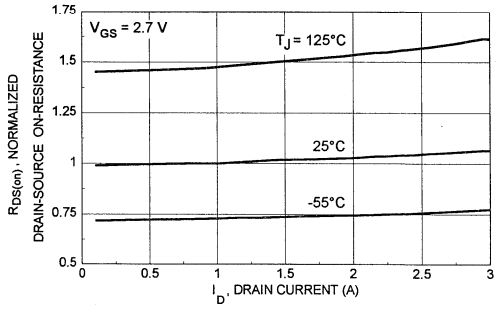


Figure 4. On-Resistance Variation with Drain Current and Temperature

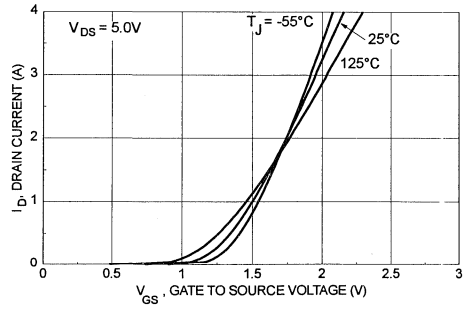


Figure 5. Transfer Characteristics

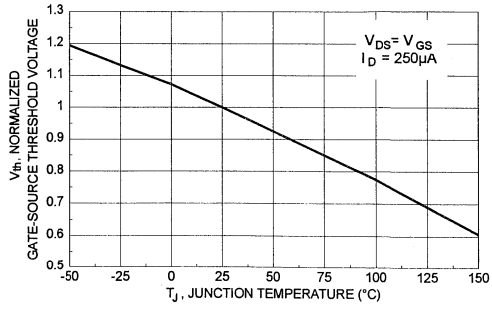


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

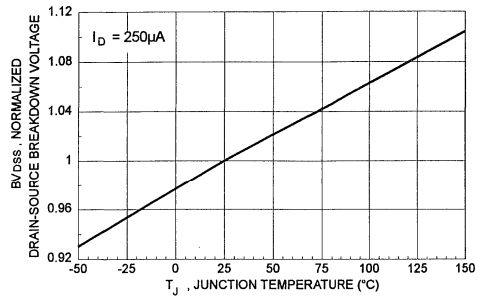


Figure 7. Breakdown Voltage Variation with Temperature

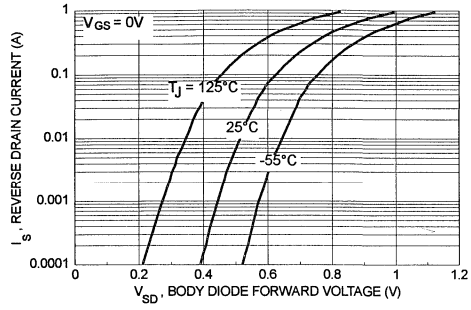


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

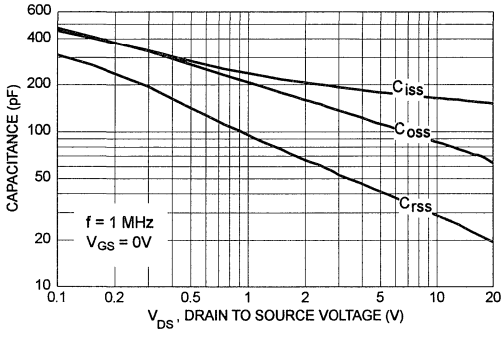


Figure 9. Capacitance Characteristics

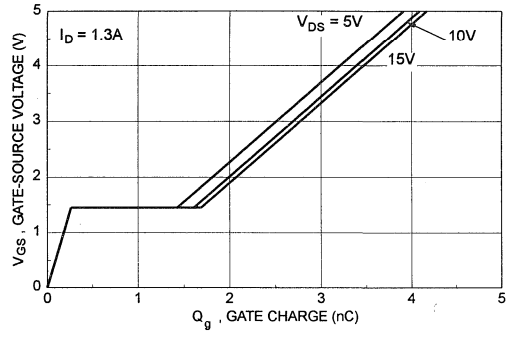


Figure 10. Gate Charge Characteristics

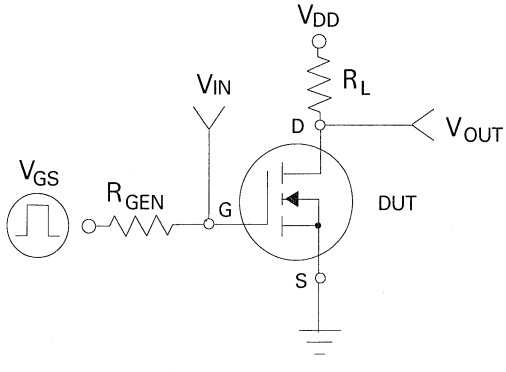


Figure 11. Switching Test Circuit

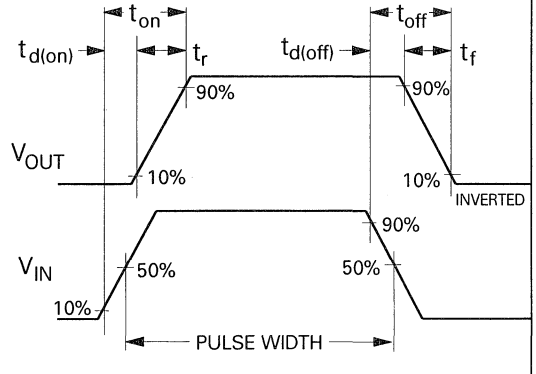


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

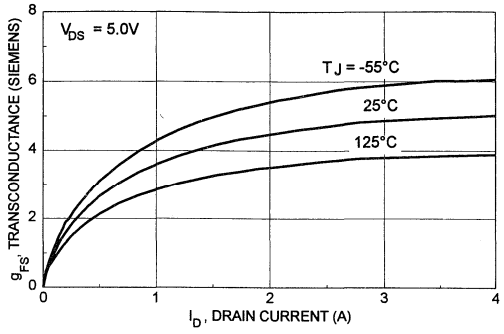


Figure 13. Transconductance Variation with Drain Current and Temperature

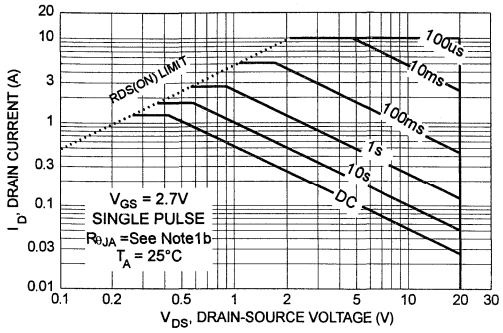
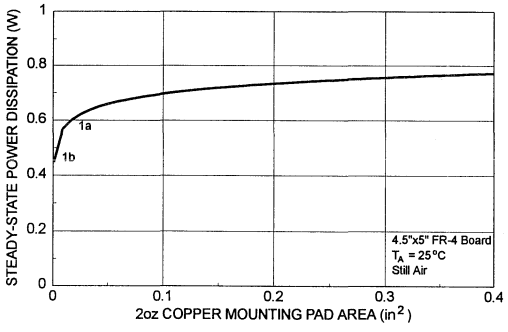


Figure 14. Maximum Safe Operating Area



Figue 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

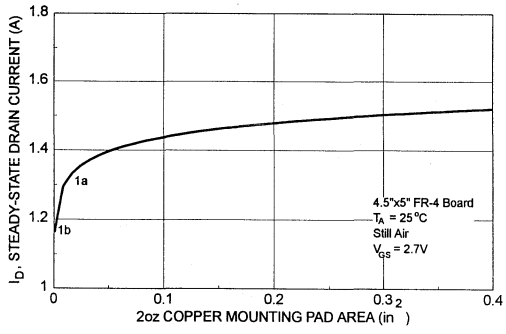


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

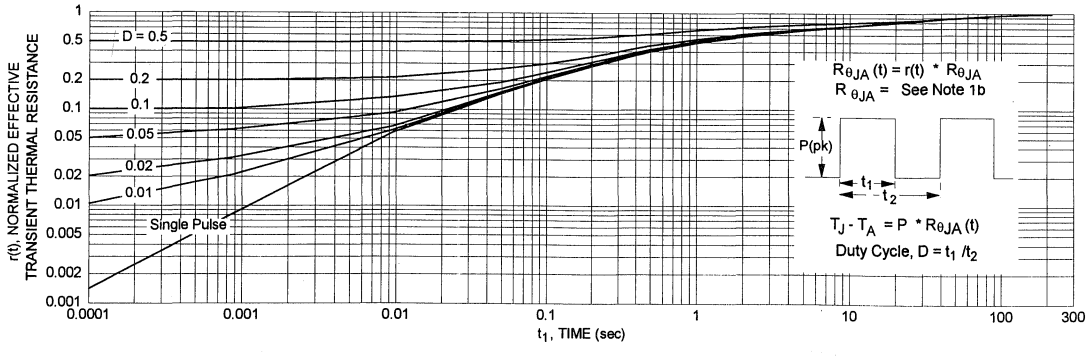


Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996
PRELIMINARY

NDS332P

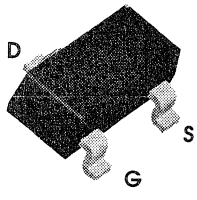
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

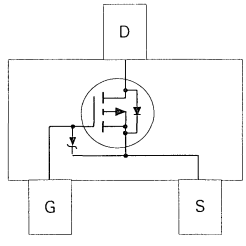
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -1 A, -20 V, $R_{DS(ON)}$ = 0.41Ω @ V_{GS}= -2.7 V
  $R_{DS(ON)}$ = 0.3 Ω @ V_{GS} = -4.5 V.
- Very low level gate drive requirements allowing direct operation in 3V circuits. $V_{GS(th)}$ < 1.0V.
- Gate-Source Zener for ESD ruggedness.
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface Mount package.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS332P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		-8	V
I_D	Drain Current - Continuous	(Note 1a)	-1	A
	- Pulsed		-10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100pf / 1500 Ohm)		2.5	kV
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.5	-0.6	-1	V
		T_J =125°C	-0.3	-0.45	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -2.7 V, I_D = -1 A		0.35	0.41	Ω
		T_J =125°C		0.5	0.74	
		V_{GS} = -4.5 V, I_D = -1 A		0.26	0.3	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -2.7 V, V_{DS} = -5 V	-1.5			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-2.5			
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1 A		2		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		195		pF
C_{oss}	Output Capacitance			105		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = -6 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		8	15	ns
t_r	Turn - On Rise Time			30	45	ns
$t_{d(off)}$	Turn - Off Delay Time			25	45	ns
t_f	Turn - Off Fall Time			27	45	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -1 A, V_{GS} = -4.5 V		3.7	5	nC
Q_{gs}	Gate-Source Charge			0.5		nC
Q_{gd}	Gate-Drain Charge			0.8		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 A (Note 2)		-0.75	-1.2	V

Notes:

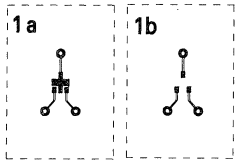
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

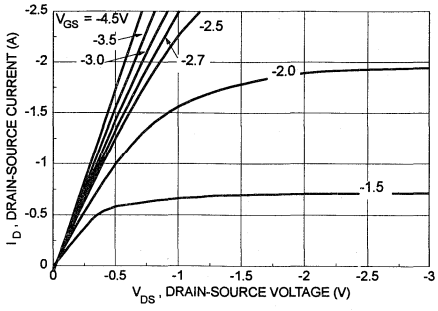


Figure 1. On-Region Characteristics

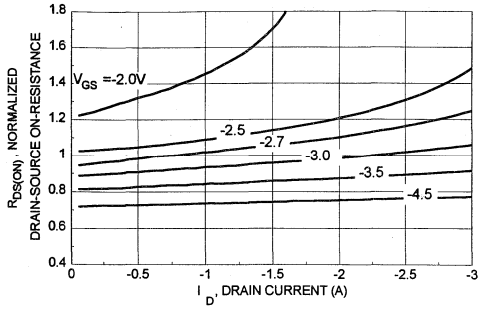


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

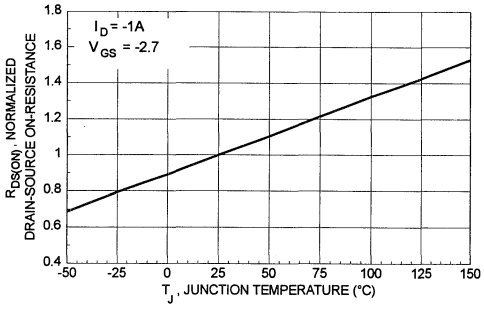


Figure 3. On-Resistance Variation with Temperature

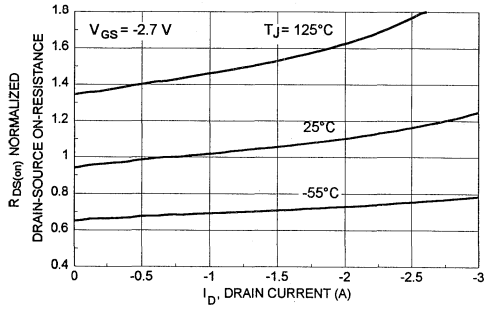


Figure 4. On-Resistance Variation with Drain Current and Temperature

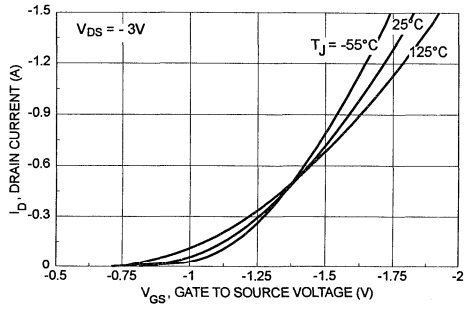


Figure 5. Transfer Characteristics

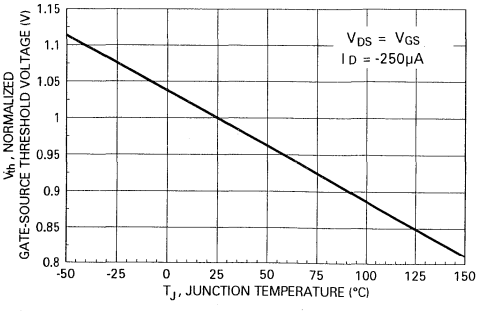


Figure 6. Gate Threshold Variation with Temperature

3

Typical Electrical Characteristics (continued)

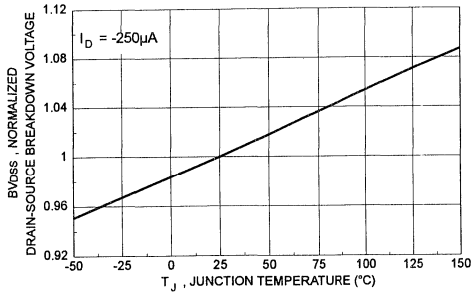


Figure 7. Breakdown Voltage Variation with Temperature

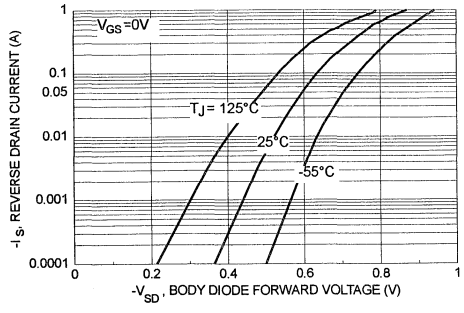


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

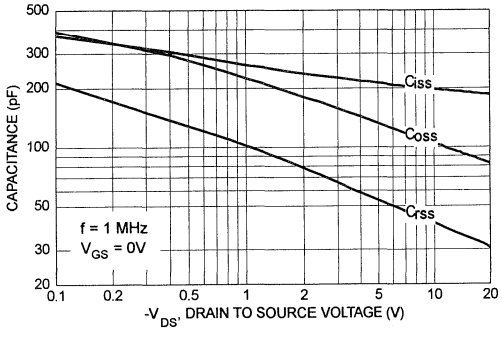


Figure 9. Capacitance Characteristics

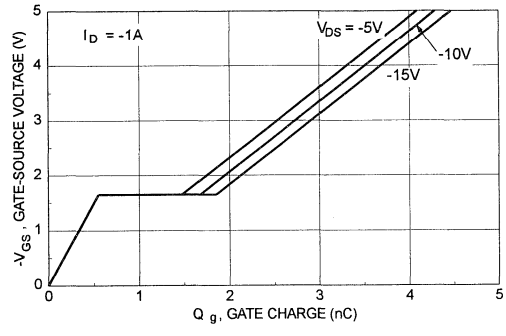


Figure 10. Gate Charge Characteristics

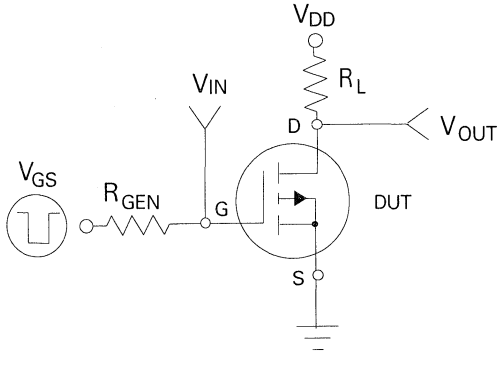


Figure 11. Switching Test Circuit

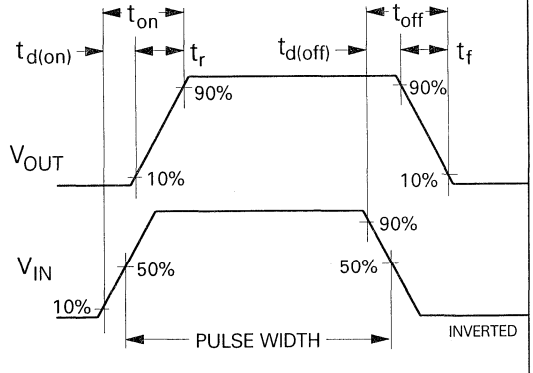


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

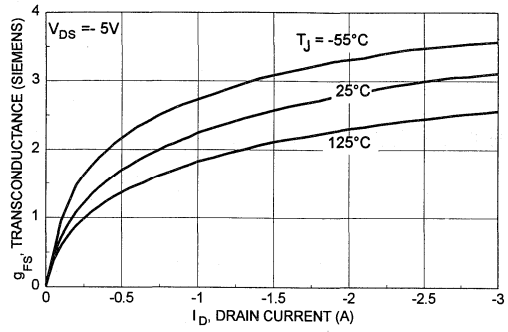


Figure 13. Transconductance Variation with Drain Current and Temperature

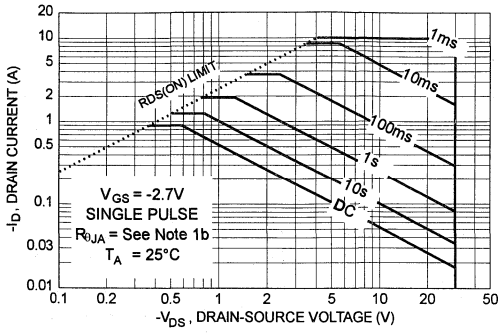


Figure 14. Maximum Safe Operating Area

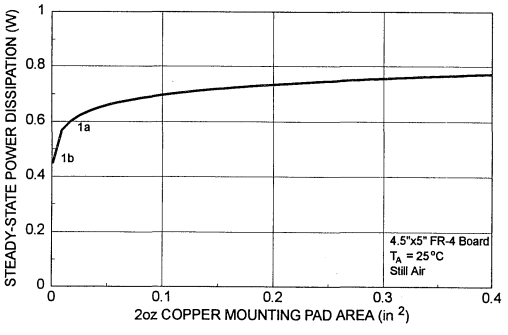


Figure 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

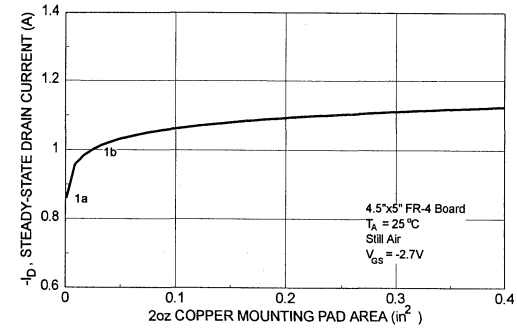


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

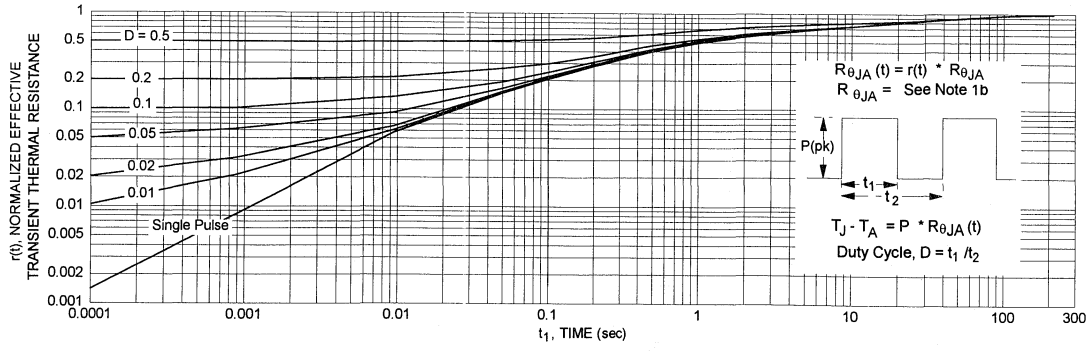


Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996
PRELIMINARY

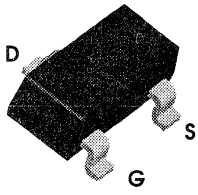
NDS335N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

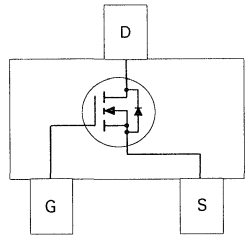
These N -Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.7 A, 20 V. $R_{DS(ON)}$ = 0.14 Ω @ V_{GS}= 2.7 V
  $R_{DS(ON)}$ = 0.11 Ω @ V_{GS}= 4.5 V.
- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDS335N	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage - Continuous	8	V
I_D	Maximum Drain Current - Continuous (Note 1a)	1.7	A
	- Pulsed	10	
P_D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J =125°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.5	0.7	1	V
		T_J =125°C	0.3	0.5	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 2.7 V, I_D = 1.7 A		0.084	0.14	Ω
		T_J =125°C		0.13	0.25	
		V_{GS} = 4.5 V, I_D = 1.7 A		0.065	0.11	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 2.7 V, V_{DS} = 5 V	5			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	10			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.7 A,		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		240		pF
C_{oss}	Output Capacitance			130		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GS} = 4.5 V, R_{Gen} = 6 Ω		8	20	ns
t_r	Turn - On Rise Time			29	45	ns
$t_{d(off)}$	Turn - Off Delay Time			28	40	ns
t_f	Turn - Off Fall Time			8	20	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.7 A, V_{GS} = 4.5 V		6.4	9	nC
Q_{gs}	Gate-Source Charge			0.5		nC
Q_{gd}	Gate-Drain Charge			2		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.42 A (Note 2)		0.8	1.2	V

Notes:

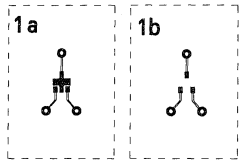
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

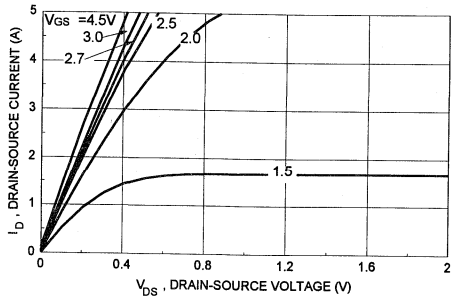


Figure 1. On-Region Characteristics

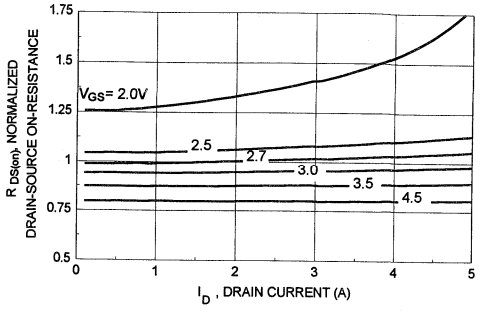


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

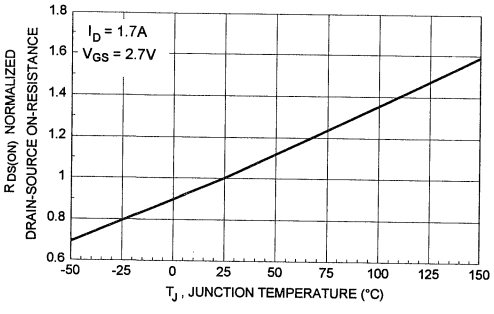


Figure 3. On-Resistance Variation with Temperature

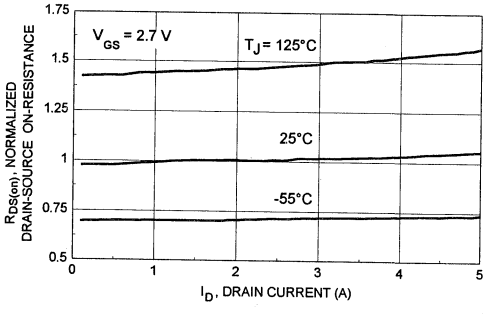


Figure 4. On-Resistance Variation with Drain Current and Temperature

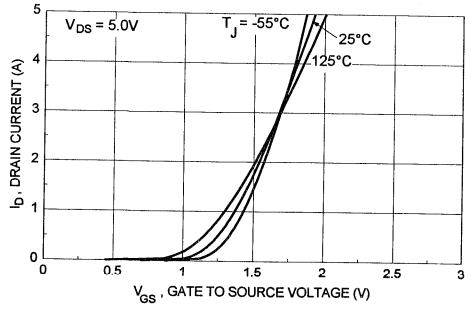


Figure 5. Transfer Characteristics

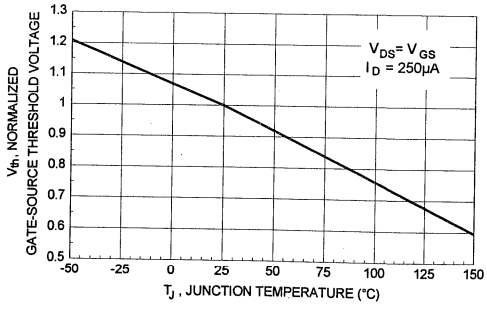


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

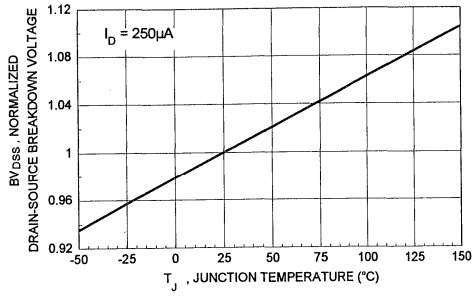


Figure 7. Breakdown Voltage Variation with Temperature

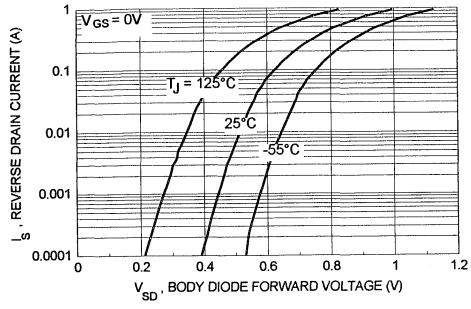


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

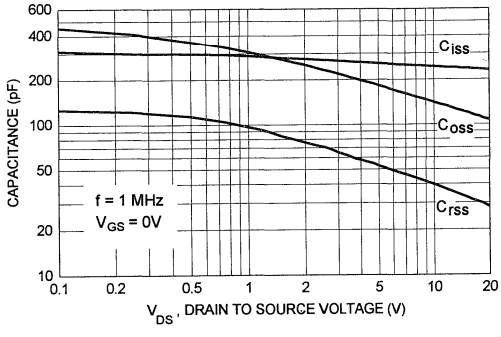


Figure 9. Capacitance Characteristics

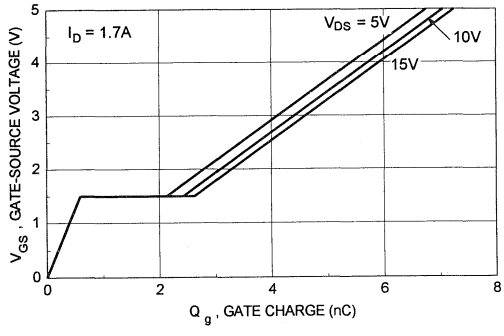


Figure 10. Gate Charge Characteristics

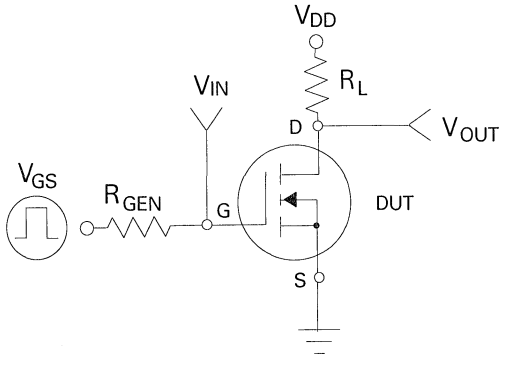


Figure 11. Switching Test Circuit

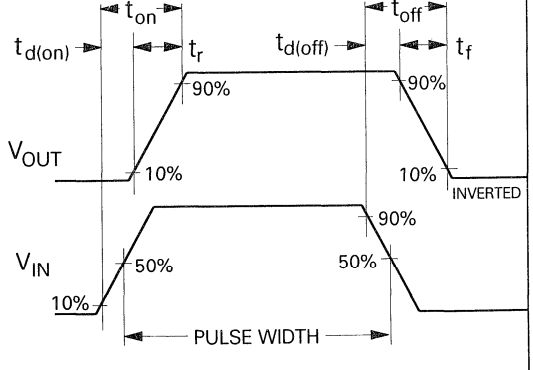


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

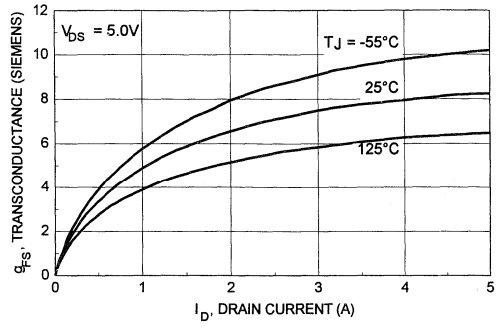


Figure 13. Transconductance Variation with Drain Current and Temperature

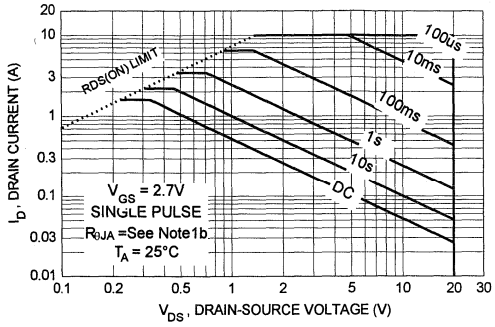
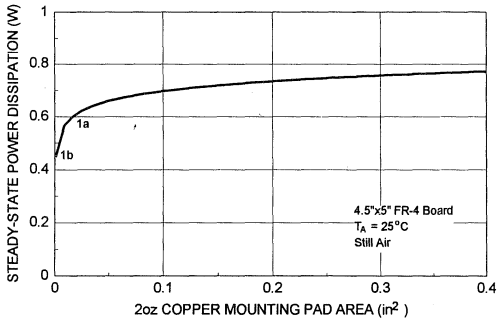


Figure 14. Maximum Safe Operating Area



Figue 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

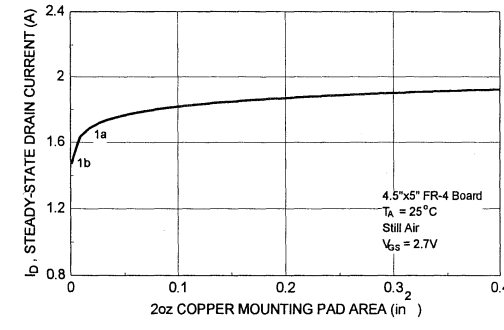


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

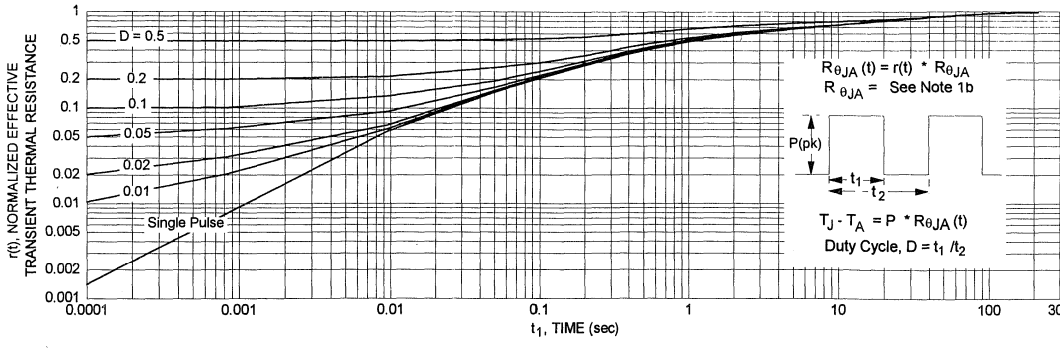


Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

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May 1996
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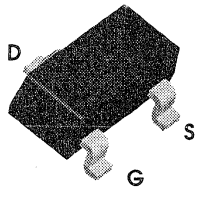
NDS336P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

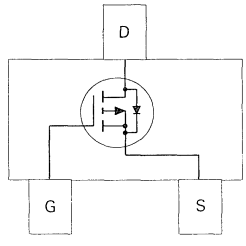
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -1.2 A, -20V. $R_{DS(ON)}$ = 0.27Ω @ V_{GS}=-2.7V
  $R_{DS(ON)}$ = 0.20Ω @ V_{GS}=-4.5V.
- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS336P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		-8	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	-1.2	A
	- Pulsed		-10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
			300	
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J =55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.5	-0.78	-1	V
		T_J =125°C	-0.3	-0.58	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -2.7 V, I_D = -1.2 A		0.22	0.27	Ω
		T_J =125°C		0.34	0.49	
		V_{GS} = -4.5 V, I_D = -1.3 A		0.16	0.2	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -2.7 V, V_{DS} = -5 V	-2			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.2 A		-3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		360		pF
C_{oss}	Output Capacitance			170		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		8	15	ns
t_r	Turn - On Rise Time			29	50	ns
$t_{D(off)}$	Turn - Off Delay Time			33	60	ns
t_f	Turn - Off Fall Time			23	45	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -1.2 A, V_{GS} = -4.5 V		5.7	8.5	nC
Q_{gs}	Gate-Source Charge			0.7		nC
Q_{gd}	Gate-Drain Charge			1.8		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 (Note 2)		-0.65	-1.2	V

Notes:

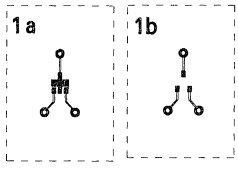
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

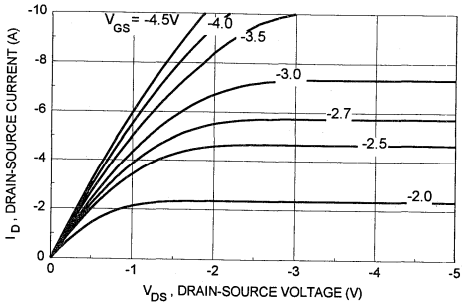


Figure 1. On-Region Characteristics

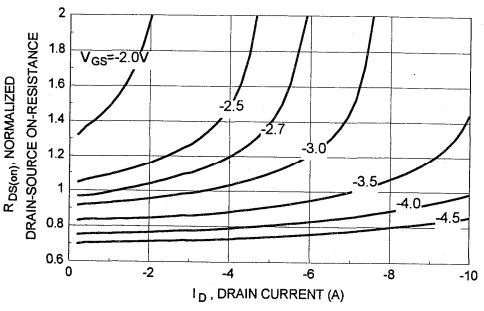


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

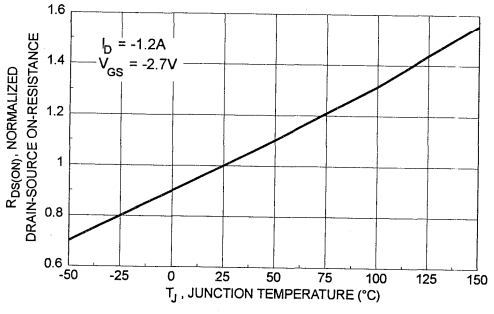


Figure 3. On-Resistance Variation with Temperature

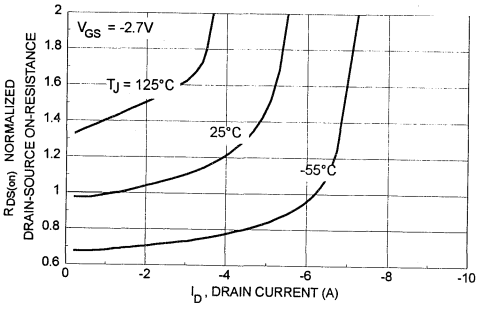


Figure 4. On-Resistance Variation with Drain Current and Temperature

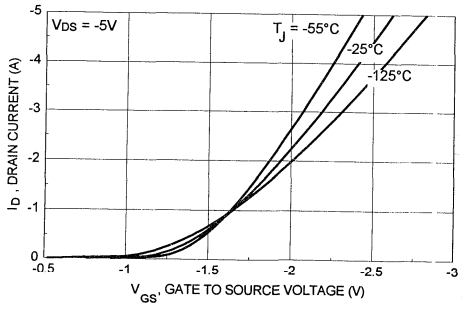


Figure 5. Transfer Characteristics

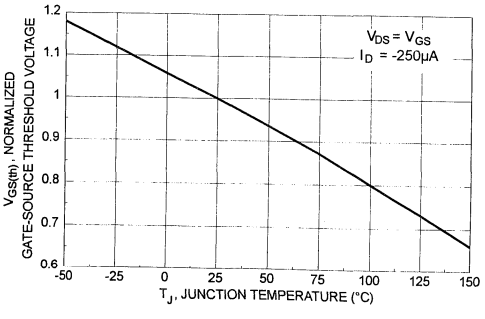


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

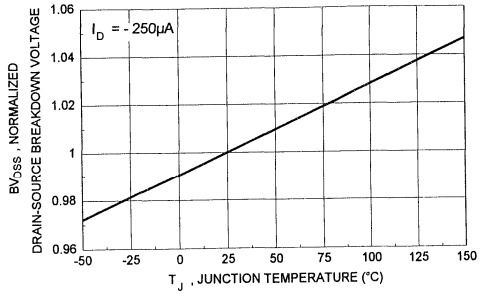


Figure 7. Breakdown Voltage Variation with Temperature

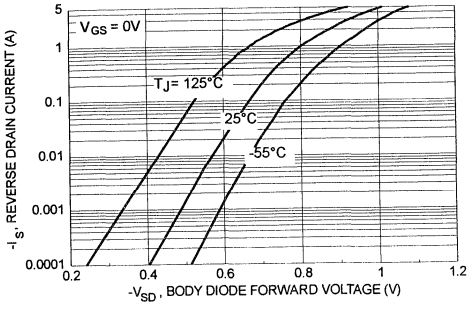


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

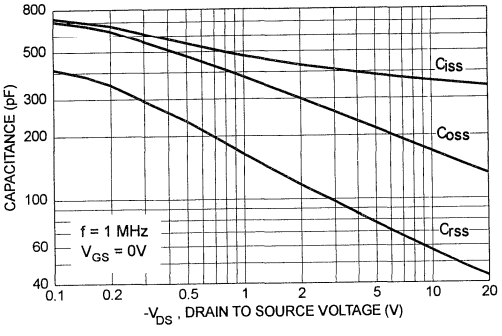


Figure 9. Capacitance Characteristics

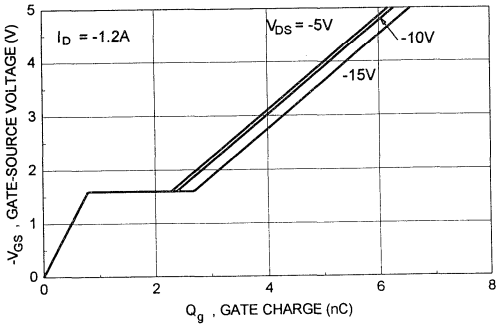


Figure 10. Gate Charge Characteristics

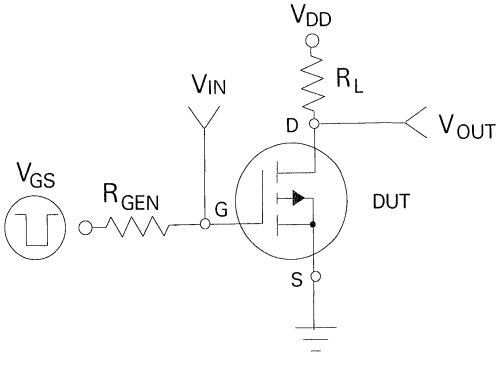


Figure 11. Switching Test Circuit

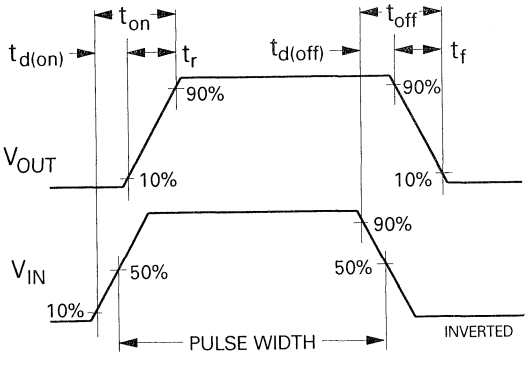


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

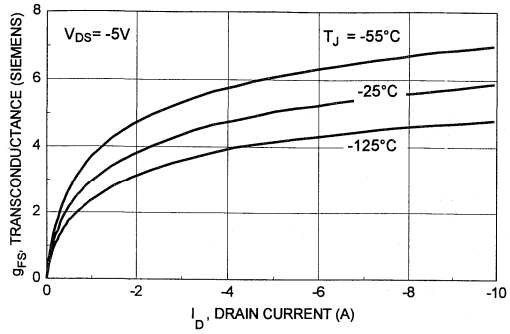


Figure 13. Transconductance Variation with Drain Current and Temperature

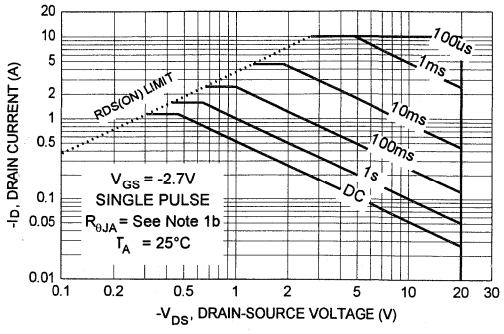


Figure 14. Maximum Safe Operating Area

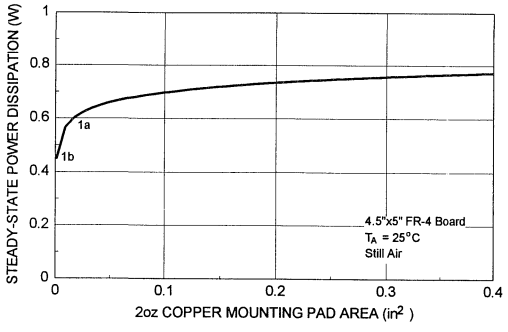


Figure 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

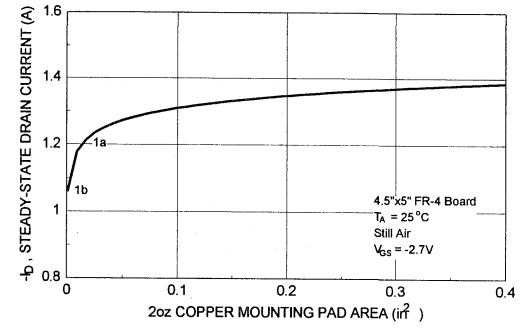


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

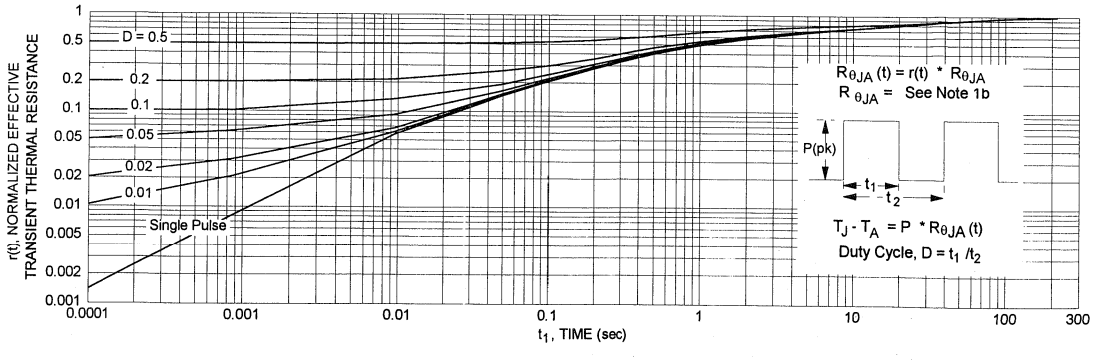


Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

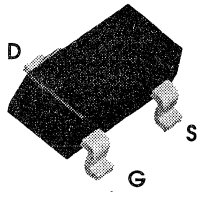
NDS351N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

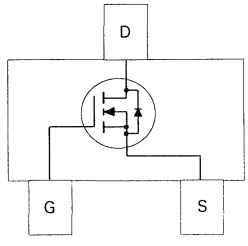
These N-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.1A, 30V. $R_{DS(ON)}$ = 0.25Ω @ V_{GS} = 4.5V.
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS351N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage - Continuous		20	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	± 1.1	A
	- Pulsed		± 10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J =125°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.8	1.6	2	V
		T_J =125°C	0.5	1.3	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 1.1 A		0.185	0.25	Ω
		T_J =125°C		0.26	0.37	
		V_{GS} = 10 V, I_D = 1.4 A		0.135	0.16	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	5			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.1 A		2.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		140		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			18		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 50 Ω		9	15	ns
t_r	Turn - On Rise Time			16	30	ns
$t_{d(off)}$	Turn - Off Delay Time			26	50	ns
t_f	Turn - Off Fall Time			19	40	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.1 A, V_{GS} = 5 V		2	3.5	nC
Q_{gs}	Gate-Source Charge				1	nC
Q_{gd}	Gate-Drain Charge				2	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.1 A (Note 2)		0.8	1.2	V

Notes:

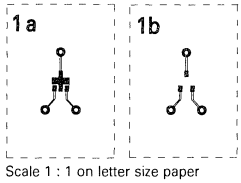
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

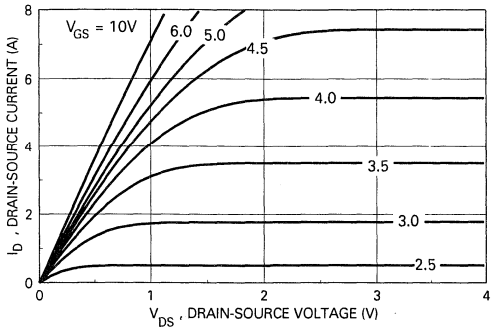


Figure 1. On-Region Characteristics

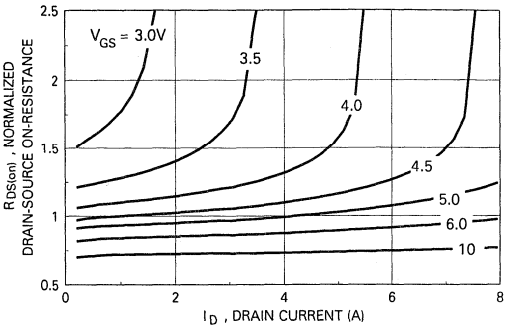


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

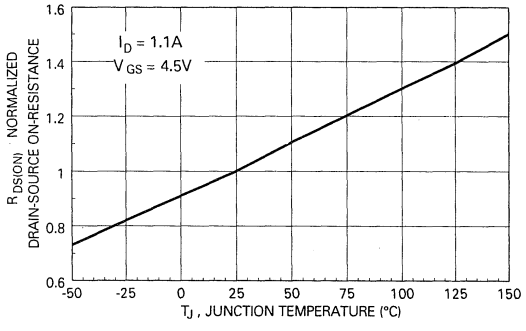


Figure 3. On-Resistance Variation with Temperature

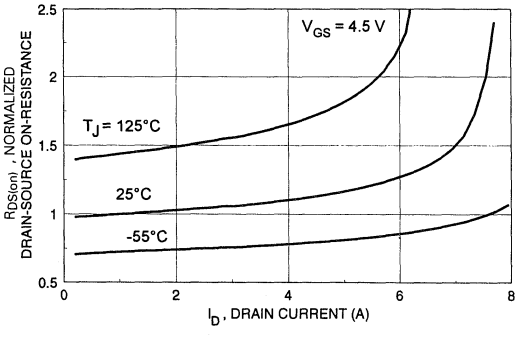


Figure 4. On-Resistance Variation with Drain Current and Temperature

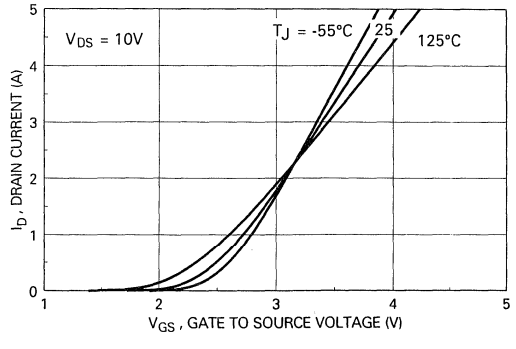


Figure 5. Transfer Characteristics

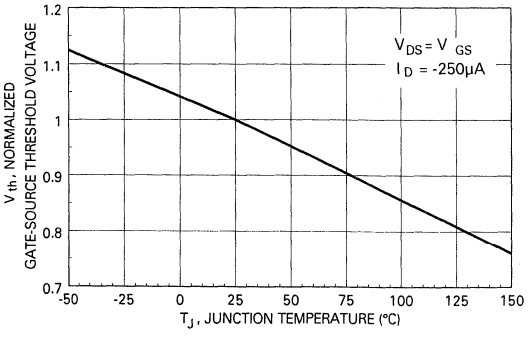


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

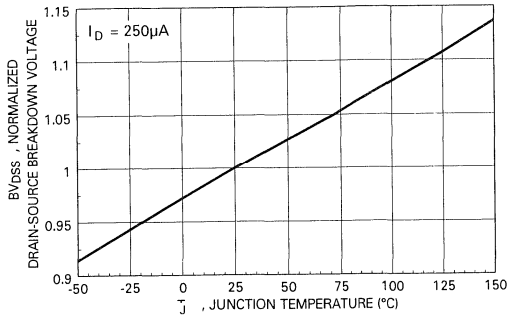


Figure 7. Breakdown Voltage Variation with Temperature

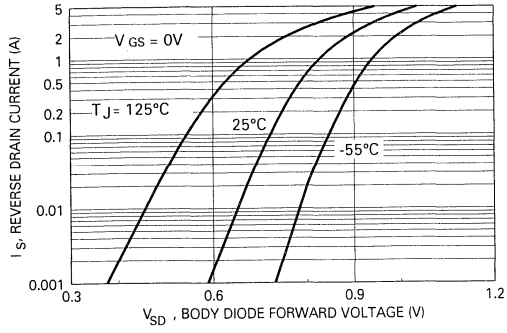


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

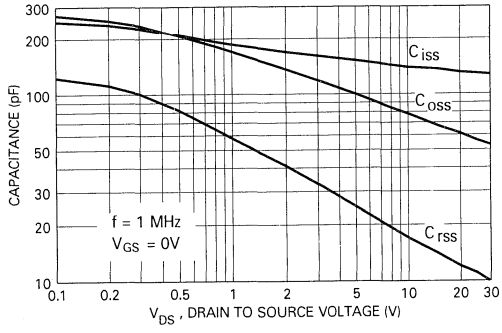


Figure 9. Capacitance Characteristics

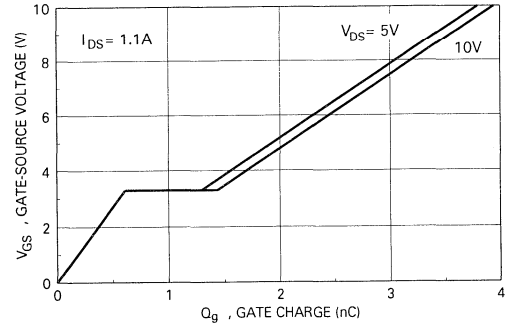


Figure 10. Gate Charge Characteristics

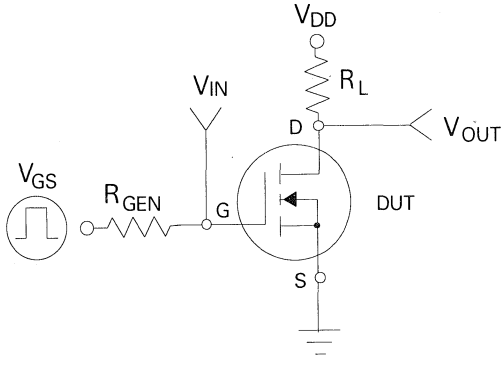


Figure 11. Switching Test Circuit

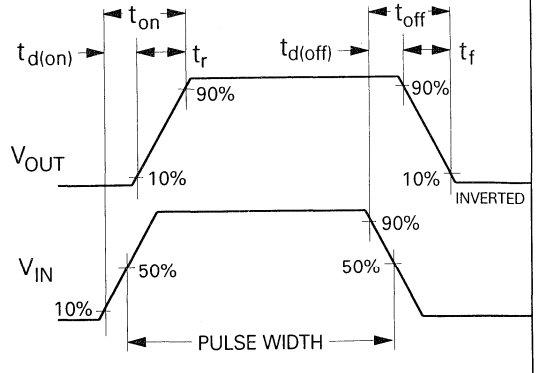


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

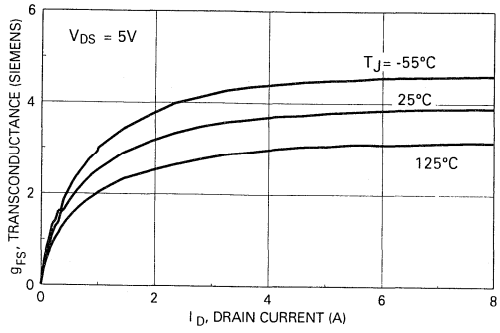


Figure 13. Transconductance Variation with Drain Current and Temperature

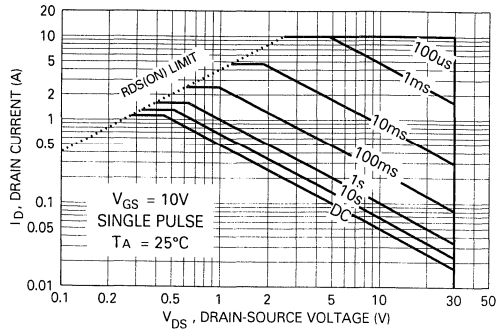


Figure 14. Maximum Safe Operating Area

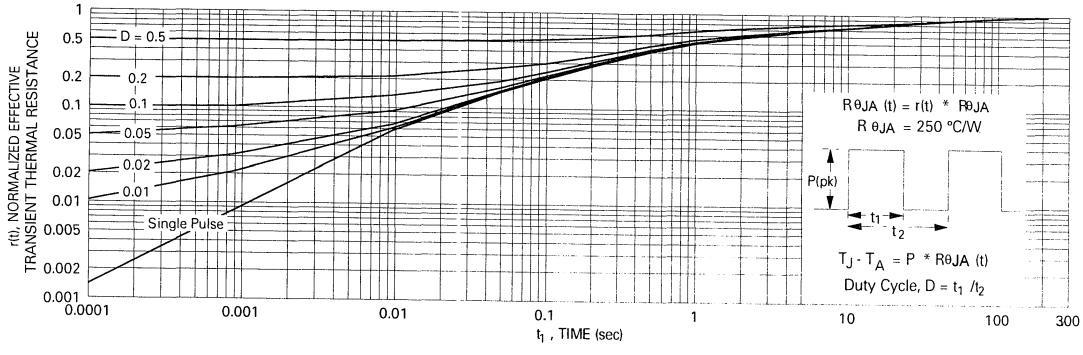


Figure 15. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

NDS352AP

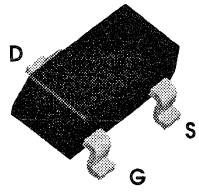
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

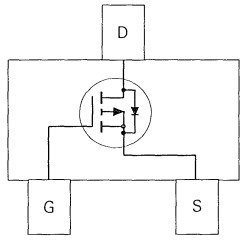
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -0.9 A, -30 V. $R_{DS(ON)}$ = 0.5 Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 0.3 Ω @ V_{GS} = -10 V.
- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS352AP	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage - Continuous		±20	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	±0.9	A
	- Pulsed		±10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J =125°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1.7	-2.5	V
		T_J =125°C	-0.5	-1.4	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -0.9 A		0.45	0.5	Ω
		T_J =125°C		0.65	0.7	
		V_{GS} = -10 V, I_D = -1 A		0.25	0.3	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-2			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -0.9 A		1.9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		135		pF
C_{oss}	Output Capacitance			88		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -6 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		5	10	ns
t_r	Turn - On Rise Time			17	30	ns
$t_{D(off)}$	Turn - Off Delay Time			35	70	ns
t_f	Turn - Off Fall Time			30	60	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -0.9 A, V_{GS} = -4.5 V		2	3	nC
Q_{gs}	Gate-Source Charge			0.5		nC
Q_{gd}	Gate-Drain Charge			1		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 (Note 2)		-0.8	-1.2	V

Notes:

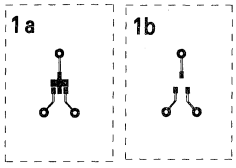
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

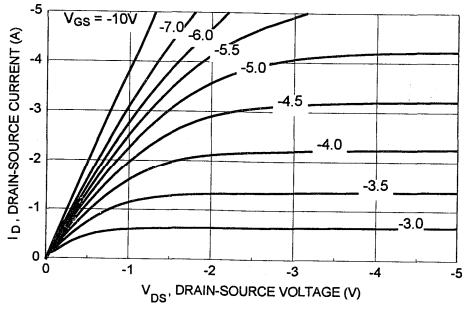


Figure 1. On-Region Characteristics

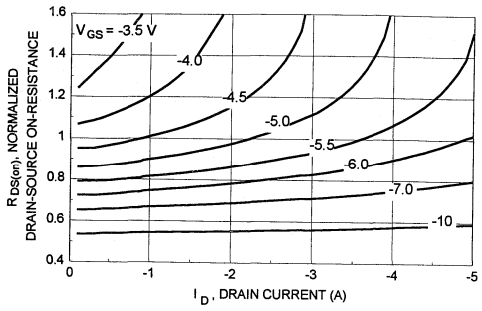


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

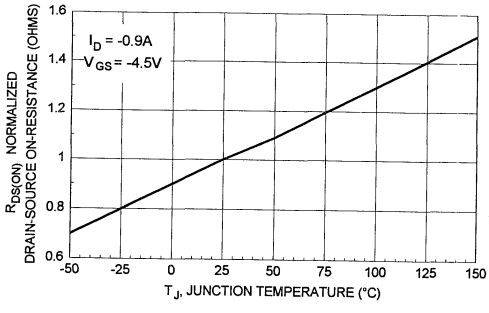


Figure 3. On-Resistance Variation with Temperature

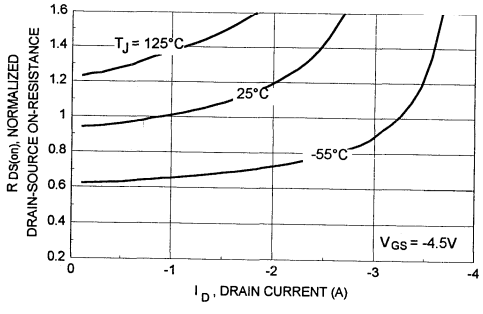


Figure 4. On-Resistance Variation with Drain Current and Temperature

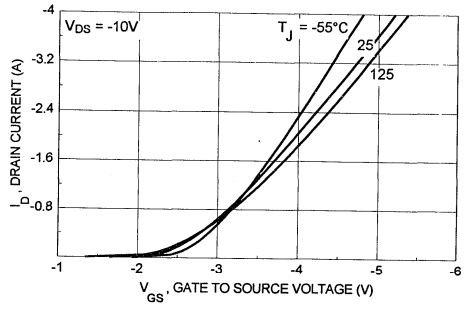


Figure 5. Transfer Characteristics

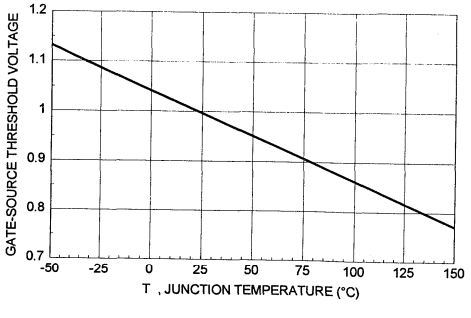


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

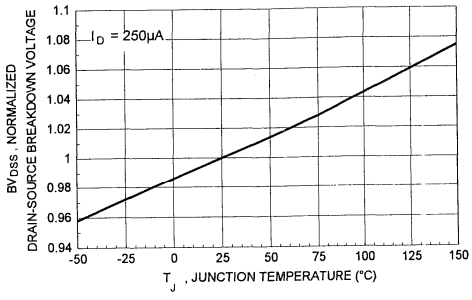


Figure 7. Breakdown Voltage Variation with Temperature

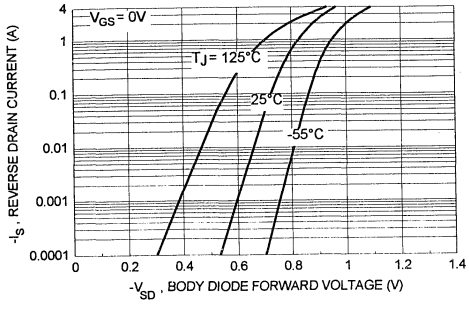


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

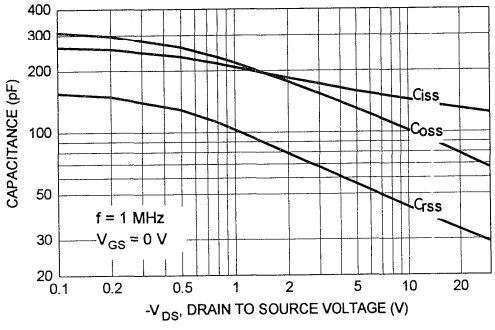


Figure 9. Capacitance Characteristics

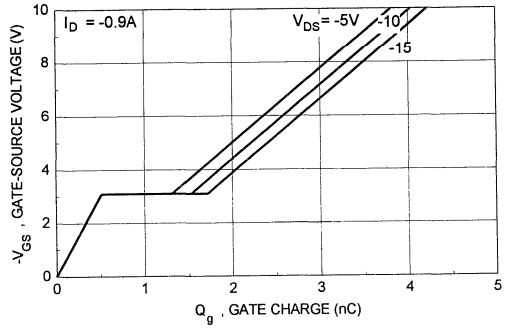


Figure 10. Gate Charge Characteristics

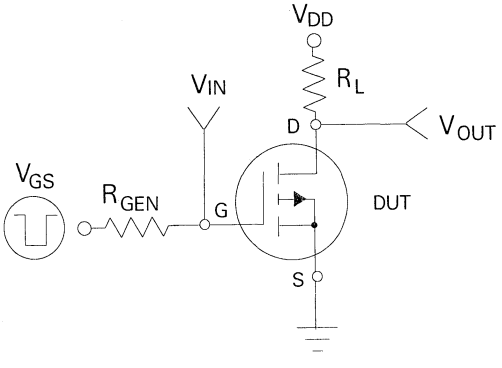


Figure 11. Switching Test Circuit

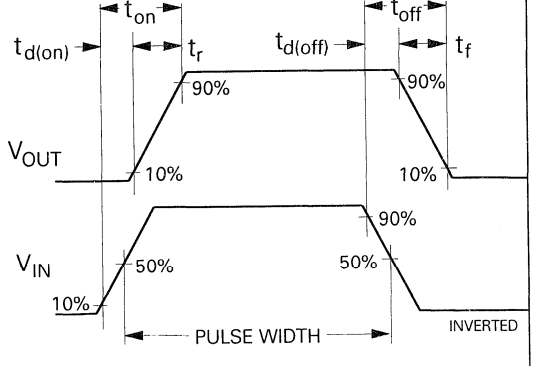


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

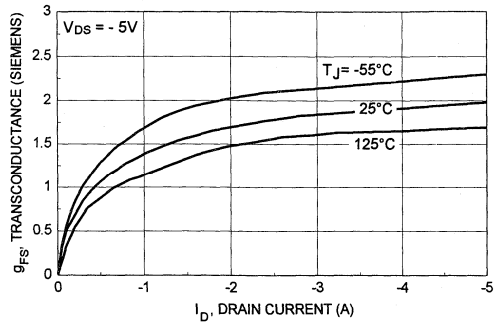


Figure 13. Transconductance Variation with Drain Current and Temperature

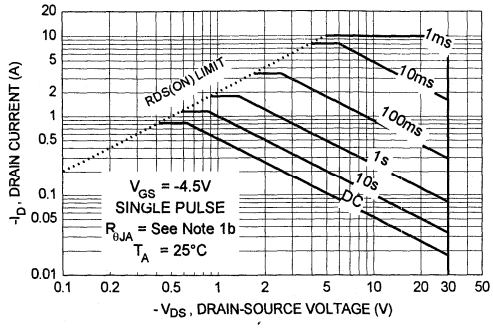
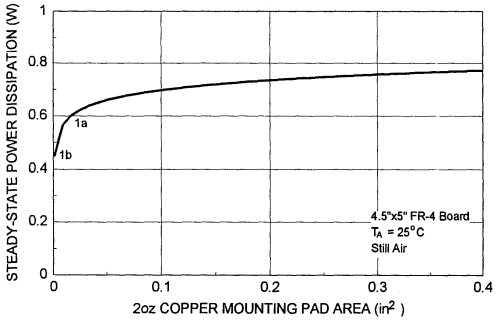


Figure 14. Maximum Safe Operating Area



Figue 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

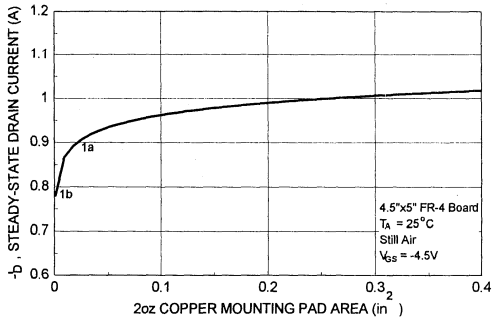


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

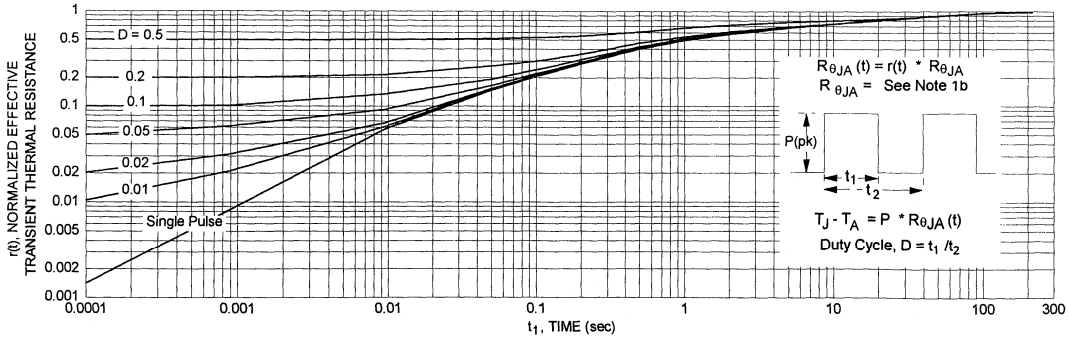


Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

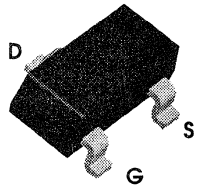
NDS352P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

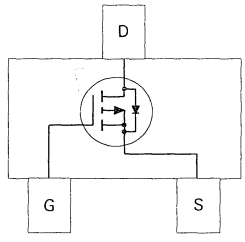
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -0.85A, -20V. $R_{DS(ON)}$ = 0.5Ω @ V_{GS} = -4.5V.
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS352P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		±12	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	±0.85	A
	- Pulsed		±10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-5	µA
		T_J =125°C			-20	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1.6	-2.5	V
		T_J =125°C	-0.5	-1.3	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -0.85 A		0.46	0.5	Ω
		T_J =125°C		0.59	0.7	
		V_{GS} = -10 V, I_D = -1 A			0.35	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-2			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -0.85 A		1.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		125		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GS} = -10 V, R_{GEN} = 50 Ω		8	15	ns
t_r	Turn - On Rise Time			19	30	ns
$t_{d(off)}$	Turn - Off Delay Time			64	90	ns
t_f	Turn - Off Fall Time			61	90	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -0.85 A, V_{GS} = -5 V		2.2	4	nC
Q_{gs}	Gate-Source Charge				1	nC
Q_{gd}	Gate-Drain Charge				2	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.85 A (Note 2)		-0.92	-1.2	V

Notes:

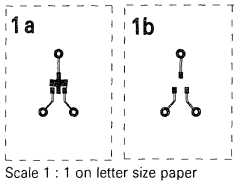
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

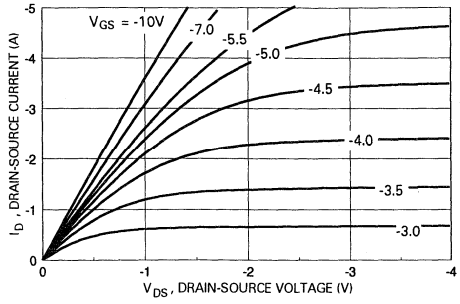


Figure 1. On-Region Characteristics

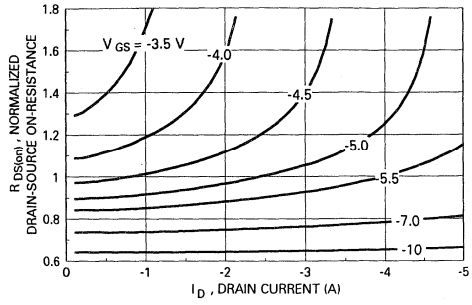


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

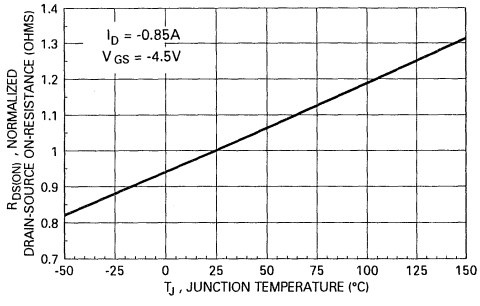


Figure 3. On-Resistance Variation with Temperature

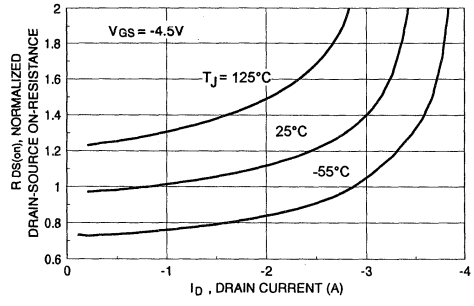


Figure 4. On-Resistance Variation with Drain Current and Temperature

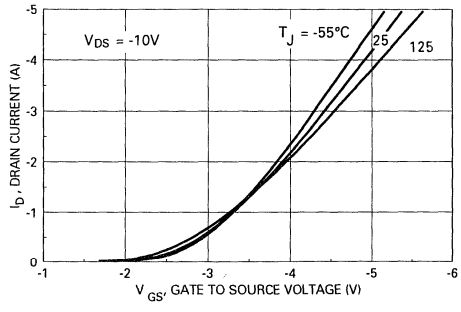


Figure 5. Transfer Characteristics

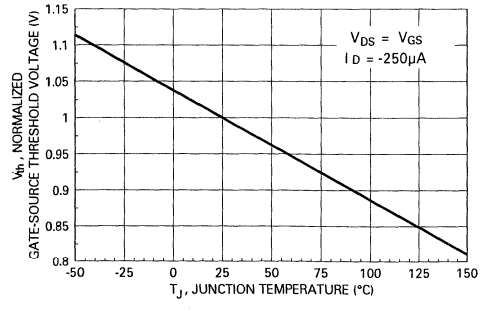


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

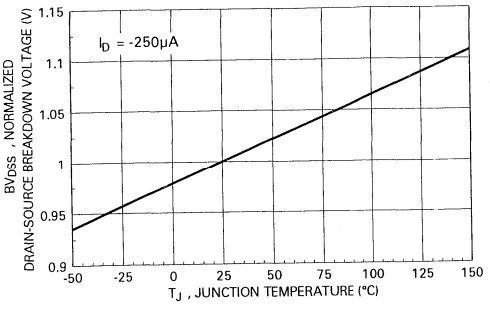


Figure 7. Breakdown Voltage Variation with Temperature

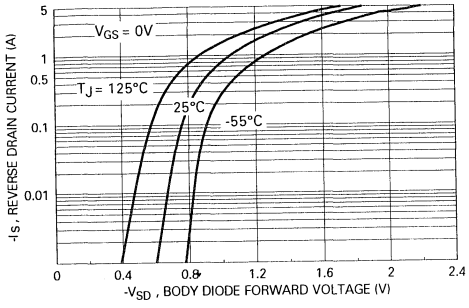


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

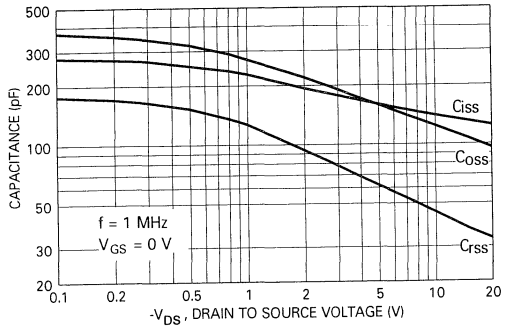


Figure 9. Capacitance Characteristics

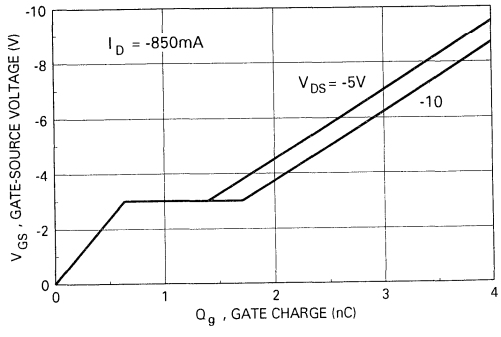


Figure 10. Gate Charge Characteristics

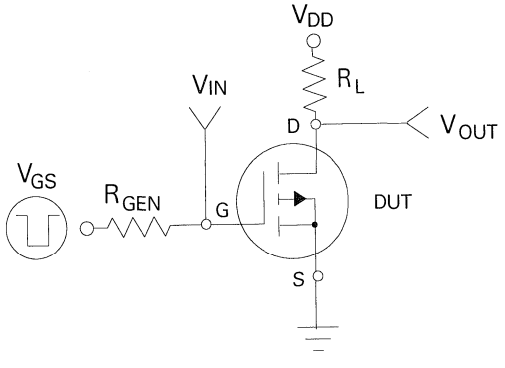


Figure 11. Switching Test Circuit

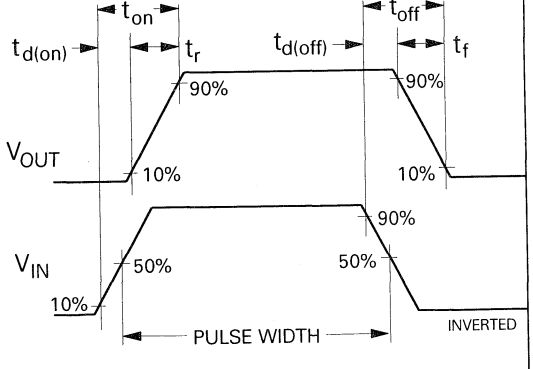


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

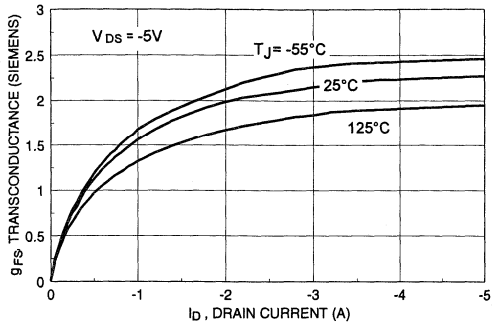


Figure 13. Transconductance Variation with Drain Current and Temperature

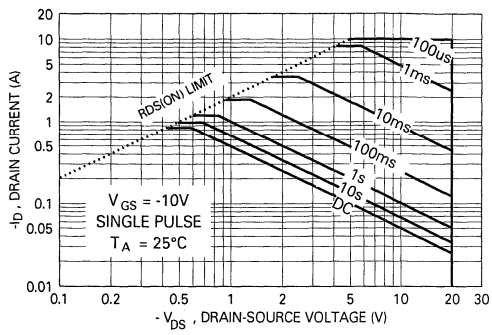


Figure 14. Maximum Safe Operating Area

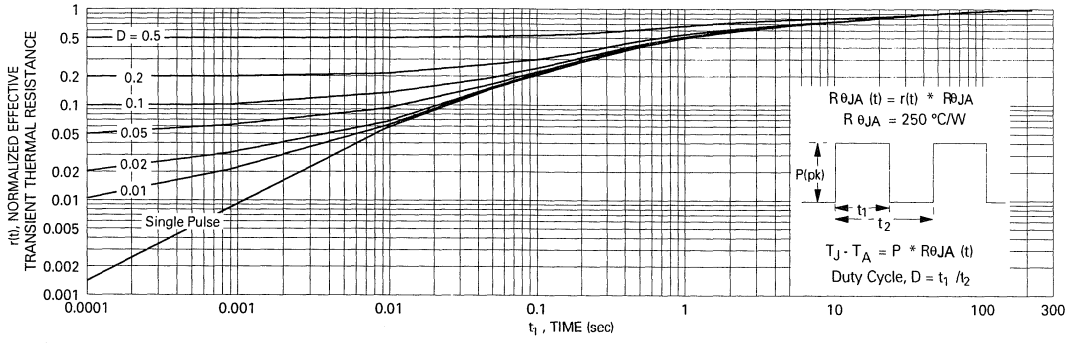


Figure 15. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

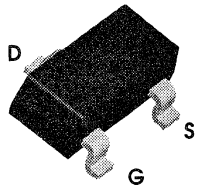
NDS355N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

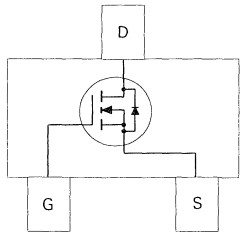
These N-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMICA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 1.6A, 30V. $R_{DS(ON)}$ = 0.125Ω @ V_{GS} = 4.5V.
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface mount package.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS355N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage - Continuous		20	V
I_D	Drain Current - Continuous	(Note 1a)	± 1.6	A
	- Pulsed		± 10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to -Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J=125°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	2	V
		T_J=125°C	0.5	1.3	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 1.6 A			0.125	Ω
		T_J=125°C			0.25	
		V_{GS} = 10 V, I_D = 1.9 A			0.085	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	6			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 1.6 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		245		pF
C_{oss}	Output Capacitance			130		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		15	30	ns
t_r	Turn - On Rise Time			14	30	ns
$t_{D(off)}$	Turn - Off Delay Time			12	25	ns
t_f	Turn - Off Fall Time			4	10	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 1.6 A, V_{GS} = 5 V		3.5	5	nC
Q_{gs}	Gate-Source Charge				1	nC
Q_{gd}	Gate-Drain Charge				2	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				0.6	A
I_{SM}	Maximum Pulse Source Current (Note 2)				6	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.6 A		0.8	1.2	V

Notes:

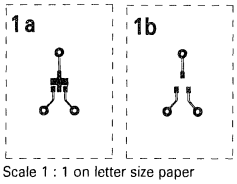
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

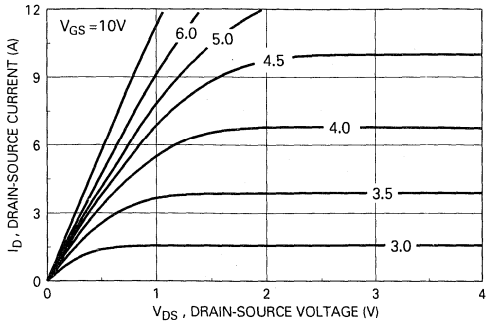


Figure 1. On-Region Characteristics

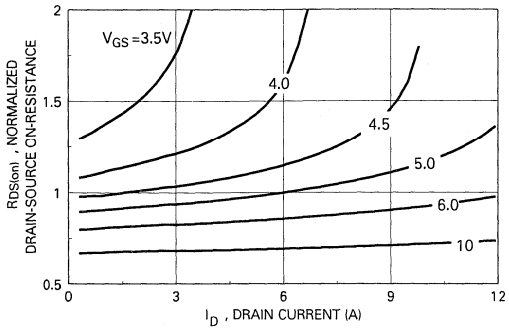


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

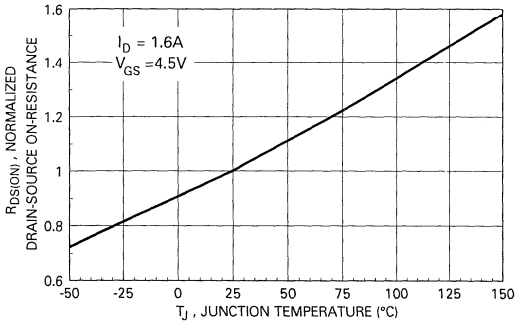


Figure 3. On-Resistance Variation with Temperature

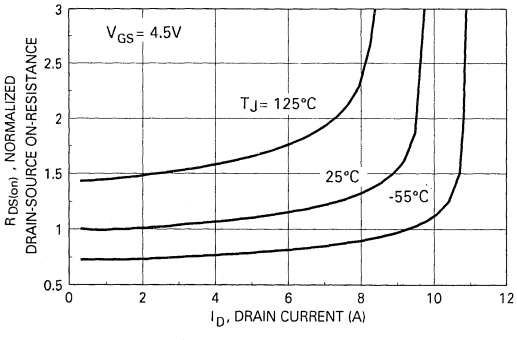


Figure 4. On-Resistance Variation with Drain Current and Temperature

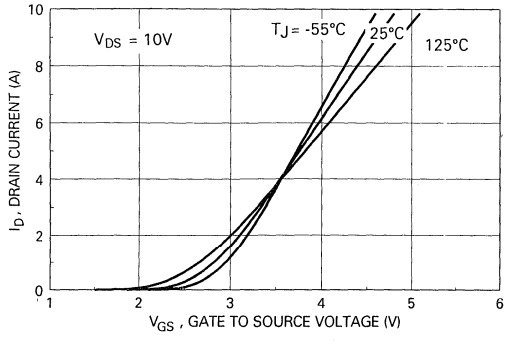


Figure 5. Transfer Characteristics

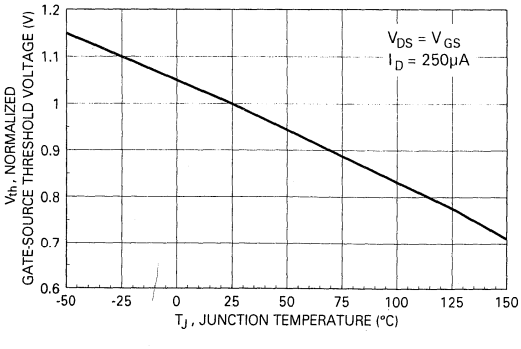


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

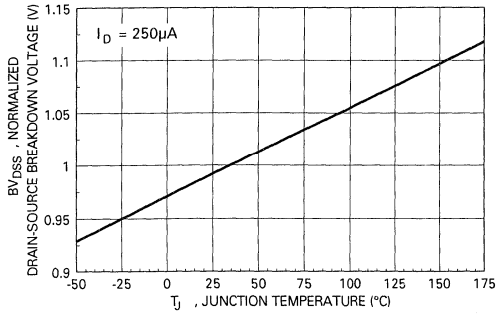


Figure 7. Breakdown Voltage Variation with Temperature

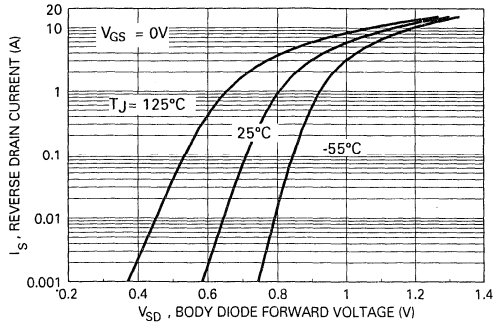


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

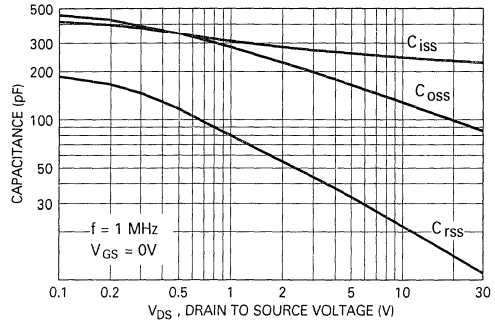


Figure 9. Capacitance Characteristics

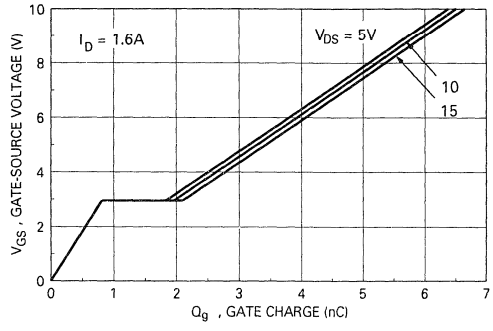


Figure 10. Gate Charge Characteristics

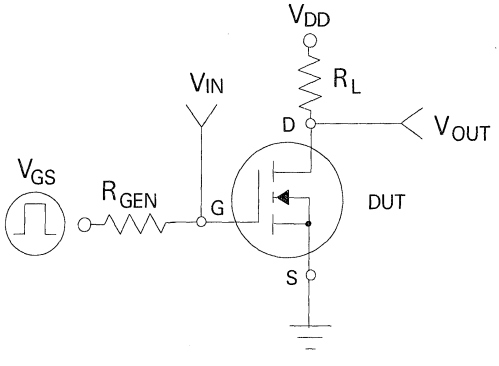


Figure 11. Switching Test Circuit

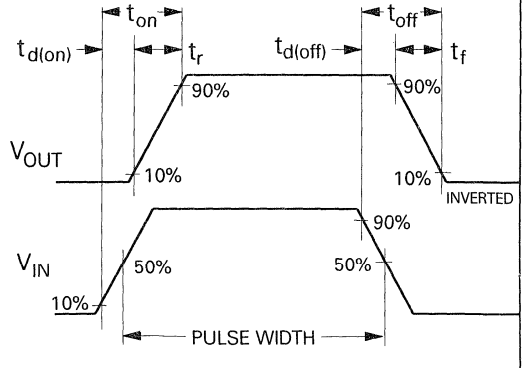


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

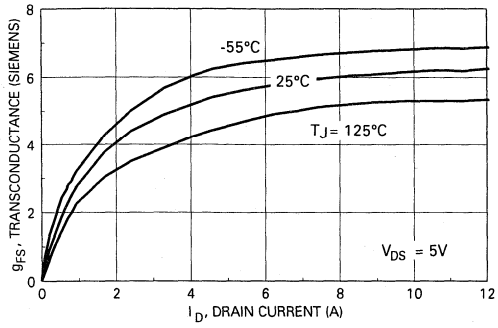


Figure 13. Transconductance Variation with Drain Current and Temperature

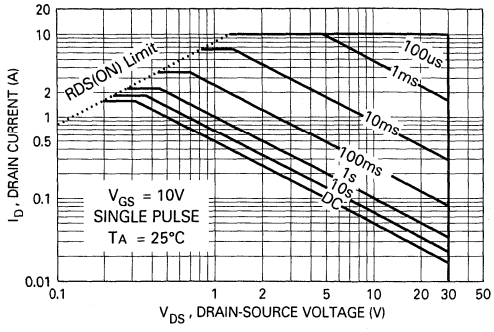


Figure 14. Maximum Safe Operating Area

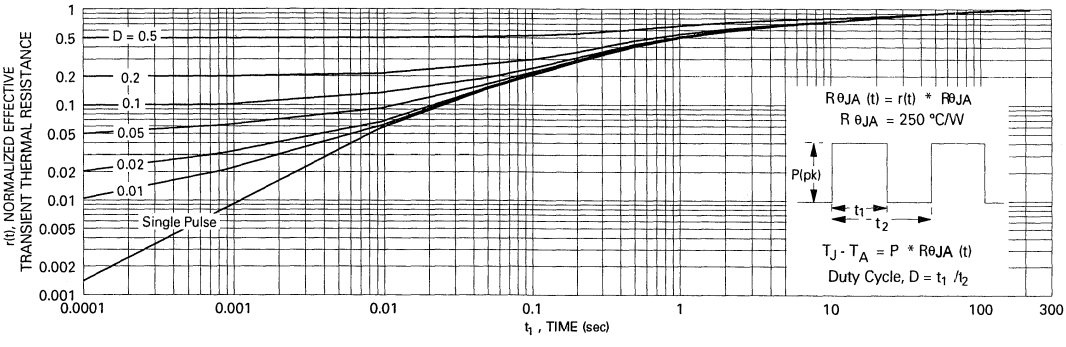


Figure 15. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

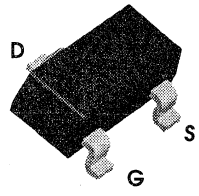
NDS356AP
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

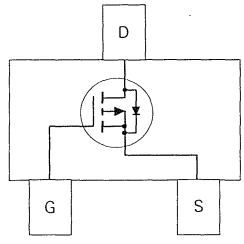
These P -Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -1.1 A, -30 V, $R_{DS(ON)}$ = 0.3 Ω @ V_{GS}=-4.5 V
  $R_{DS(ON)}$ = 0.2 Ω @ V_{GS}=-10 V.
- Industry standard outline SOT-23 surface mount package using poprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS356AP	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage - Continuous		±20	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	±1.1	A
	- Pulsed		±10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J =55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1.6	-2.5	V
		T_J =125°C	-0.5	-1.3	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -1.1 A		0.25	0.3	Ω
		T_J =125°C		0.35	0.4	
		V_{GS} = -10 V, I_D = -1.3 A		0.14	0.2	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-3			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.1 A		2		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		280		pF
C_{oss}	Output Capacitance			170		pF
C_{rss}	Reverse Transfer Capacitance			65		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn - On Rise Time			24	45	ns
$t_{D(off)}$	Turn - Off Delay Time			15	30	ns
t_f	Turn - Off Fall Time			8	16	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -1.1 A, V_{GS} = -4.5 V		3.1	4.4	nC
Q_{gs}	Gate-Source Charge			0.7		nC
Q_{gd}	Gate-Drain Charge			1.5		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				-0.42	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-10	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 A (Note 2)		-0.8	-1.2	V

Notes:

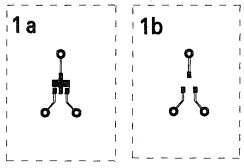
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in² pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

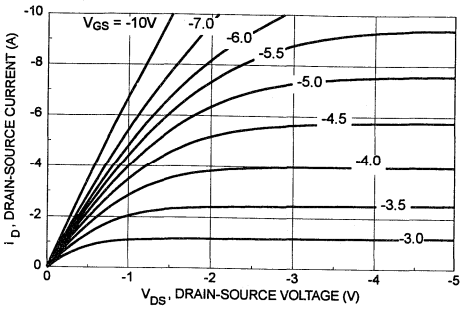


Figure 1. On-Region Characteristics

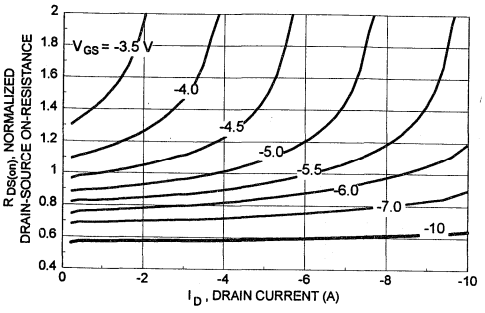


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

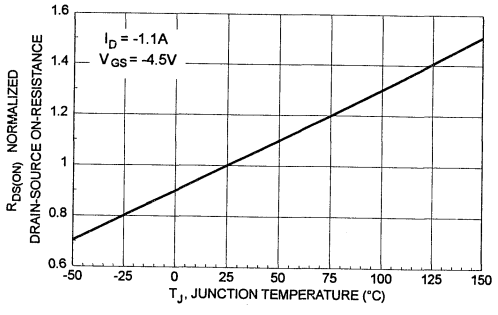


Figure 3. On-Resistance Variation with Temperature

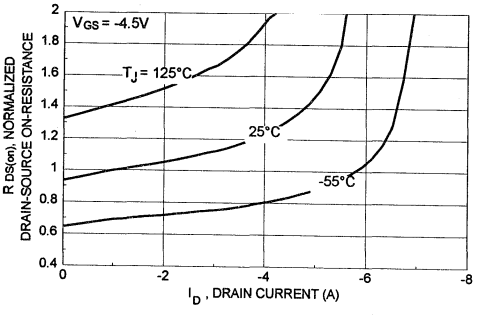


Figure 4. On-Resistance Variation with Drain Current and Temperature

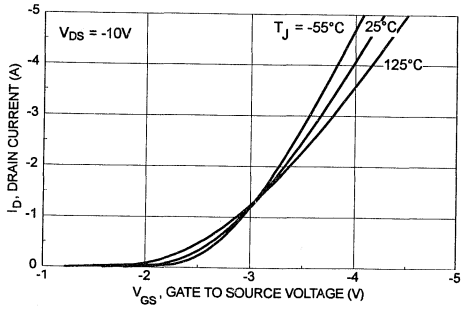


Figure 5. Transfer Characteristics

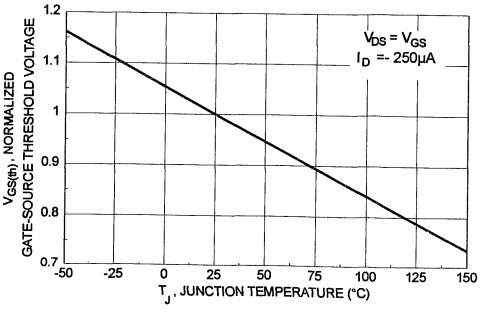


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

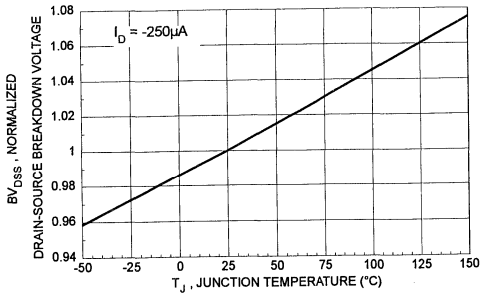


Figure 7. Breakdown Voltage Variation with Temperature

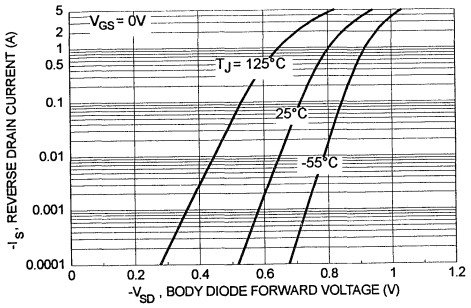


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

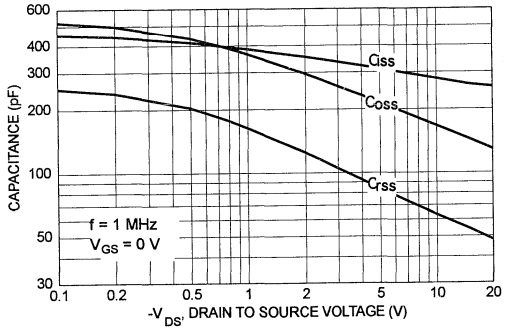


Figure 9. Capacitance Characteristics

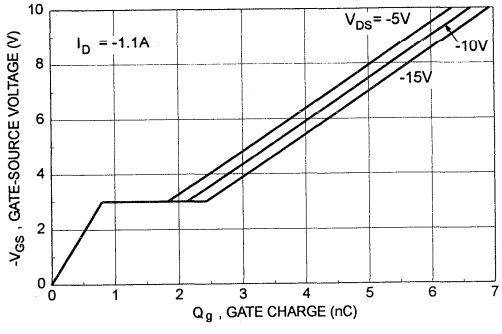


Figure 10. Gate Charge Characteristics

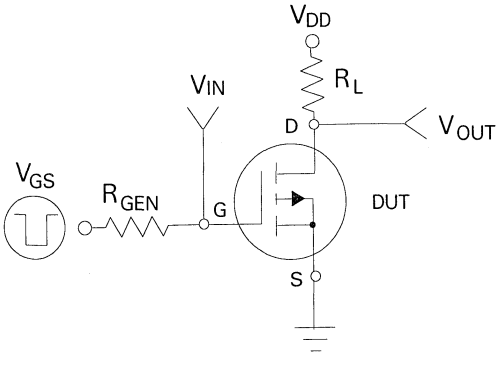


Figure 11. Switching Test Circuit

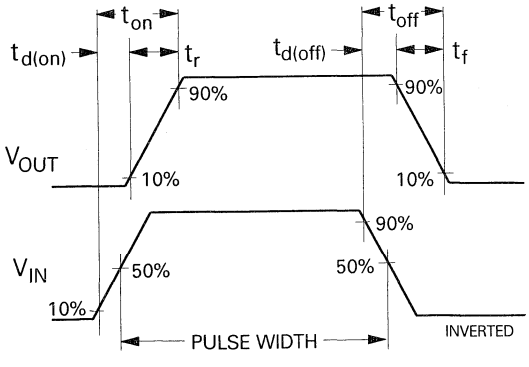


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

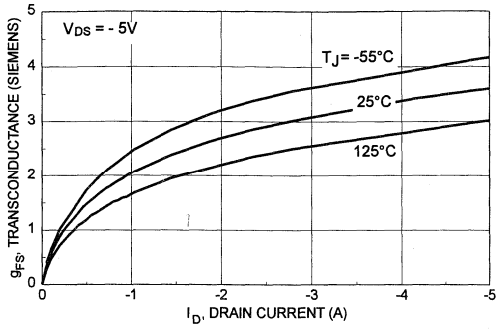


Figure 13. Transconductance Variation with Drain Current and Temperature

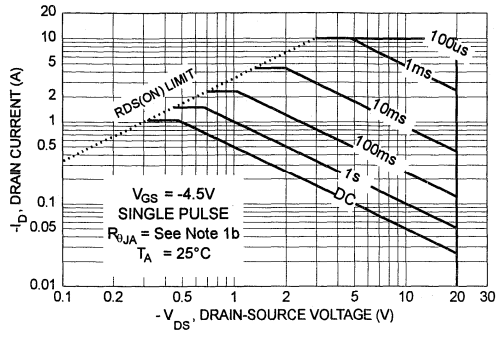
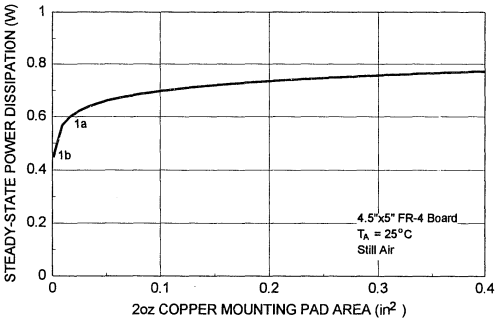


Figure 14. Maximum Safe Operating Area



Figue 15. SuperSOT™-3 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

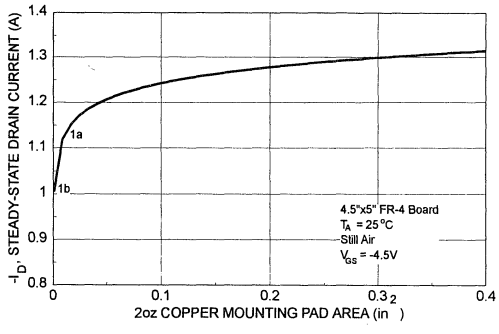


Figure 16. Maximum Steady-State Drain Current versus Copper Mounting Pad Area

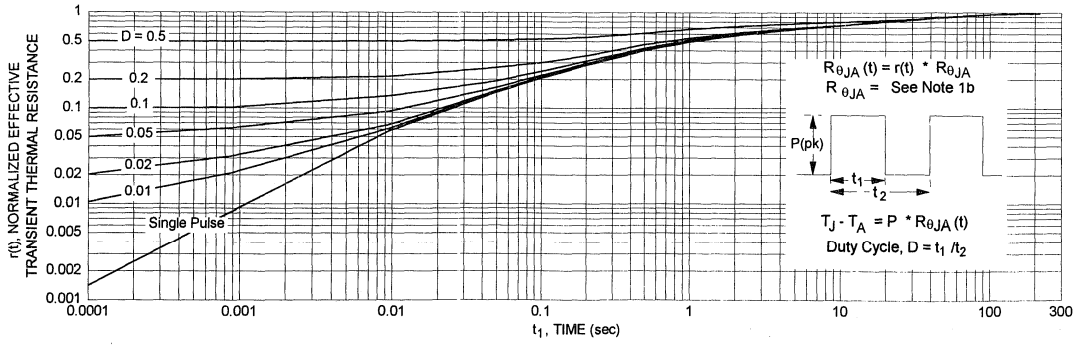


Figure 17. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1b. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

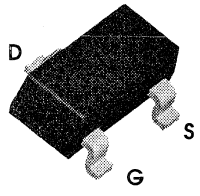
NDS356P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

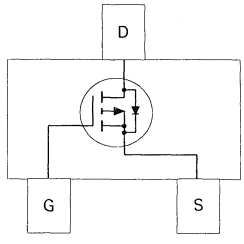
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management, portable electronics, and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -1.1 A, -20V. $R_{DS(ON)}$ = 0.3Ω @ V_{GS} = -4.5V.
- Proprietary package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.
- Compact industry standard SOT-23 surface mount package.



SuperSOT™-3 (SOT-23)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS356P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		± 12	V
I_D	Maximum Drain Current - Continuous	(Note 1a)	±1.1	A
	- Pulsed		±10	
P_D	Maximum Power Dissipation	(Note 1a)	0.5	W
		(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-5	µA
		T_J =125°C			-20	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1.6	-2.5	V
		T_J =125°C	-0.5	-1.3	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -1.1 A			0.3	Ω
		T_J =125°C			0.4	
		V_{GS} = -10 V, I_D = -1.3 A			0.21	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-3			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.1 A		1.8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		180		pF
C_{oss}	Output Capacitance			255		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GS} = -10 V, R_{GEN} = 50 Ω		7	15	ns
t_r	Turn - On Rise Time			17	30	ns
$t_{d(off)}$	Turn - Off Delay Time			56	90	ns
t_f	Turn - Off Fall Time			41	80	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -1.1 A, V_{GS} = -5 V		3.5	5	nC
Q_{gs}	Gate-Source Charge				1.5	nC
Q_{gd}	Gate-Drain Charge				2	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				-4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.1 A (Note 2)		-0.85	-1.2	V

Notes:

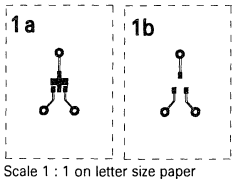
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 250°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

b. 270°C/W when mounted on a 0.001 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

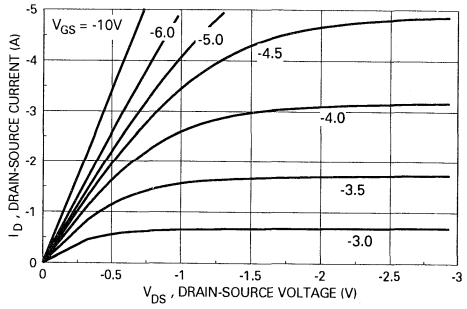


Figure 1. On-Region Characteristics

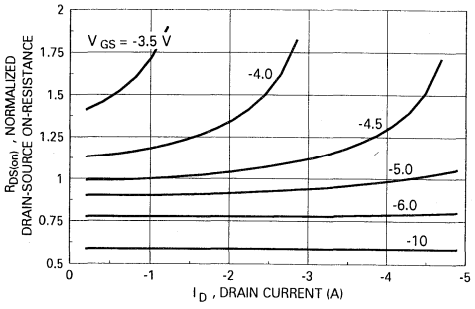


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

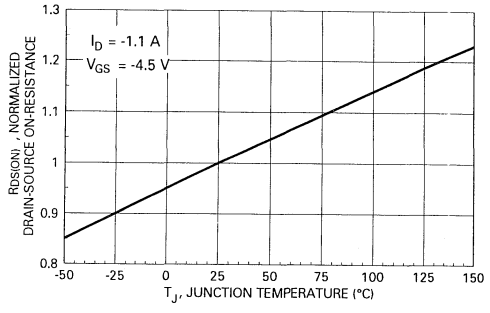


Figure 3. On-Resistance Variation with Temperature

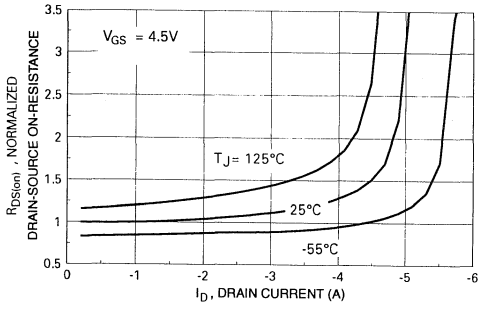


Figure 4. On-Resistance Variation with Drain Current and Temperature

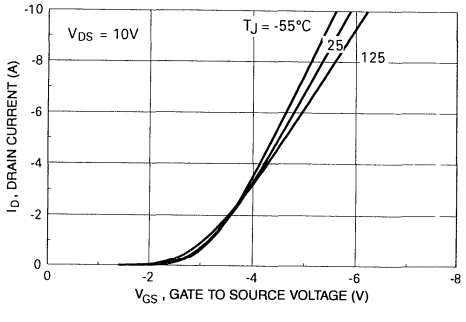


Figure 5. Transfer Characteristics

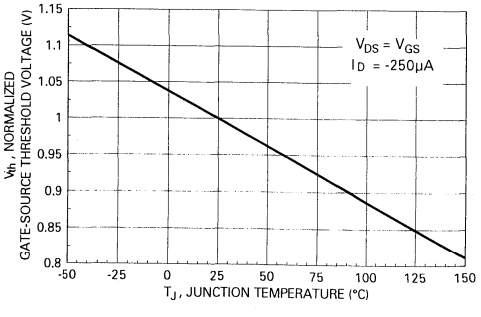


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

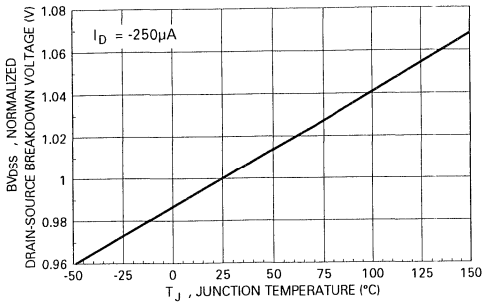


Figure 7. Breakdown Voltage Variation with Temperature

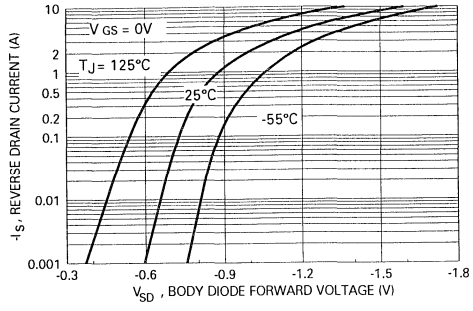


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

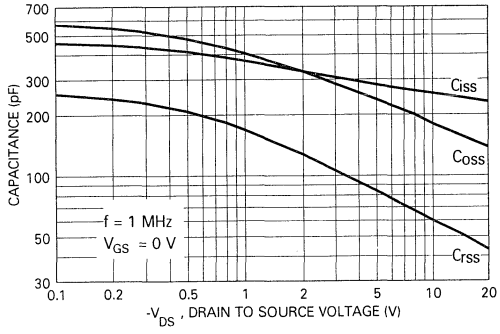


Figure 9. Capacitance Characteristics

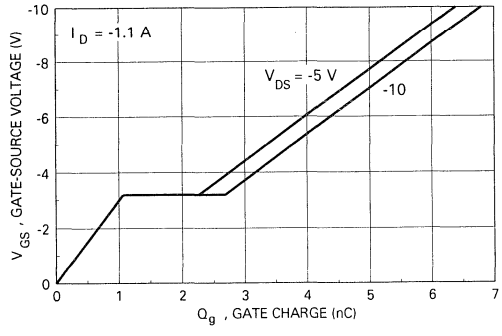


Figure 10. Gate Charge Characteristics

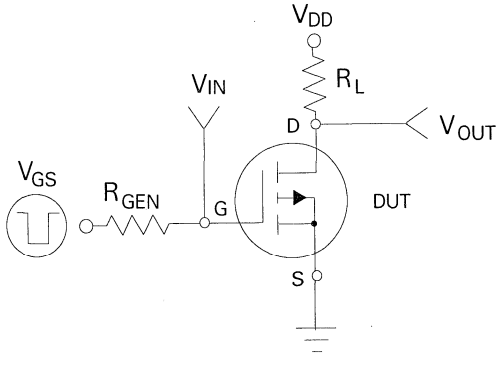


Figure 11. Switching Test Circuit

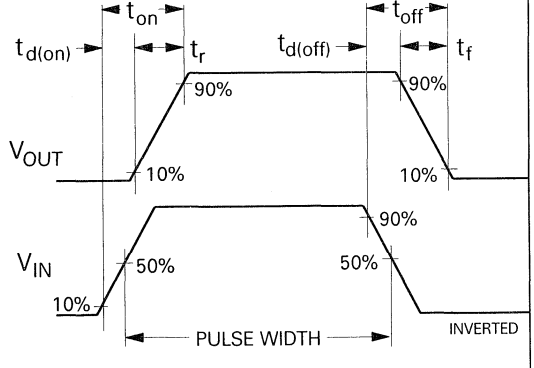


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

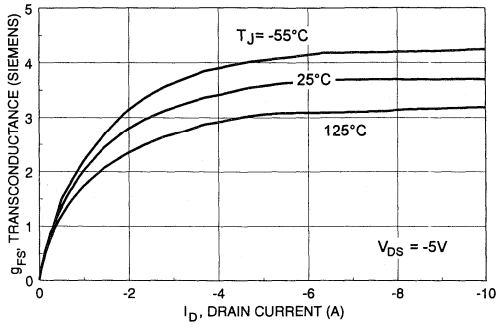


Figure 13. Transconductance Variation with Drain Current and Temperature

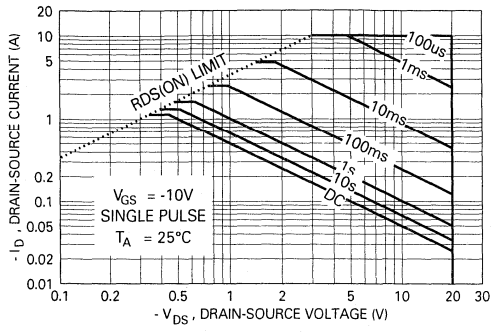


Figure 14. Maximum Safe Operating Area

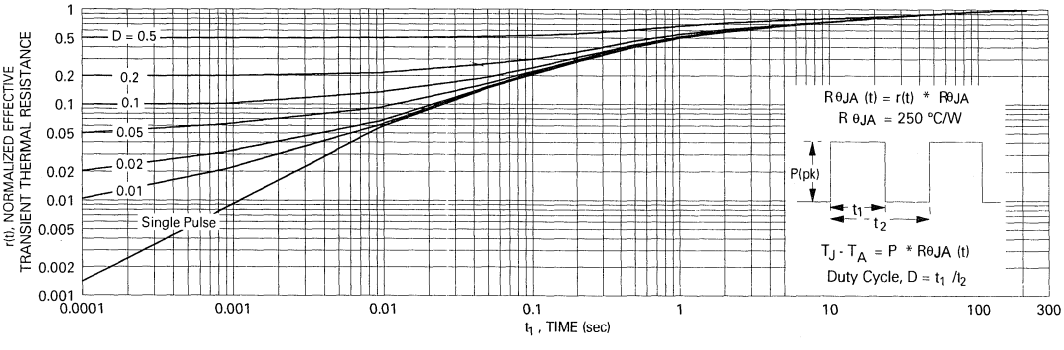


Figure 15. Transient Thermal Response Curve

Note : Characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

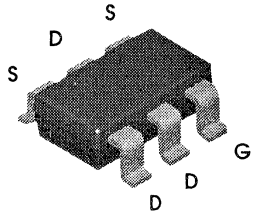
NDC631N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

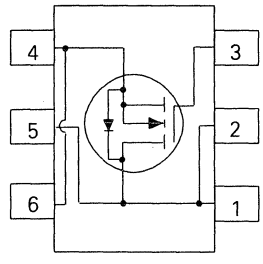
These N-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMICA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 4.1 A, 20 V. $R_{DS(ON)}$ = 0.06 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.075 Ω @ V_{GS} =2.7 V.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-6



Absolute Maximum Ratings

T_A = 25°C unless otherwise note

Symbol	Parameter		NDC631N	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage - Continuous		8	V
I_D	Drain Current - Continuous	(Note 1a)	4.1	A
	- Pulsed		15	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	1	
		(Note 1c)	0.8	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.7	1	V
		T_J = 125°C	0.3	0.5	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 4.1 A		0.039	0.06	Ω
		T_J = 125°C		0.06	0.11	
		V_{GS} = 2.7 V, I_D = 3.6 A		0.05	0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 4.5 V, I_D = 4.1 A		12		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		365		pF
C_{oss}	Output Capacitance			230		pF
C_{rss}	Reverse Transfer Capacitance			95		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω		9	17	ns
t_r	Turn - On Rise Time			25	45	ns
$t_{D(off)}$	Turn - Off Delay Time			28	50	ns
t_f	Turn - Off Fall Time			8	15	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 4.1 A, V_{GS} = 4.5 V		10	14	nC
Q_{gs}	Gate-Source Charge			1		nC
Q_{gd}	Gate-Drain Charge			3.3		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.75	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

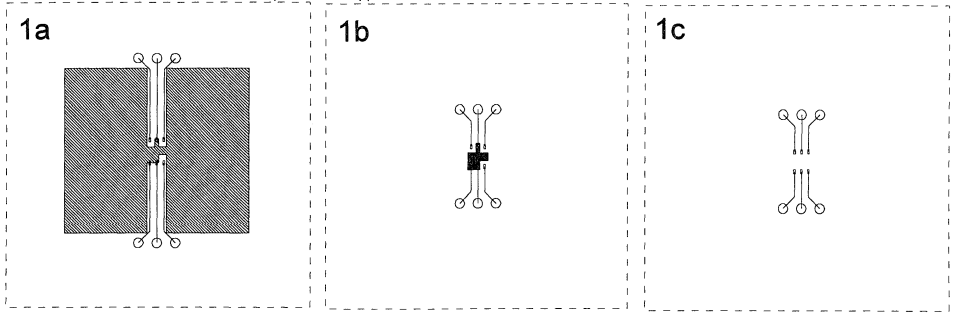
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.01 in^2 pad of 2oz copper.

c. 156°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

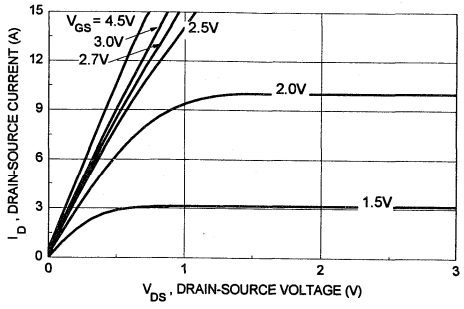


Figure 1. On-Region Characteristics

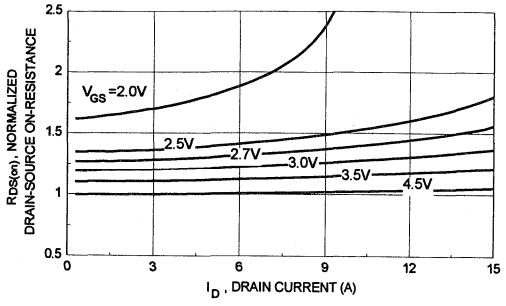


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

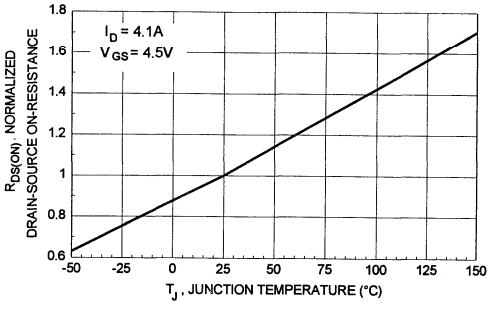


Figure 3. On-Resistance Variation with Temperature

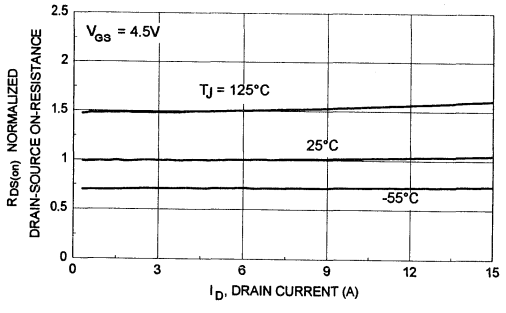


Figure 4. On-Resistance Variation with Drain Current and Temperature

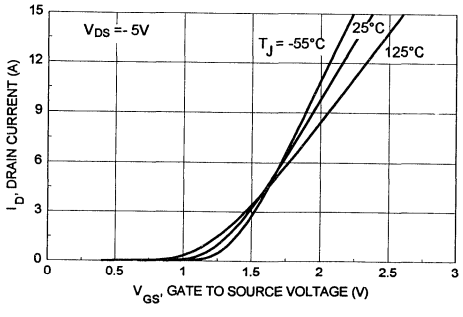


Figure 5. Transfer Characteristics

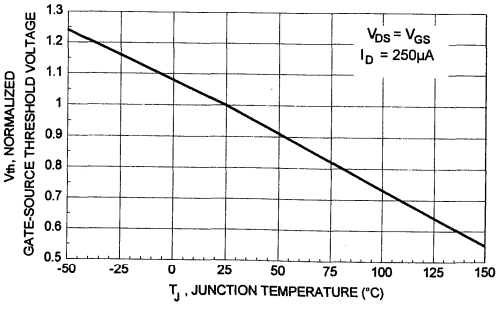


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

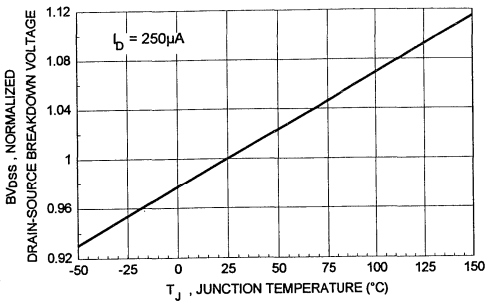


Figure 7. Breakdown Voltage Variation with Temperature

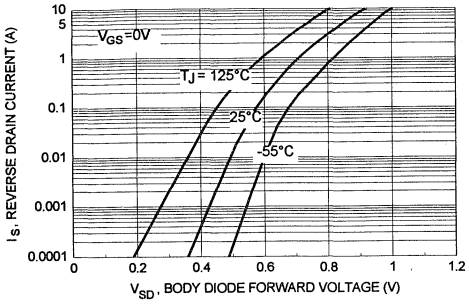


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

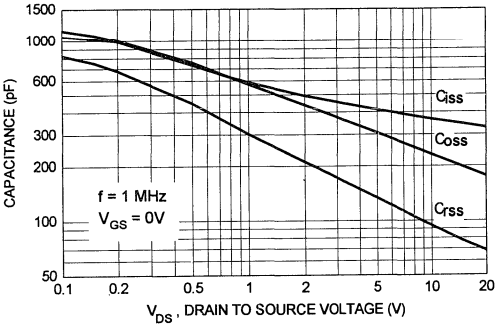


Figure 9. Capacitance Characteristics

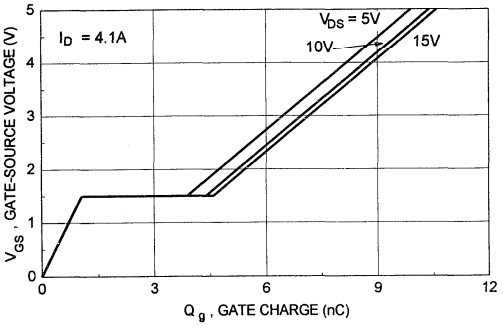


Figure 10. Gate Charge Characteristics

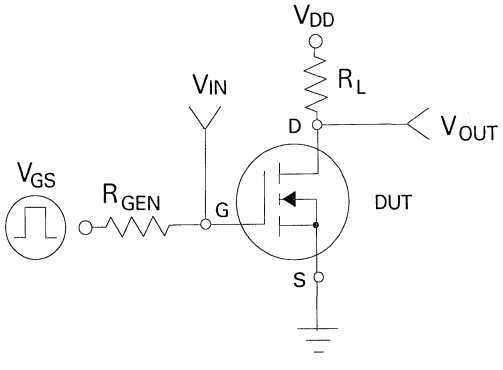


Figure 11. Switching Test Circuit

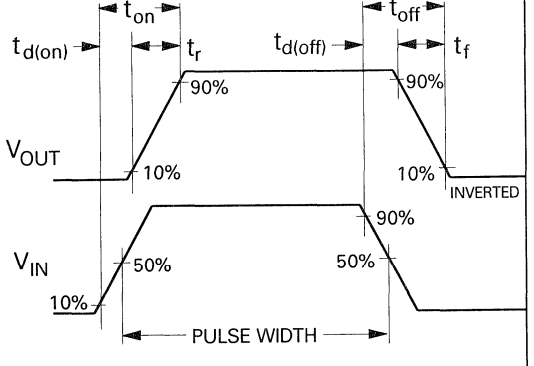


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

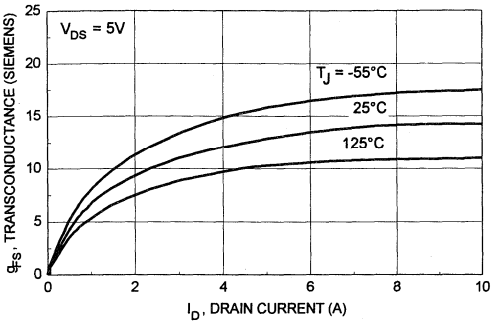


Figure 13. Transconductance Variation with Drain Current and Temperature

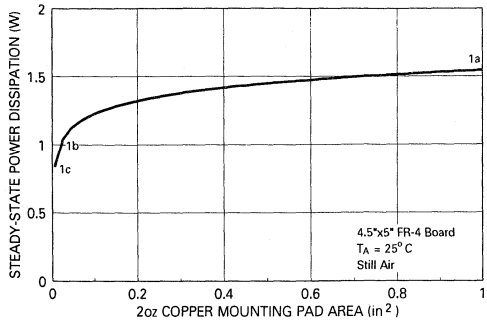


Figure 14. SuperSOT™-6 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

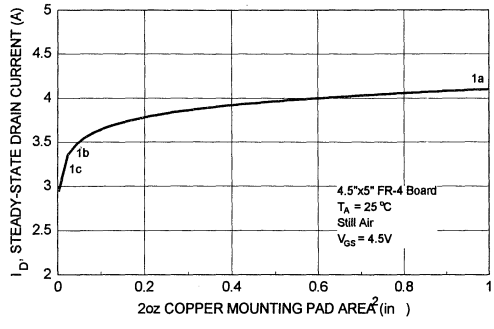


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

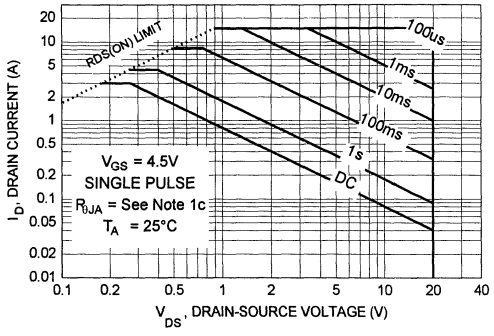


Figure 16. Maximum Safe Operating Area

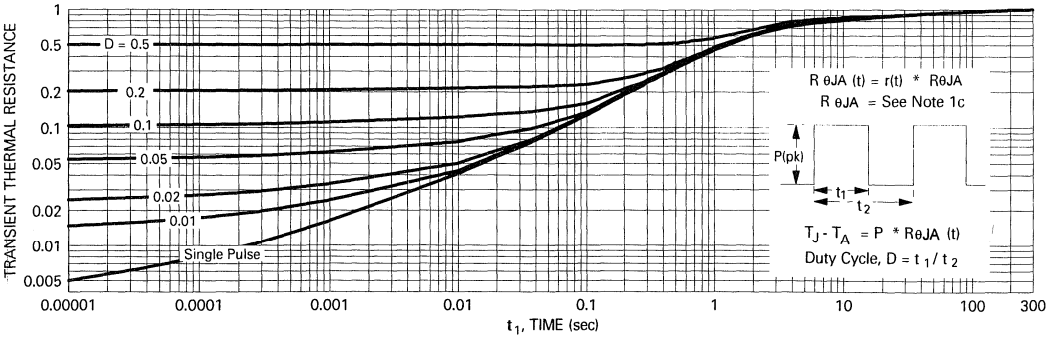


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

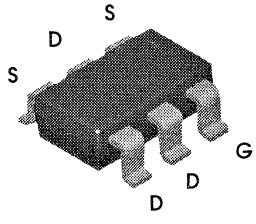
NDC632P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

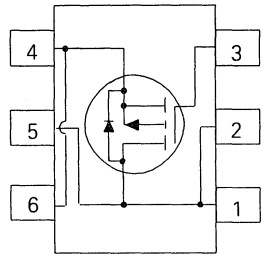
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -2.7A, -20V. $R_{DS(ON)}$ = 0.14Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.2Ω @ V_{GS} = -2.7V.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDC632P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		-8	V
I_D	Drain Current - Continuous		-2.7	A
	- Pulsed		-10	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	1	
		(Note 1c)	0.8	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.7	-1	V
		T_J = 125°C	-0.3	-0.5	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = - 2.7 A		0.1	0.14	Ω
		T_J = 125°C		0.145	0.28	
		V_{GS} = -2.7 V, I_D = - 2.2 A		0.152	0.2	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-10			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-4			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = - 2.7 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		550		pF
C_{oss}	Output Capacitance			260		pF
C_{rss}	Reverse Transfer Capacitance			75		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn - On Rise Time			40	60	ns
$t_{D(off)}$	Turn - Off Delay Time			25	40	ns
t_f	Turn - Off Fall Time			17	30	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -2.7 A, V_{GS} = -4.5 V		8.7	15	nC
Q_{gs}	Gate-Source Charge			1.7		nC
Q_{gd}	Gate-Drain Charge			1.8		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)		-0.77	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

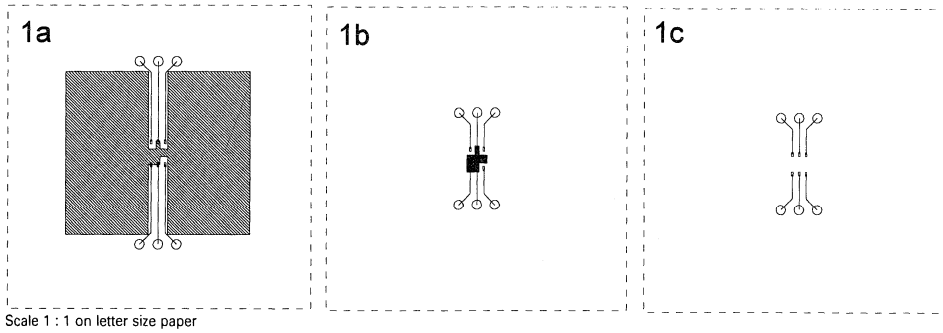
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.01 in^2 pad of 2oz copper.

c. 156°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

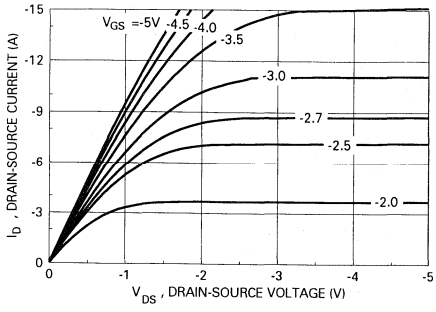


Figure 1. On-Region Characteristics

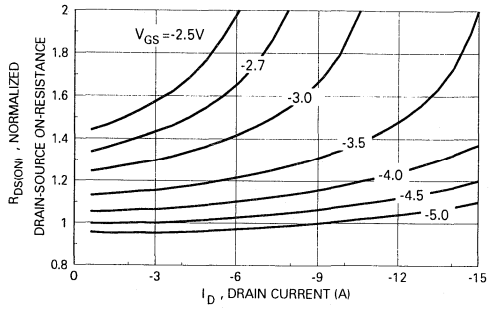


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

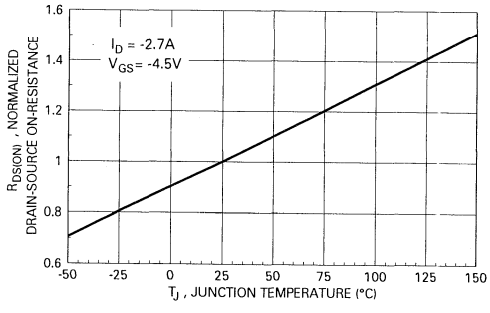


Figure 3. On-Resistance Variation with Temperature

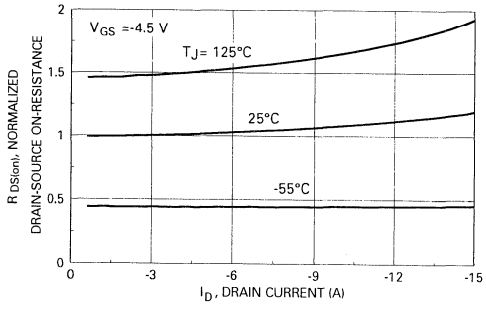


Figure 4. On-Resistance Variation with Drain Current and Temperature

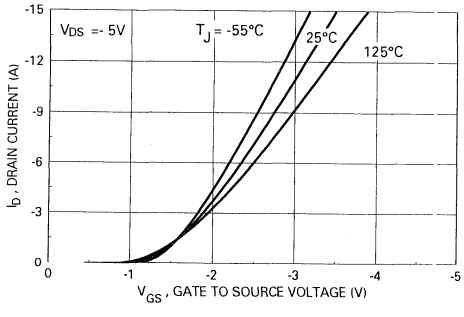


Figure 5. Transfer Characteristics

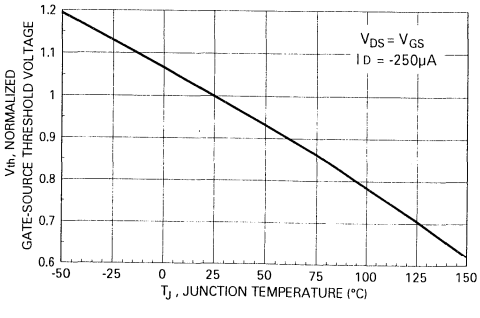


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

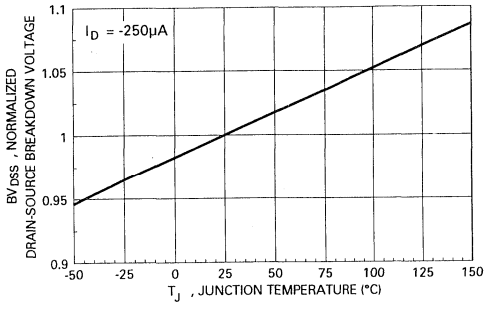


Figure 7. Breakdown Voltage Variation with Temperature

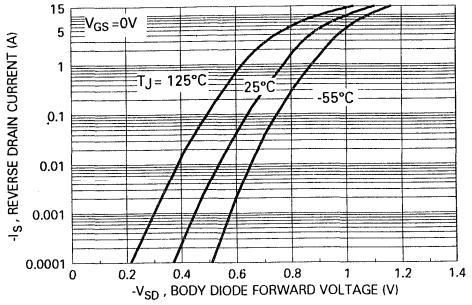


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

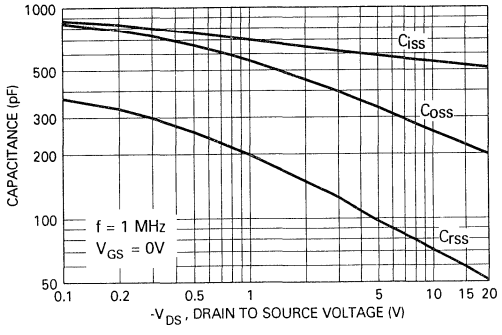


Figure 9. Capacitance Characteristics

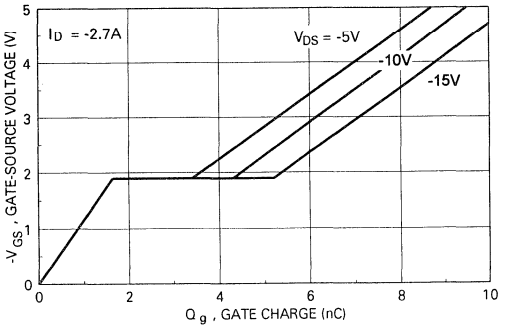


Figure 10. Gate Charge Characteristics

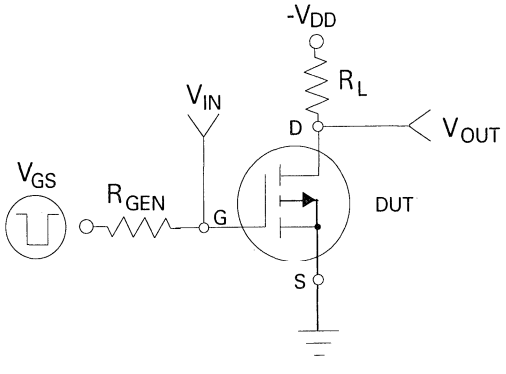


Figure 11. Switching Test Circuit

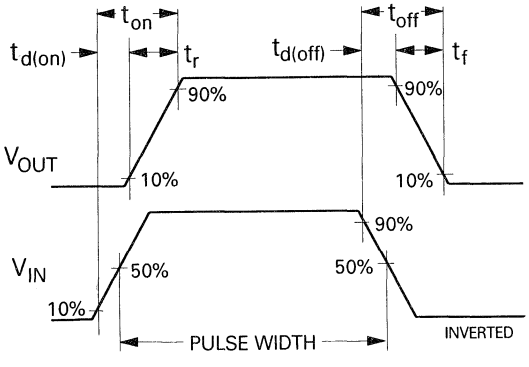


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

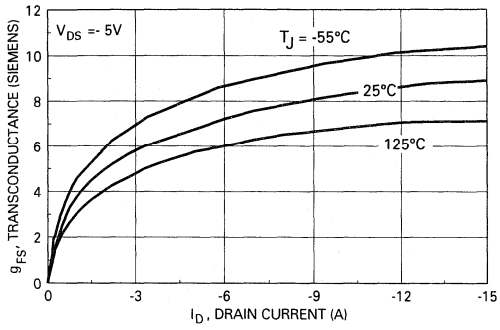


Figure 13. Transconductance Variation with Drain Current and Temperature

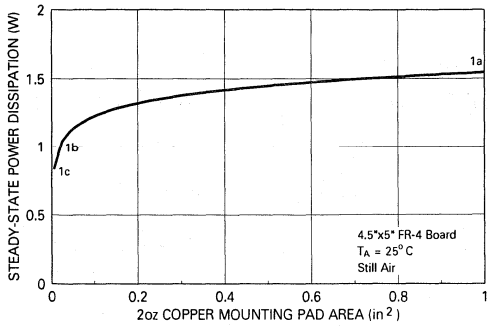


Figure 14. SuperSOT™-6 Maximum Steady-State Power Dissipation versus Copper Mounting Pad

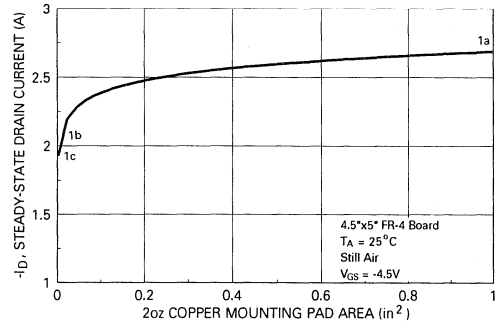


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

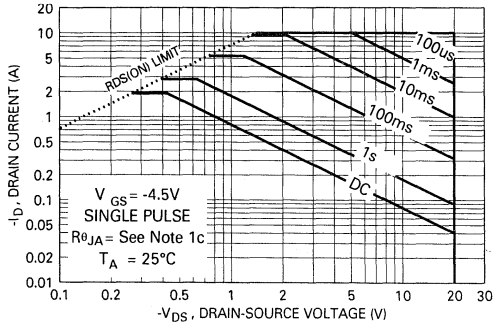


Figure 16. Maximum Safe Operating

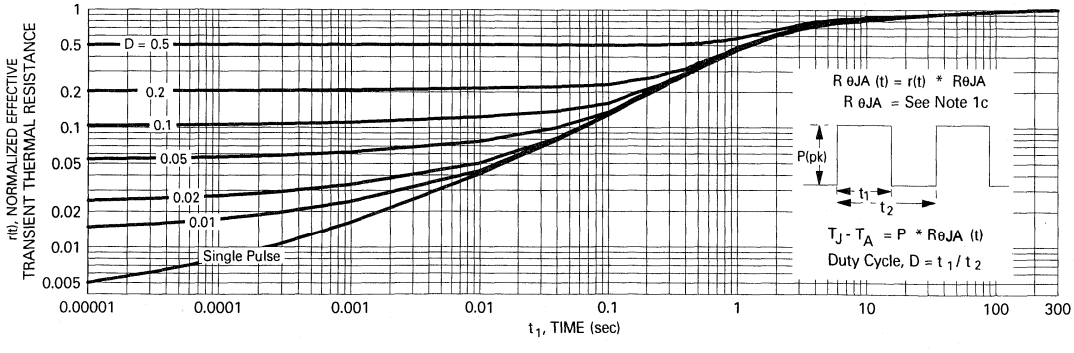


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

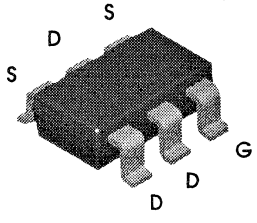
NDC651N
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

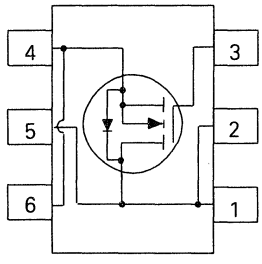
These N-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMICA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 3.2A, 30V. $R_{DS(ON)}$ = 0.09Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.06Ω @ V_{GS} = 10V.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise note

Symbol	Parameter		NDC651N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage - Continuous		20	V
I_D	Drain Current - Continuous	(Note 1a)	3.2	A
	- Pulsed		15	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	1	
		(Note 1c)	0.8	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.7	3	V
		T_J = 125°C	0.7	1.3	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 3.2 A		0.068	0.09	Ω
		T_J = 125°C		0.095	0.18	
		V_{GS} = 10 V, I_D = 4 A		0.042	0.06	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.2 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		290		pF
C_{oss}	Output Capacitance			180		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω		9	20	ns
t_r	Turn - On Rise Time			19	30	ns
$t_{D(off)}$	Turn - Off Delay Time			15	30	ns
t_f	Turn - Off Fall Time			7	20	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 3.2 A, V_{GS} = 10 V		10	20	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			2.6		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

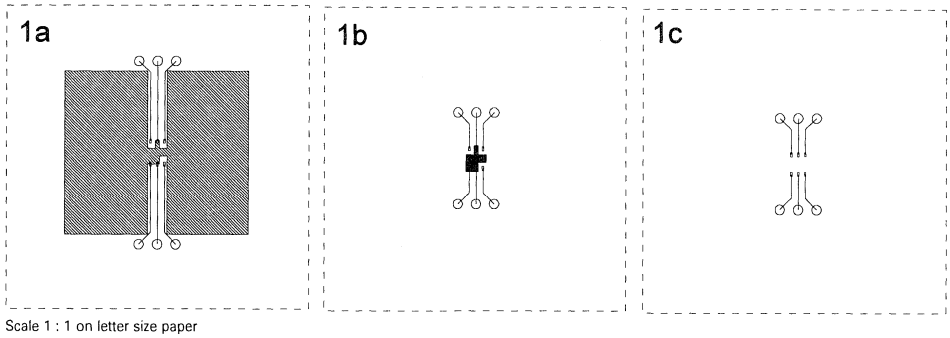
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.01 in^2 pad of 2oz copper.

c. 156°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

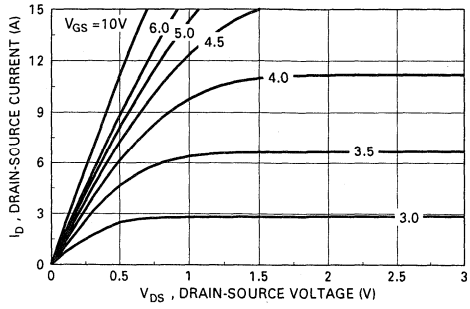


Figure 1. On-Region Characteristics

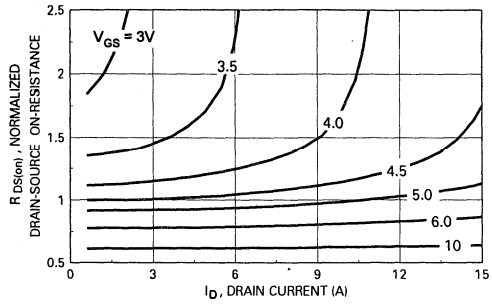


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

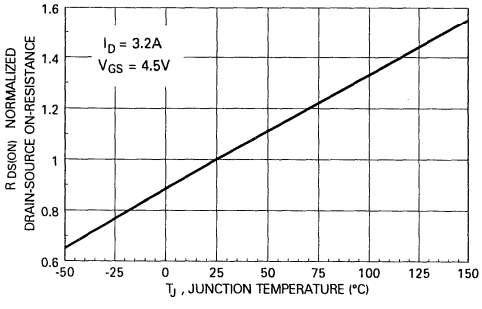


Figure 3. On-Resistance Variation with Temperature

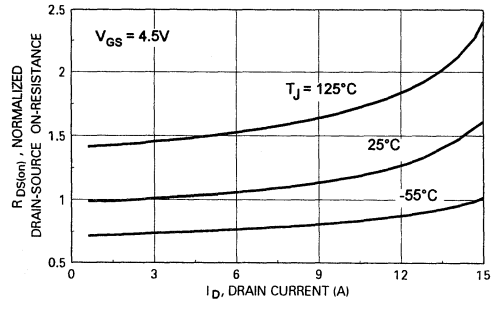


Figure 4. On-Resistance Variation with Drain Current and Temperature

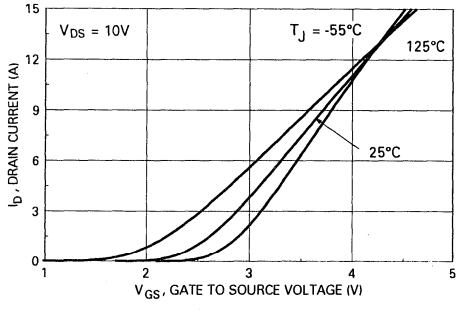


Figure 5. Transfer Characteristics

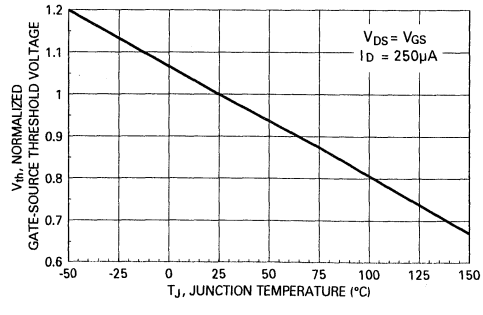


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

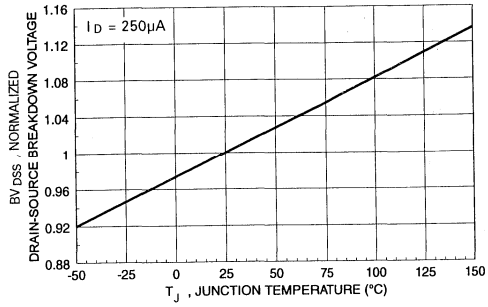


Figure 7. Breakdown Voltage Variation with Temperature

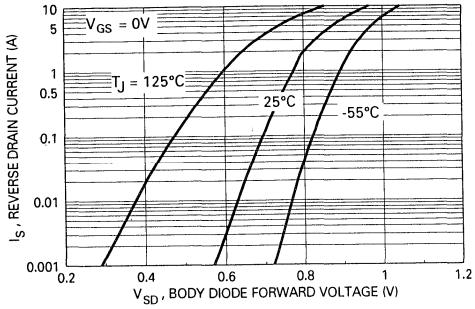


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

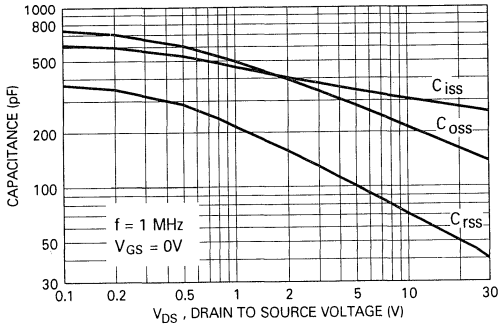


Figure 9. Capacitance Characteristics

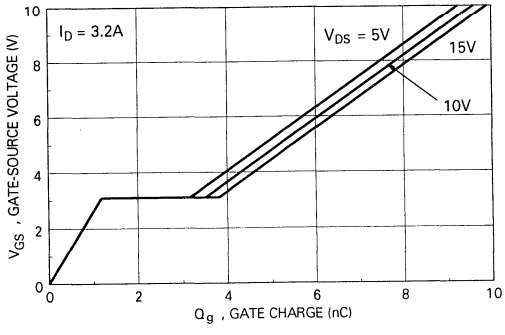


Figure 10. Gate Charge Characteristics

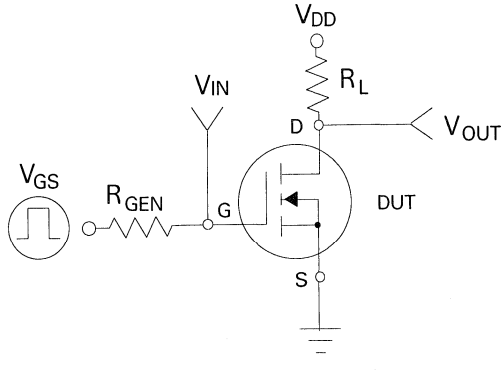


Figure 11. Switching Test Circuit

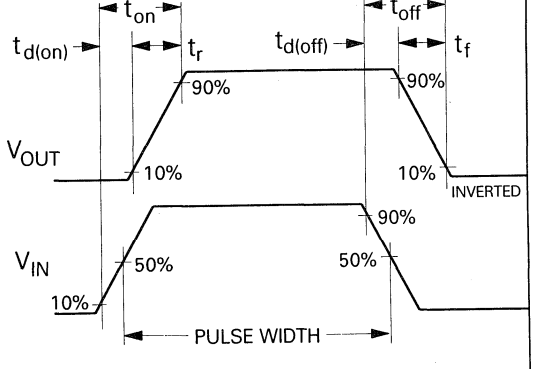


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

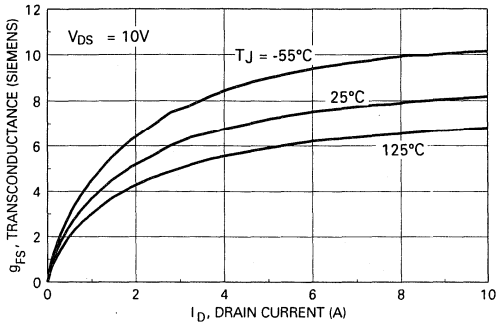


Figure 13. Transconductance Variation with Drain Current and Temperature

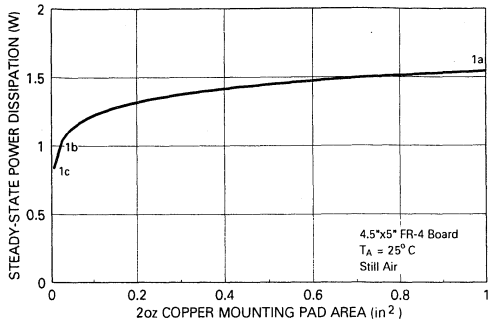


Figure 14. SuperSOT™-6 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

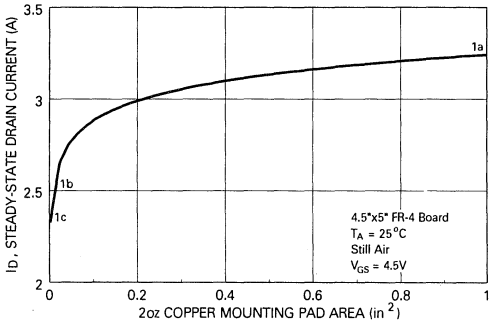


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

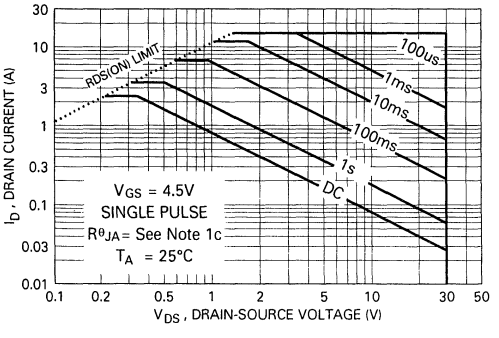


Figure 16. Maximum Safe Operating Area

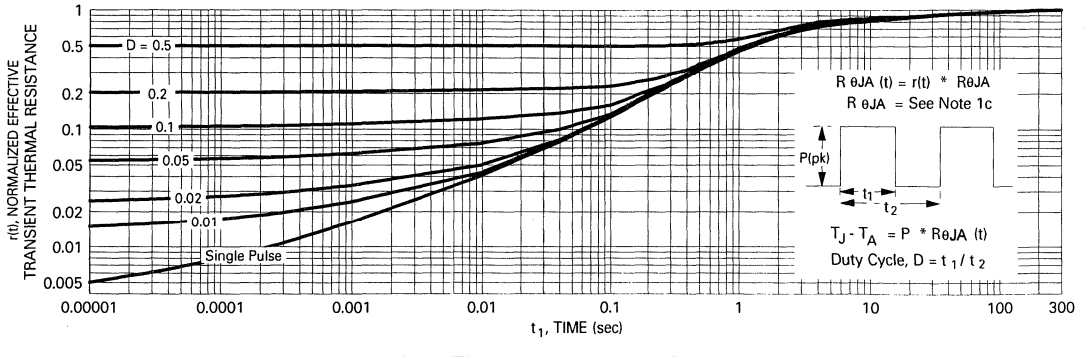


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

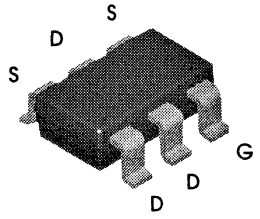
NDC652P
P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

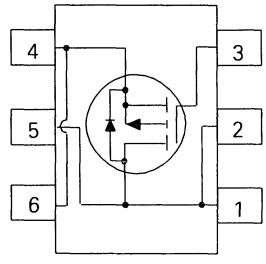
These P-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -2.4A, -30V. $R_{DS(ON)}$ = 0.18Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.11Ω @ V_{GS} = -10V.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDC652P	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage - Continuous		-20	V
I_D	Drain Current - Continuous		-2.4	A
	- Pulsed		-10	
P_D	Maximum Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	1	
		(Note 1c)	0.8	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	30	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.5	-3	V
		T_J = 125°C	-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -2.4 A		0.16	0.18	Ω
		T_J = 125°C		0.22	0.36	
		V_{GS} = -10 V, I_D = -3.1 A		0.09	0.11	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-5			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2.4 A		3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		290		pF
C_{oss}	Output Capacitance			180		pF
C_{rss}	Reverse Transfer Capacitance			60		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω		13	20	ns
t_r	Turn - On Rise Time			26	35	ns
$t_{D(off)}$	Turn - Off Delay Time			22	30	ns
t_f	Turn - Off Fall Time			19	30	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -2.4 A, V_{GS} = -10 V		10.5	20	nC
Q_{gs}	Gate-Source Charge			1.5		nC
Q_{gd}	Gate-Drain Charge			3.3		nC

3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

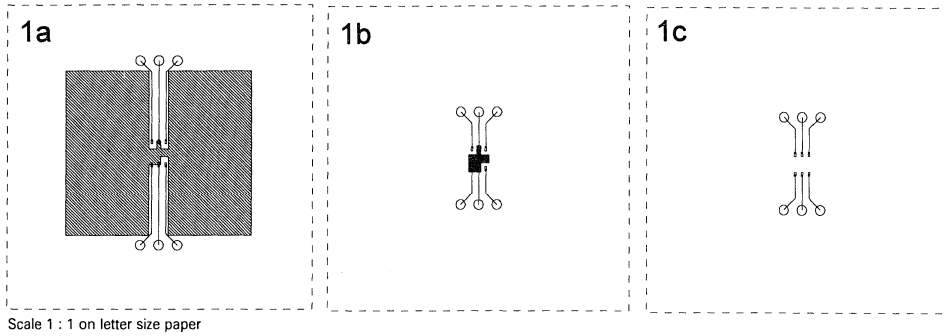
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.01 in^2 pad of 2oz copper.

c. 156°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

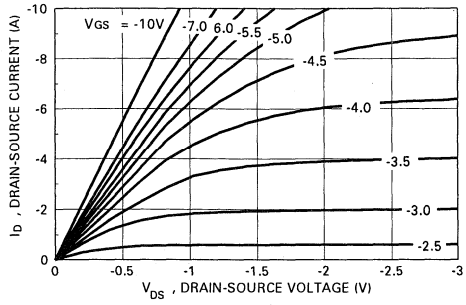


Figure 1. On-Region Characteristics

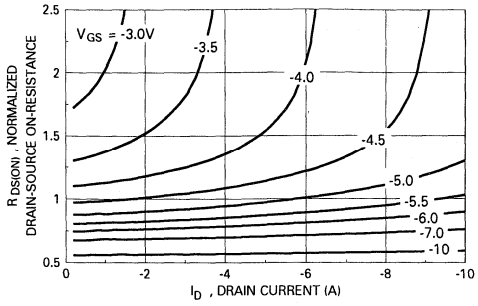


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

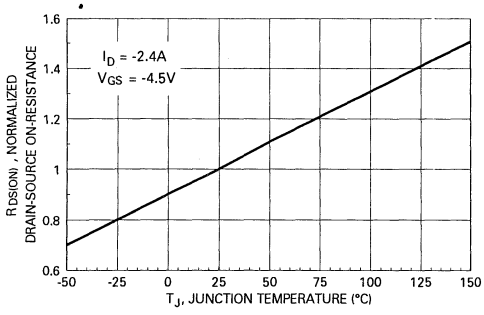


Figure 3. On-Resistance Variation with Temperature

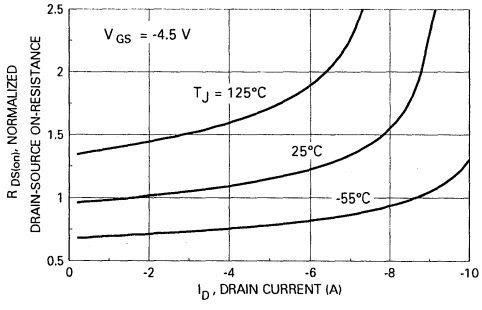


Figure 4. On-Resistance Variation with Drain Current and Temperature

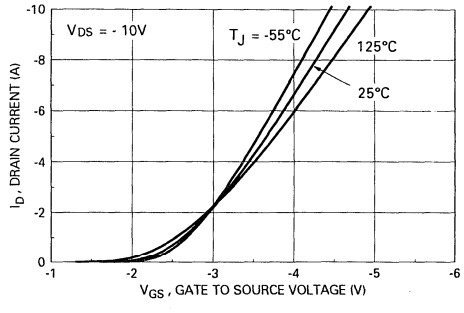


Figure 5. Transfer Characteristics

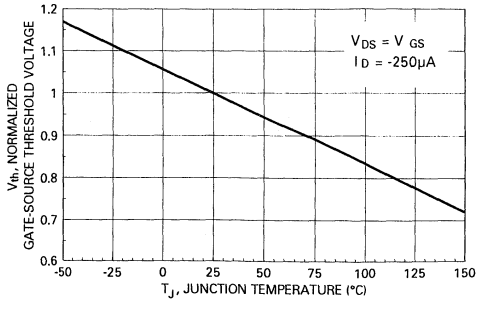


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

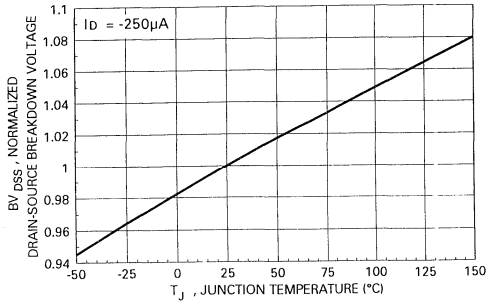


Figure 7. Breakdown Voltage Variation with Temperature

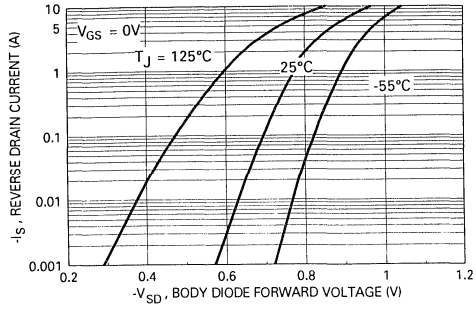


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

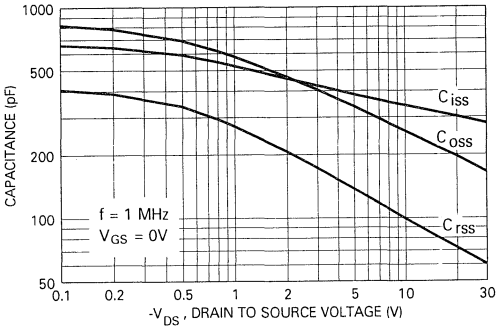


Figure 9. Capacitance Characteristics

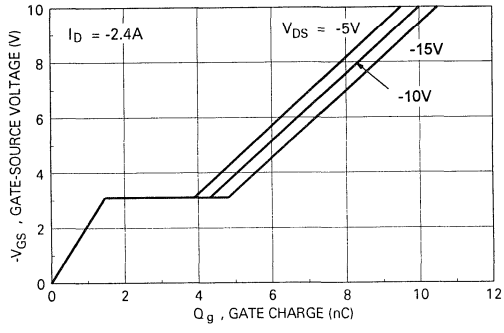


Figure 10. Gate Charge Characteristics

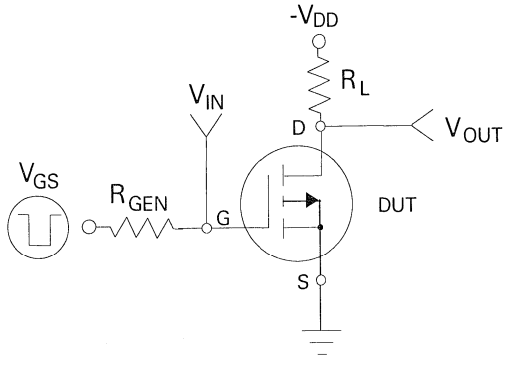


Figure 11. Switching Test Circuit

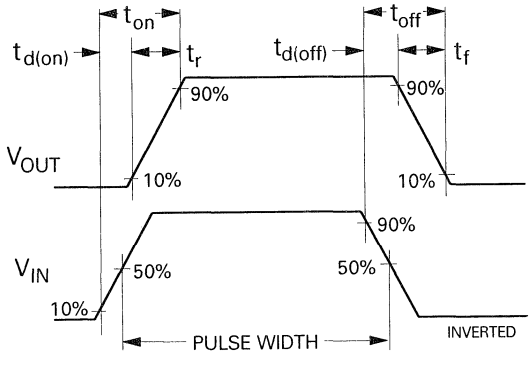


Figure 12. Switching Waveforms

Typical Electrical and ThermalCharacteristics (continued)

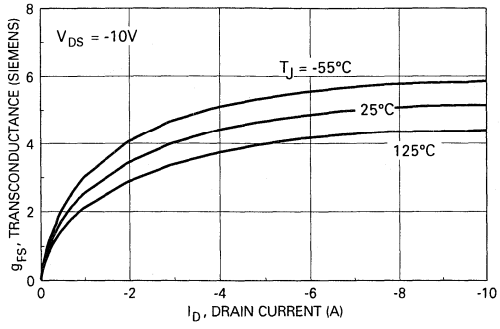


Figure 13. Transconductance Variation with Drain Current and Temperature

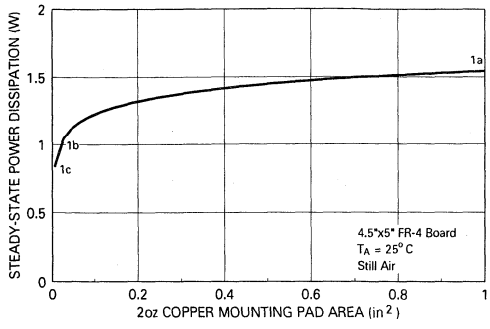


Figure 14. SuperSOT™-6 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

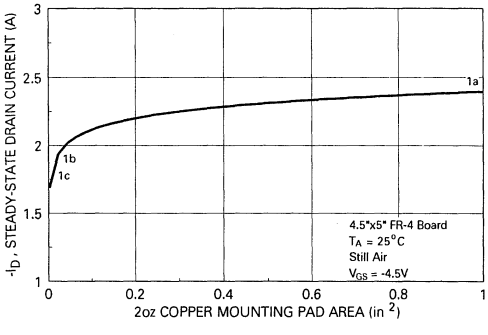


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

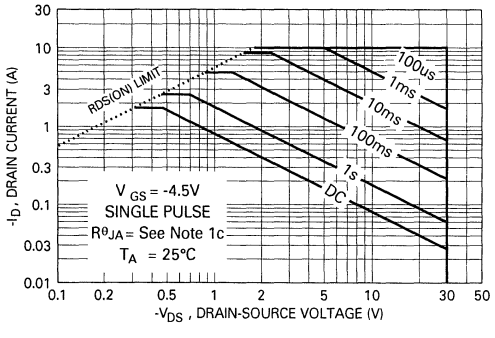


Figure 16. Maximum Safe Operating Area

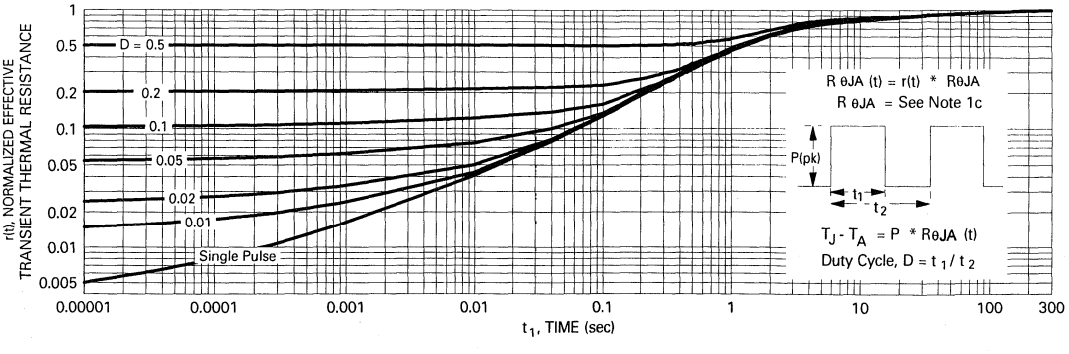


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

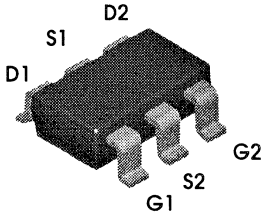
NDC7001C
Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

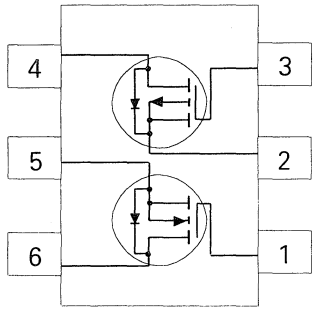
These dual N and P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage, low current, switching, and power supply applications.

Features

- N-Channel 0.51A, 50V, $R_{DS(ON)}$ = 2Ω @ V_{GS}=10V
- P-Channel -0.34A, -50V. $R_{DS(ON)}$= 5Ω @ V_{GS}=-10V.
- High density cell design for low $R_{DS(ON)}$.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		50	-50	V
V_{GSS}	Gate-Source Voltage - Continuous		20	-20	V
I_D	Drain Current - Continuous	(Note 1a)	0.51	-0.34	A
	- Pulsed		1.5	-1	
P_D	Maximum Power Dissipation	(Note 1a)	0.96		W
		(Note 1b)	0.9		
		(Note 1c)	0.7		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60		°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	50			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-50			
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 125°C				500	
		V_{DS} = -40 V, V_{GS} = 0 V	P-Ch			-1	
		T_J = 125°C				-500	
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.9	2.5	V
		T_J = 125°C		0.8	1.5	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2.5	-3.5	
		T_J = 125°C		-0.8	-2.2	-3	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.51 A	N-Ch		1	2	Ω
		T_J = 125°C			1.7	3.5	
		V_{GS} = 4.5 V, I_D = 0.35 A			1.6	4	
		V_{GS} = -10 V, I_D = -0.34 A	P-Ch		2.5	5	
		T_J = 125°C			4	10	
		V_{GS} = -4.5 V, I_D = -0.25 A			5.3	7.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	N-Ch	1.5			A
		V_{GS} = -10 V, V_{DS} = -10 V	P-Ch	-1			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.51 A	N-Ch		400		mS
		V_{DS} = -10 V, I_D = -0.34 A	P-Ch		250		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		20		pF
			P-Ch		40		
C_{oss}	Output Capacitance	P-Channel V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		13		pF
			P-Ch		13		
C_{rss}	Reverse Transfer Capacitance		N-Ch		5		pF
			P-Ch		4		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameters	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 25 V, I_D = 0.25 A, V_{GS} = 10 V, R_{GEN} = 25 Ω	N-Ch		6	20	nS
			P-Ch		14	20	
t_r	Turn - On Rise Time		N-Ch		6	20	
			P-Ch		6	20	
$t_{D(off)}$	Turn - Off Delay Time	P-Channel V_{DD} = -25 V, I_D = -0.25 A, V_{GS} = -10 V, R_{GEN} = 25 Ω	N-Ch		11	20	
			P-Ch		13	20	
t_f	Turn - Off Fall Time		N-Ch		5	20	
			P-Ch		6	20	
Q_g	Total Gate Charge	N-Channel V_{DS} = 25 V, I_D = 0.51 A, V_{GS} = 10 V	N-Ch		1		nC
			P-Ch		1.3		
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -25 V, I_D = -0.34 A, V_{GS} = -10 V	N-Ch		0.19		nC
			P-Ch		0.23		
Q_{gd}	Gate-Drain Charge		N-Ch		0.33		nC
			P-Ch		0.38		
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuous Source Current		N-Ch			0.51	A
			P-Ch			-0.34	
I_{SM}	Maximum Pulse Source Current (Note 2)		N-Ch			1.5	A
			P-Ch			-1	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.51 A (Note 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -0.34 A (Note 2)	P-Ch		-0.8	-1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

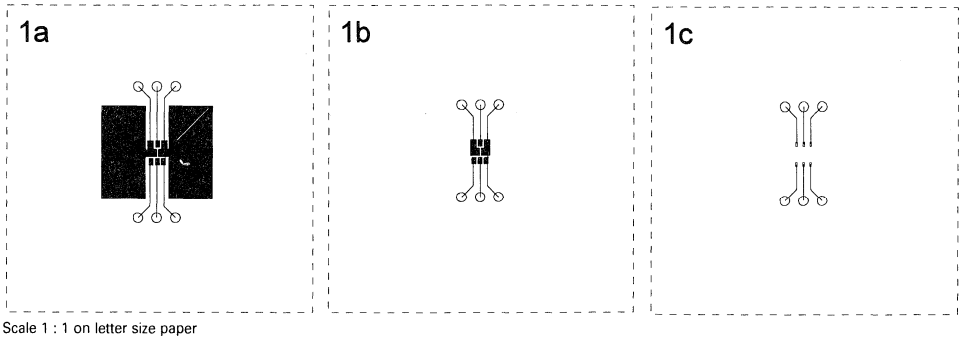
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 130°C/W when mounted on a 0.125 in^2 pad of 2oz copper.

b. 140°C/W when mounted on a 0.005 in^2 pad of 2oz copper.

c. 180°C/W when mounted on a 0.0015 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

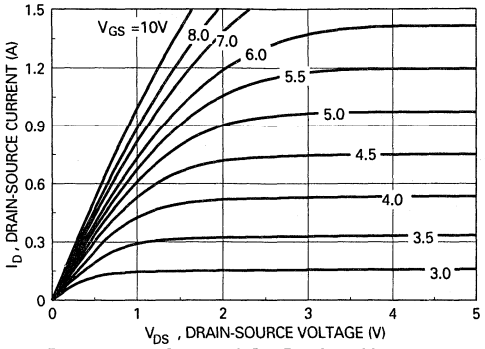


Figure 1. N-Channel On-Region Characteristics.

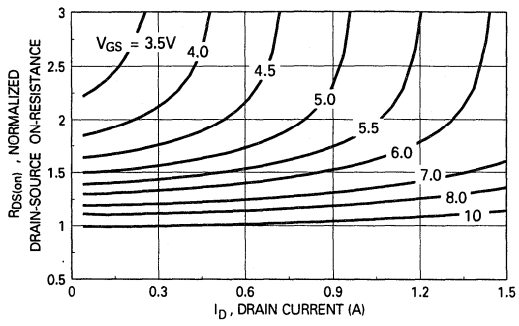


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

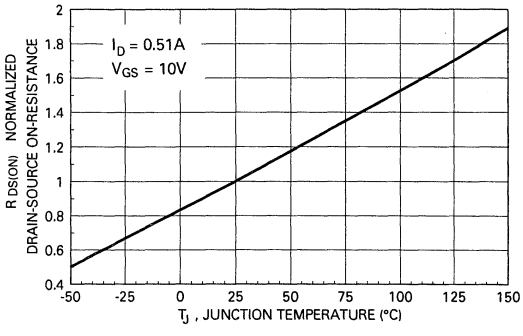


Figure 3. N-Channel On-Resistance Variation with Temperature.

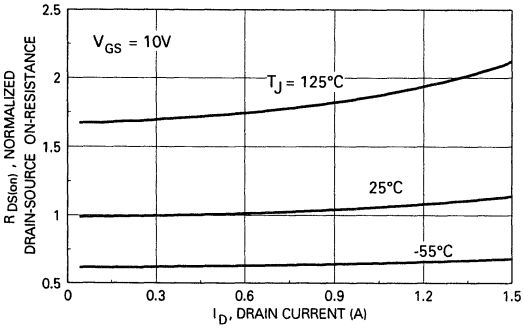


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

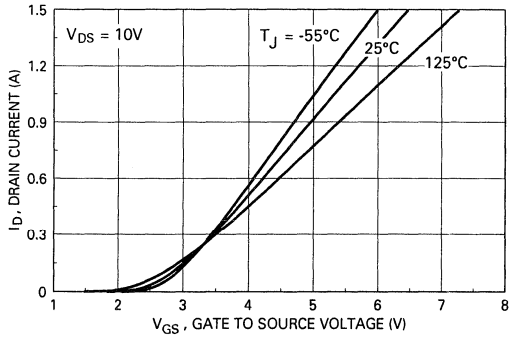


Figure 5. N-Channel Transfer Characteristics.

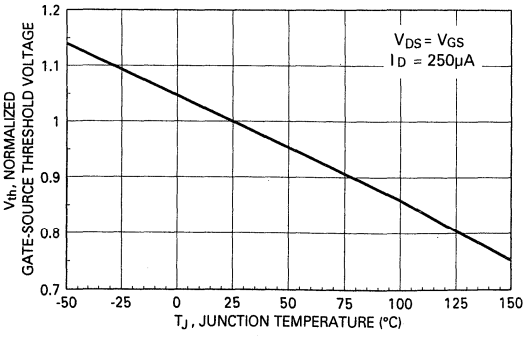


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

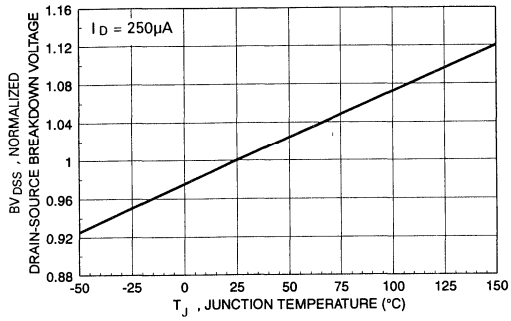


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

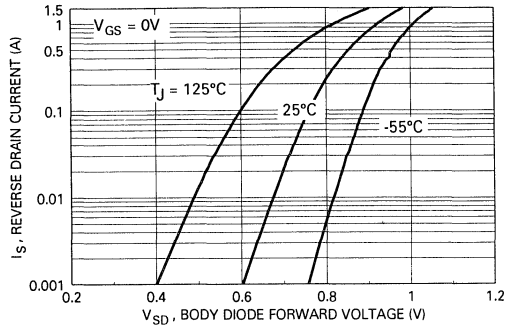


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

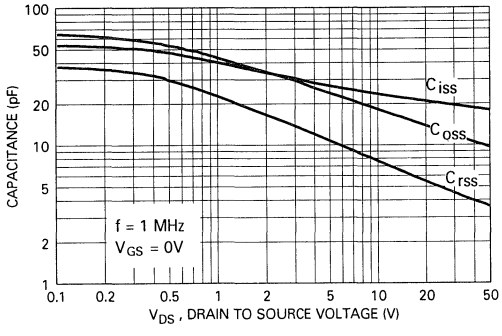


Figure 9. N-Channel Capacitance Characteristics.

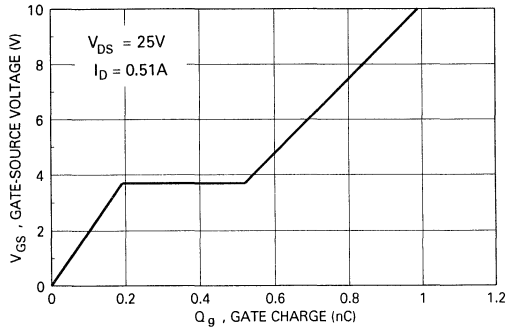


Figure 10. N-Channel Gate Charge Characteristics.

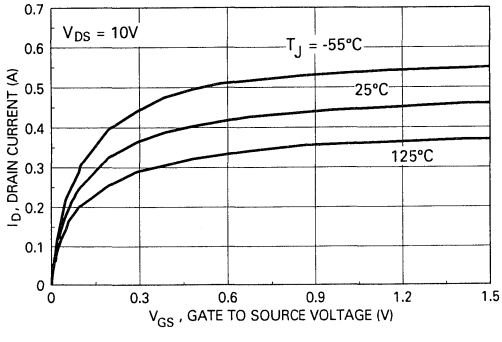


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

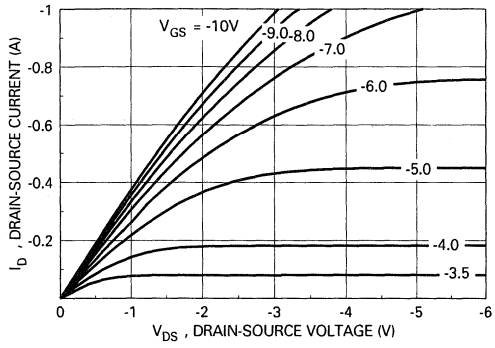


Figure 12. P-Channel On-Region Characteristics.

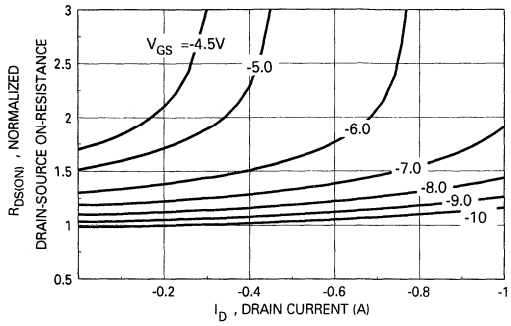


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

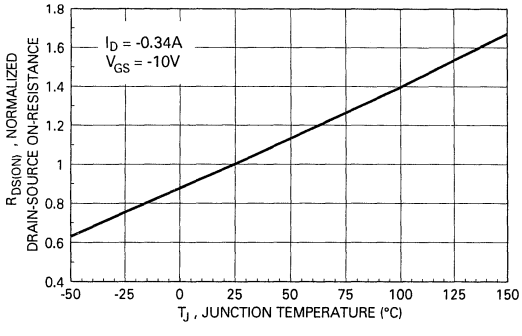


Figure 14. P-Channel On-Resistance Variation with Temperature.

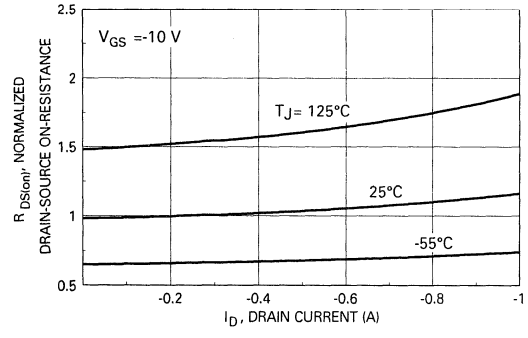


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

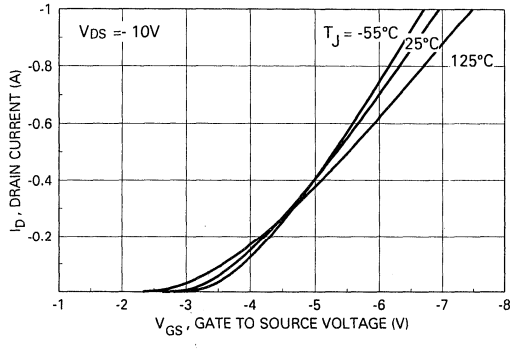


Figure 16. P-Channel Transfer Characteristics.

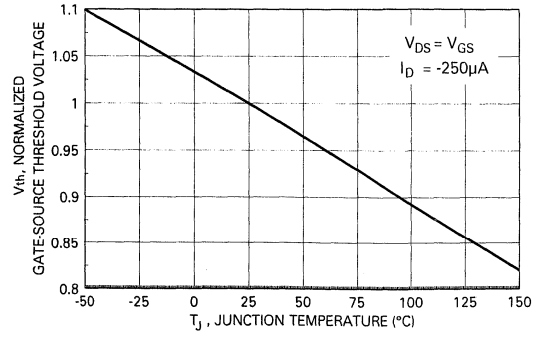


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

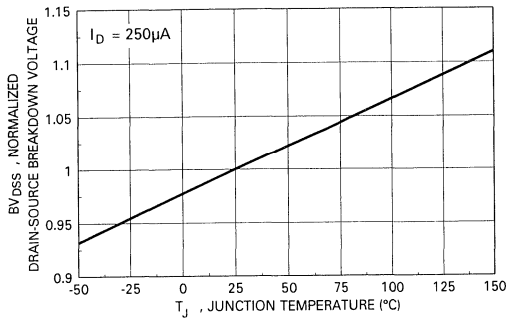


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

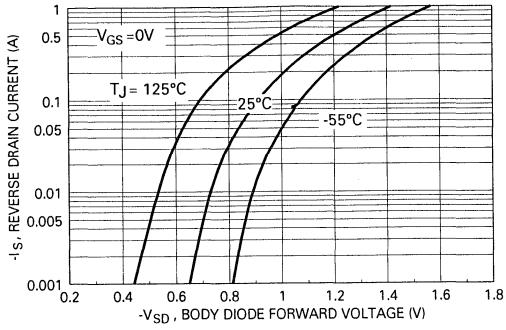


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

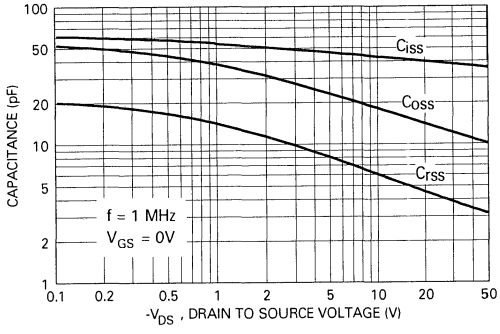


Figure 20. P-Channel Capacitance Characteristics.

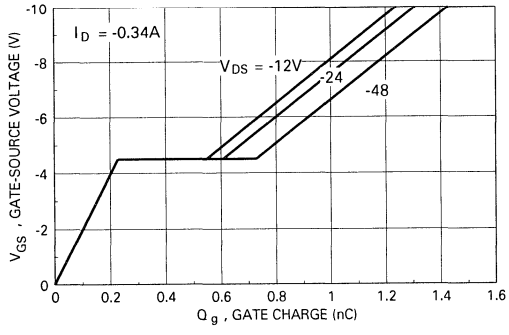


Figure 21. P-Channel Gate Charge Characteristics.

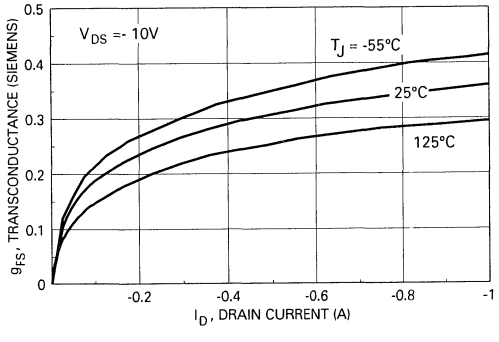


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

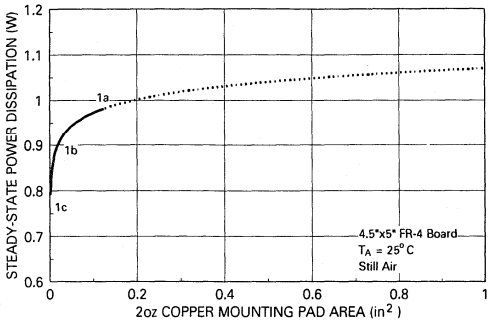


Figure 23. SuperSOT™-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

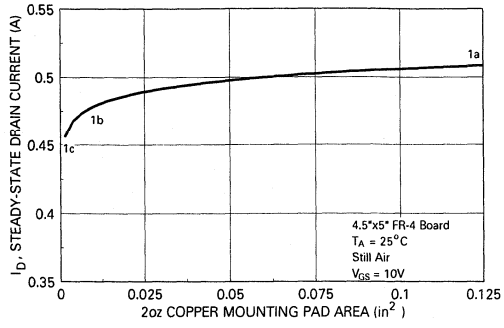


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

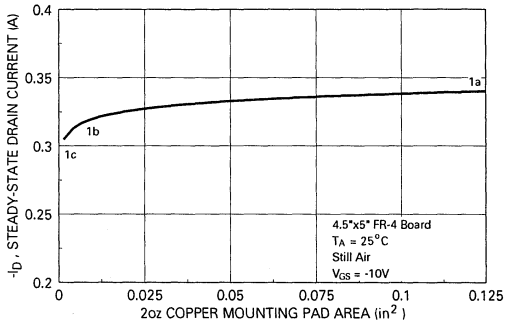


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

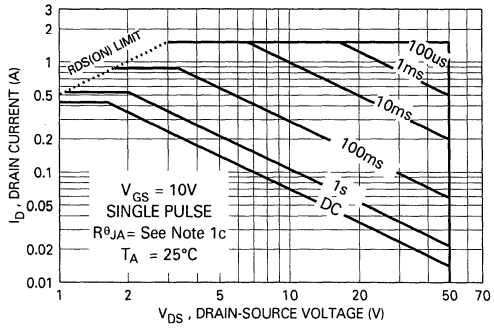


Figure 26. N-Channel Maximum Safe Operating Area.

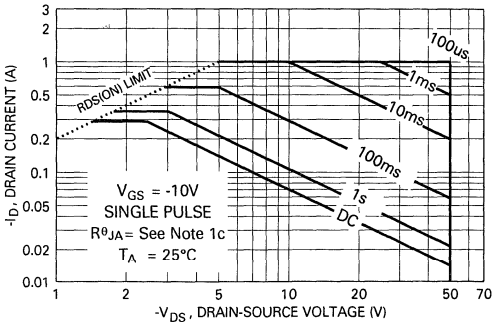


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

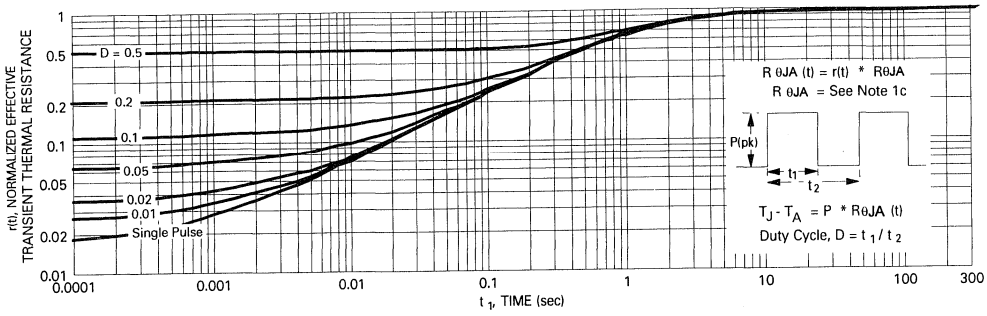


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

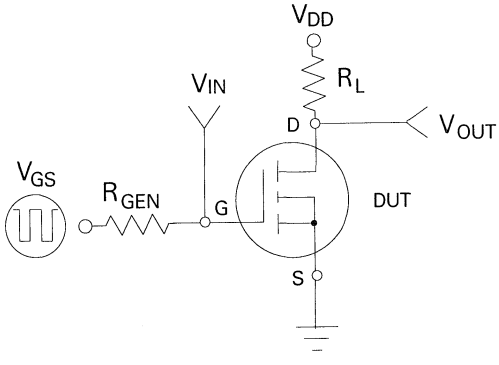


Figure 29. N or P-Channel Switching Test Circuit.

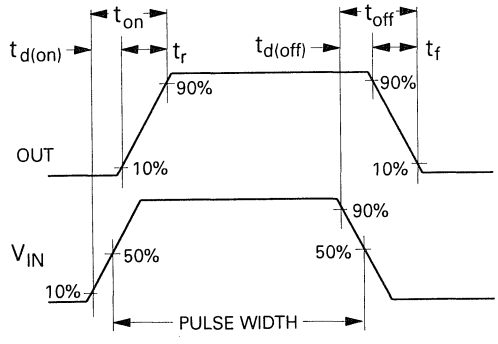


Figure 30. N or P-Channel Switching Waveforms.

National Semiconductor™

March 1996

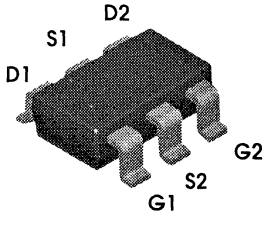
NDC7002N
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

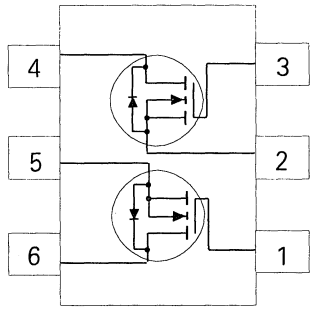
These dual N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. These devices is particularly suited for low voltage applications requiring a low current high side switch.

Features

- 0.51A, 50V, $R_{DS(ON)}$ = 2Ω @ V_{GS}=10V
- High density cell design for low $R_{DS(ON)}$.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High saturation current.



SuperSOT™-6



3

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDC7002N	Units
V_{DSS}	Drain-Source Voltage		50	V
V_{GSS}	Gate-Source Voltage - Continuous		20	V
I_D	Drain Current - Continuous	(Note 1a)	0.51	A
	- Pulsed		1.5	
P_D	Maximum Power Dissipation	(Note 1a)	0.96	W
		(Note 1b)	0.9	
		(Note 1c)	0.7	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			500	
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.9	2.5	V
		T_J = 125°C	0.8	1.5	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.51 A		1	2	Ω
		T_J = 125°C		1.7	3.5	
		V_{GS} = 4.5 V, I_D = 0.35 A		1.6	4	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	1.5			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.51 A		400		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		20		pF
C_{oss}	Output Capacitance			13		pF
C_{rss}	Reverse Transfer Capacitance			5		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 0.25 A, V_{GS} = 10 V, R_{GEN} = 25 Ω		6	20	nS
t_r	Turn - On Rise Time			6	20	
$t_{D(off)}$	Turn - Off Delay Time			11	20	
t_f	Turn - Off Fall Time			5	20	
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 0.51 A, V_{GS} = 10 V		1		nC
Q_{gs}	Gate-Source Charge			0.19		nC
Q_{gd}	Gate-Drain Charge			0.33		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source Current				0.51	A
I_{SM}	Maximum Pulse Source Current (Note 2)				1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.51 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

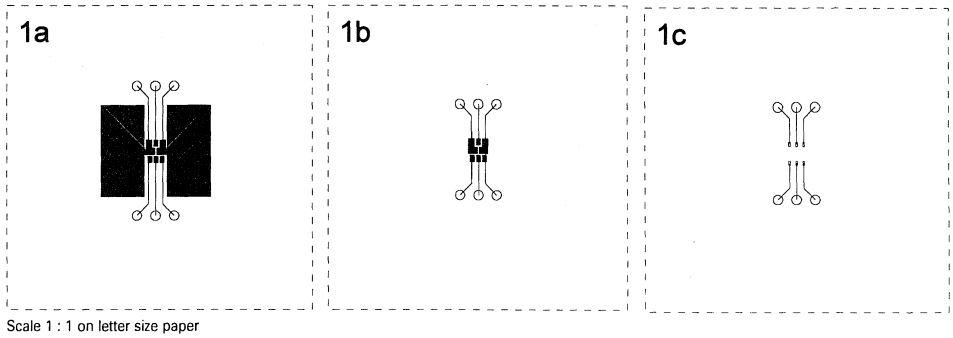
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 130°C/W when mounted on a 0.125 in^2 pad of 2oz copper.

b. 140°C/W when mounted on a 0.005 in^2 pad of 2oz copper.

c. 180°C/W when mounted on a 0.0015 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

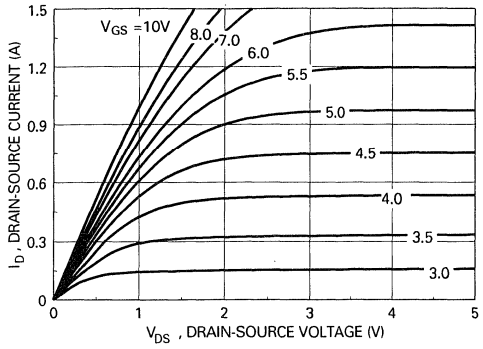


Figure 1. On-Region Characteristics.

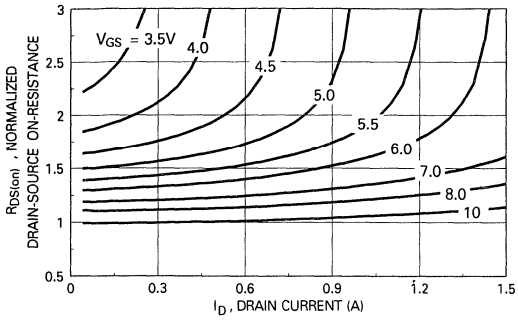


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

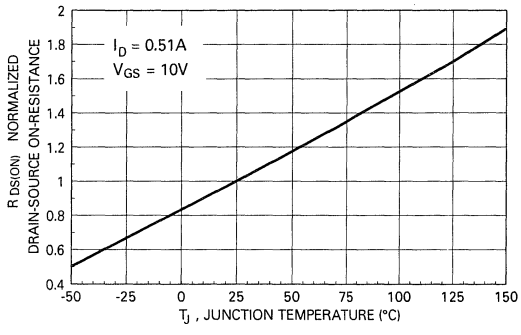


Figure 3. On-Resistance Variation with Temperature.

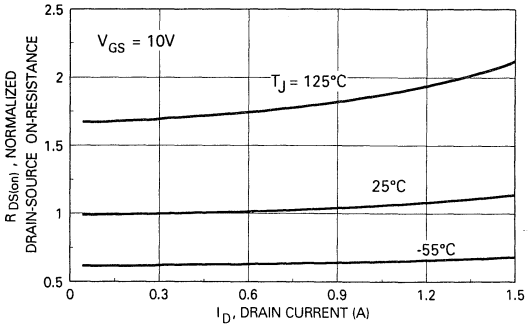


Figure 4. On-Resistance Variation with Drain Current and Temperature.

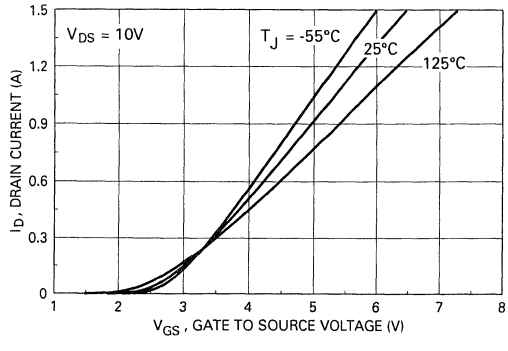


Figure 5. Transfer Characteristics.

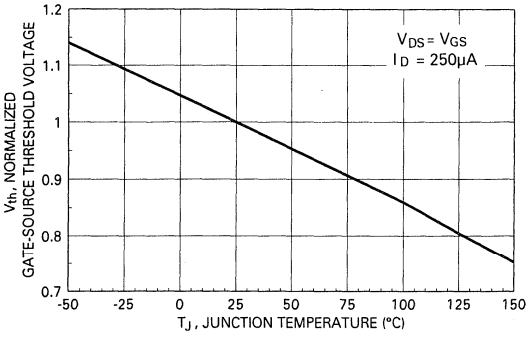


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

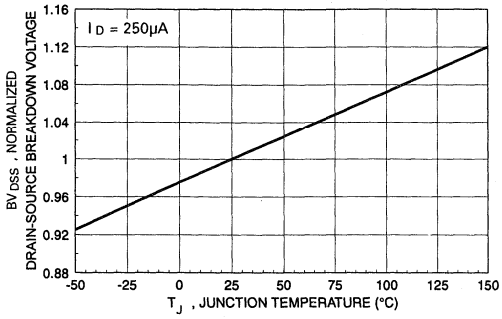


Figure 7. Breakdown Voltage Variation with Temperature.

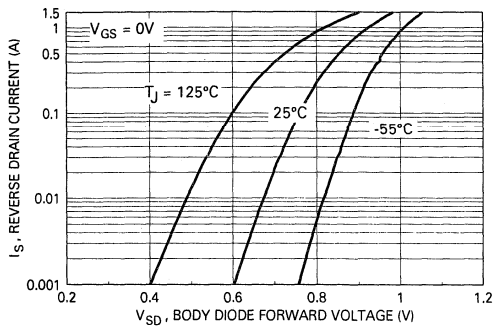


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

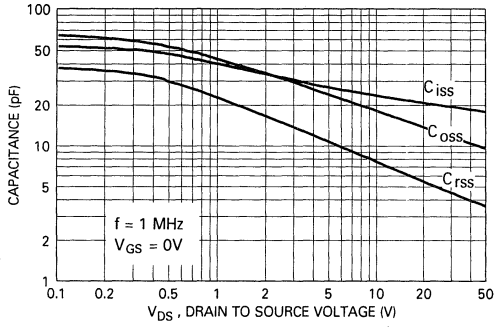


Figure 9. Capacitance Characteristics.

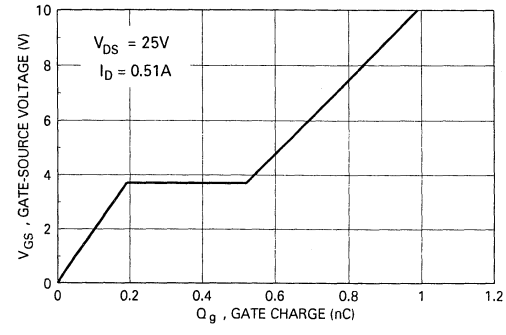


Figure 10. Gate Charge Characteristics.

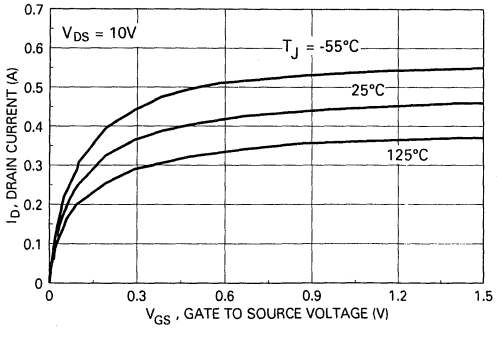


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

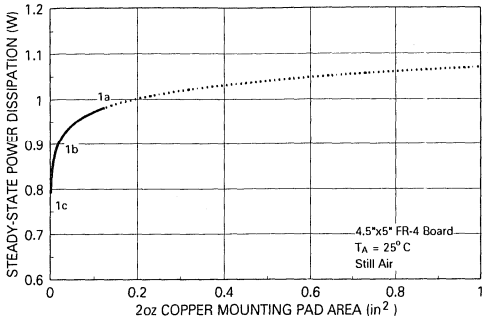


Figure 12. SuperSOT™-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

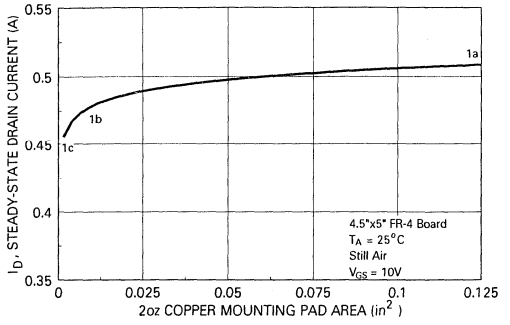


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

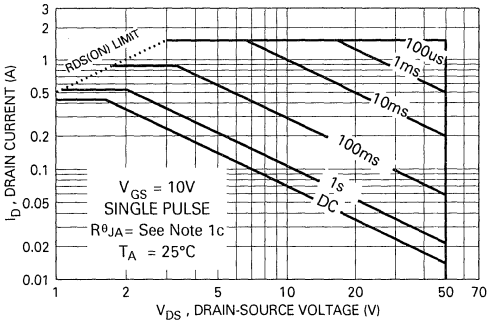


Figure 14. Maximum Safe Operating Area.

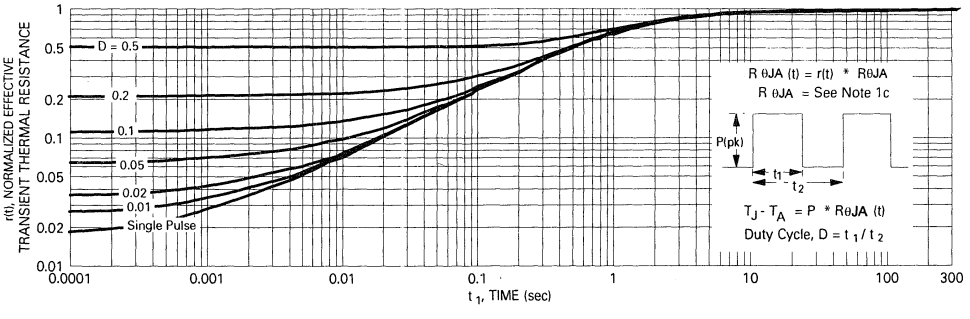


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

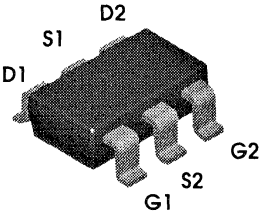
NDC7003P
Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

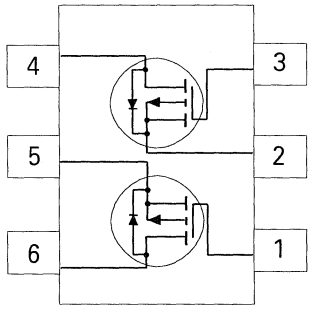
These dual P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- -0.34A, -50V. $R_{DS(ON)}$= 5Ω @ V_{GS}=-10V.
- High density cell design for low $R_{DS(ON)}$.
- Proprietary SuperSOT™-6 package design using copper lead frame for superior thermal and electrical capabilities.
- High saturation current.



SuperSOT™-6



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDC7003P	Units
V_{DSS}	Drain-Source Voltage		-50	V
V_{GSS}	Gate-Source Voltage - Continuous		-20	V
I_D	Drain Current - Continuous	(Note 1a)	-0.34	A
	- Pulsed		-1	
P_D	Maximum Power Dissipation	(Note 1a)	0.96	W
		(Note 1b)	0.9	
		(Note 1c)	0.7	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	130	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	60	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -40 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-500	
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2.5	-3.5	V
		T_J = 125°C	-0.8	-2.2	-3	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.34 A		2.5	5	Ω
		T_J = 125°C		4	10	
		V_{GS} = -4.5 V, I_D = -0.25 A		5.3	7.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -10 V	-1			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -0.34 A		250		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		40		pF
C_{oss}	Output Capacitance			13		pF
C_{rss}	Reverse Transfer Capacitance			4		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -25 V, I_D = -0.25 A, V_{GS} = -10 V, R_{GEN} = 25 Ω		14	20	nS
t_r	Turn - On Rise Time			6	20	
$t_{D(off)}$	Turn - Off Delay Time			13	20	
t_f	Turn - Off Fall Time			6	20	
Q_g	Total Gate Charge	V_{DS} = -25 V, I_D = -0.34 A, V_{GS} = -10 V		1.3		nC
Q_{gs}	Gate-Source Charge			0.23		nC
Q_{gd}	Gate-Drain Charge			0.38		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source Current				-0.34	A
I_{SM}	Maximum Pulse Source Current (Note 2)				-1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.34 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

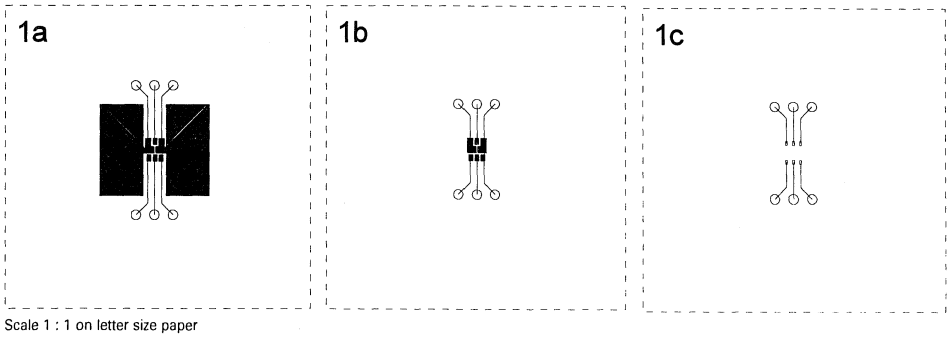
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 130°C/W when mounted on a 0.125 in² pad of 2oz copper.

b. 140°C/W when mounted on a 0.005 in² pad of 2oz copper.

c. 180°C/W when mounted on a 0.0015 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

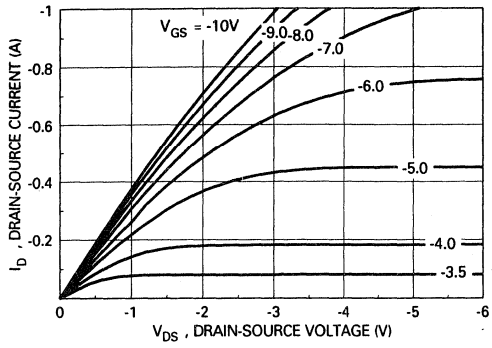


Figure 1. On-Region Characteristics.

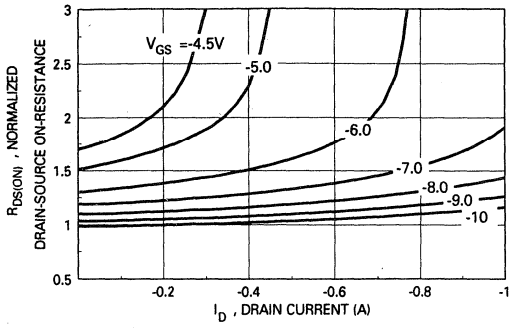


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

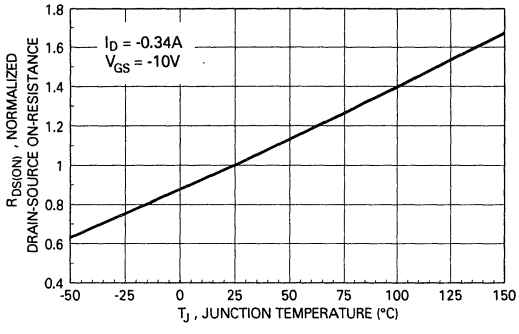


Figure 3. On-Resistance Variation with Temperature.

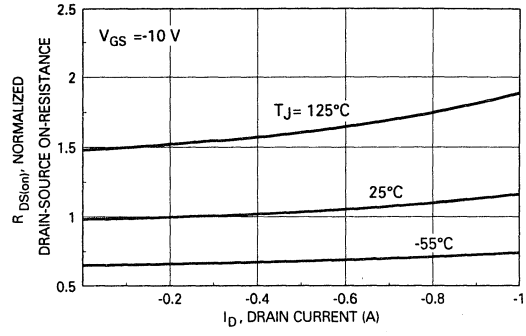


Figure 4. On-Resistance Variation with Drain Current and Temperature.

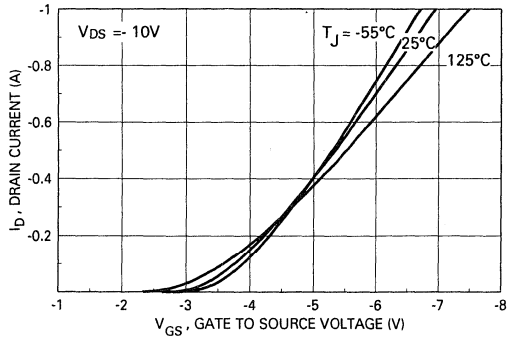


Figure 5. Transfer Characteristics.

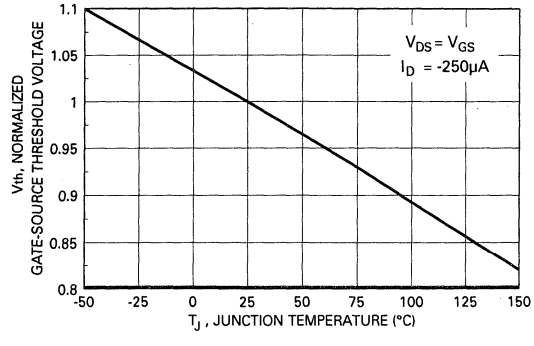


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

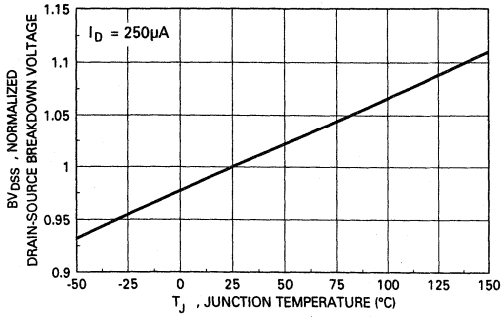


Figure 7. Breakdown Voltage Variation with Temperature.

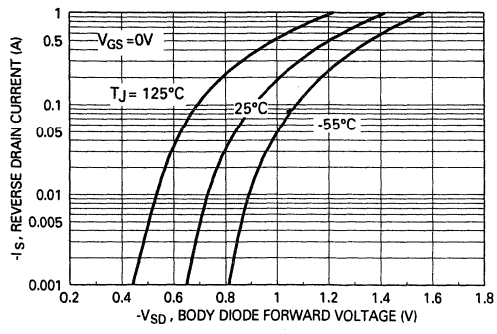


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

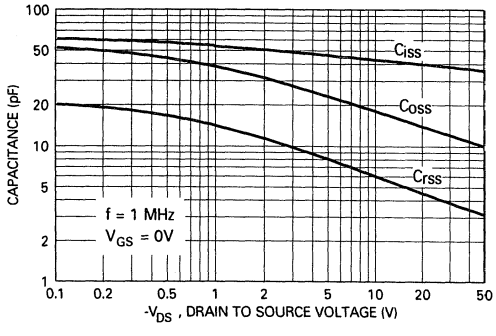


Figure 9. Capacitance Characteristics.

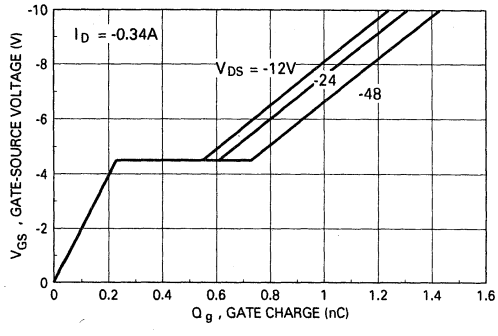


Figure 10. Gate Charge Characteristics.

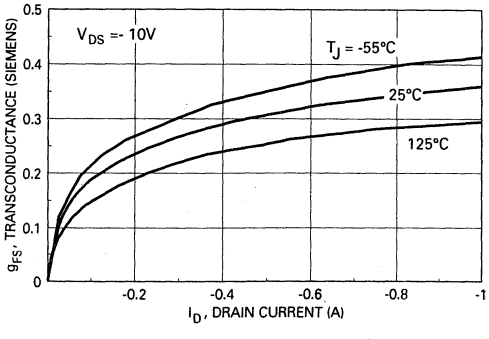


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

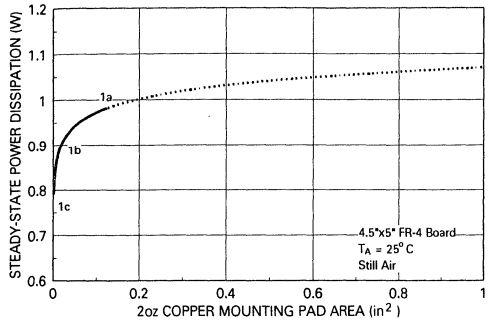


Figure 12. SuperSOT™-6 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

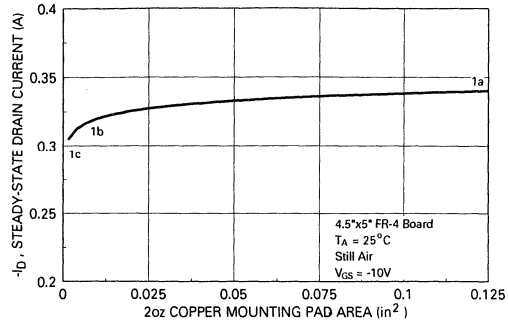


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

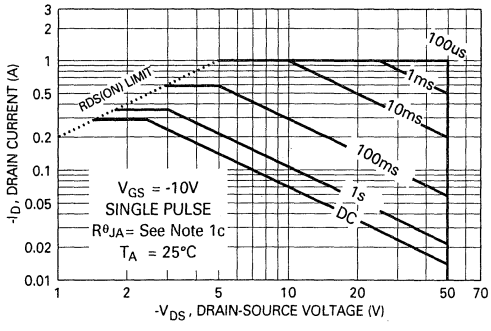


Figure 14. Maximum Safe Operating Area

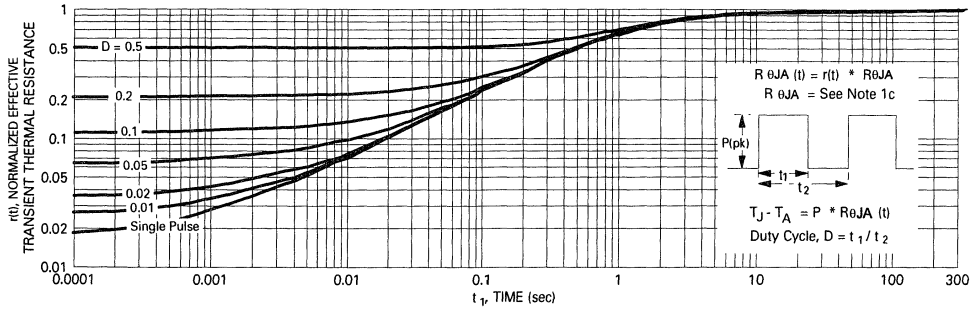


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

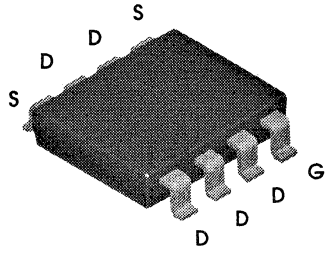
NDH831N
N-Channel Enhancement Mode Field Effect Transistor

General Description

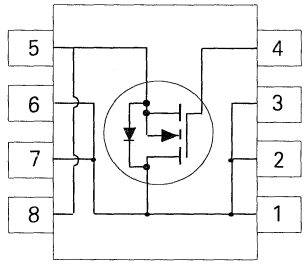
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and portable electronics where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5.8A, 20V. $R_{DS(ON)}$ = 0.03Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.04Ω @ V_{GS} = 2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- Enhanced SuperSOT™-8 small outline surface mount package with high power and current handling capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDH831N	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		8	V
I_D	Drain Current - Continuous	(Note 1a)	5.8	A
	- Pulsed		20	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.6	1	V
		T_J = 125°C	0.3	0.35	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 5.8 A		0.022	0.03	Ω
		T_J = 125°C		0.03	0.054	
		V_{GS} = 2.7 V, I_D = 5 A		0.027	0.04	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	20			A
		V_{GS} = 2.7 V, V_{DS} = 5 V	5			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.8 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		720		pF
C_{oss}	Output Capacitance			430		pF
C_{rss}	Reverse Transfer Capacitance			155		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 6 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn - On Rise Time			30	50	ns
$t_{D(off)}$	Turn - Off Delay Time			55	80	ns
t_f	Turn - Off Fall Time			20	40	ns
Q_g	Total Gate Charge	V_{DS} = 5 V, I_D = 5.8 A, V_{GS} = 4.5 V		19.5	28	nC
Q_{gs}	Gate-Source Charge			1.8		nC
Q_{gd}	Gate-Drain Charge			5.5		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.75	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

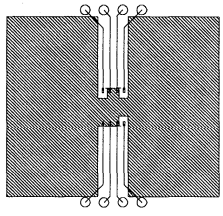
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 70°C/W when mounted on a 1 in^2 pad of 2oz copper.

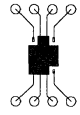
b. 125°C/W when mounted on a 0.026 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.005 in^2 pad of 2oz copper.

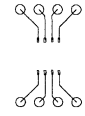
1a



1b



1c



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

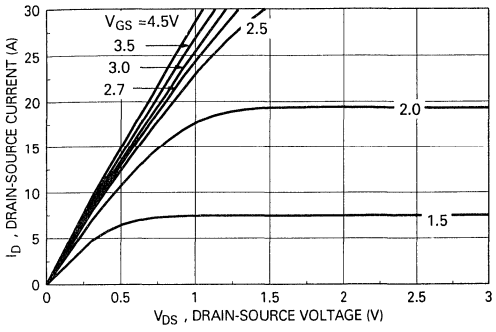


Figure 1. On-Region Characteristics.

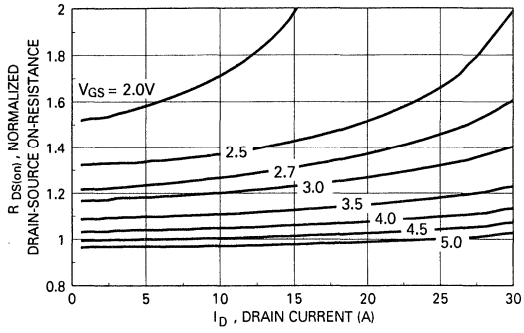


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

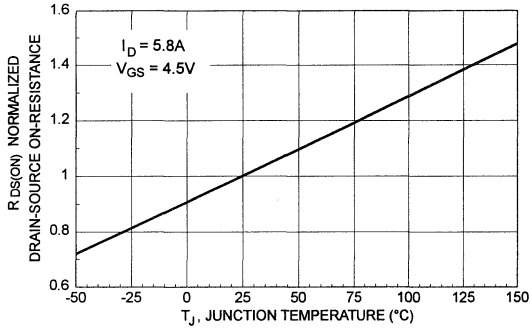


Figure 3. On-Resistance Variation with Temperature.

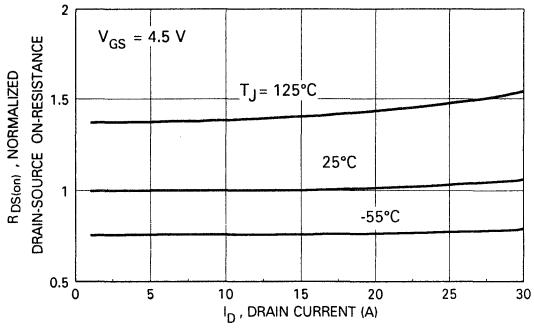


Figure 4. On-Resistance Variation with Drain Current and Temperature.

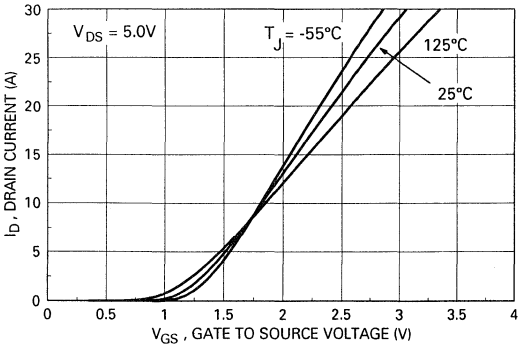


Figure 5. Transfer Characteristics.

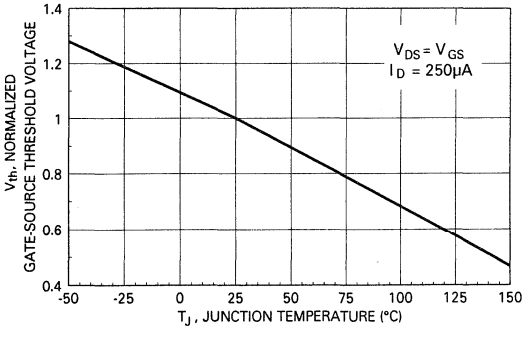


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

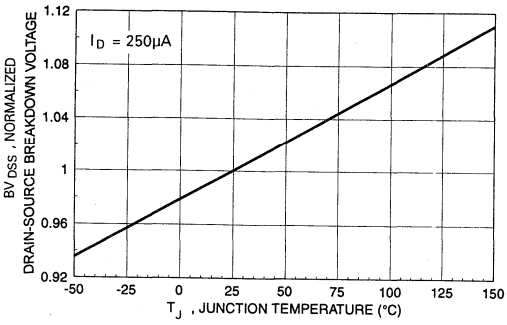


Figure 7. Breakdown Voltage Variation with Temperature.

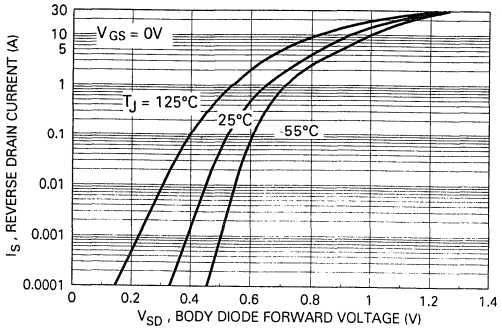


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

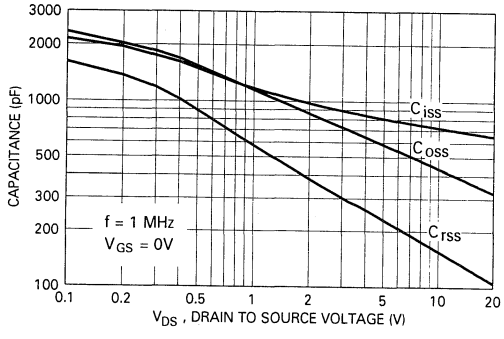


Figure 9. Capacitance Characteristics.

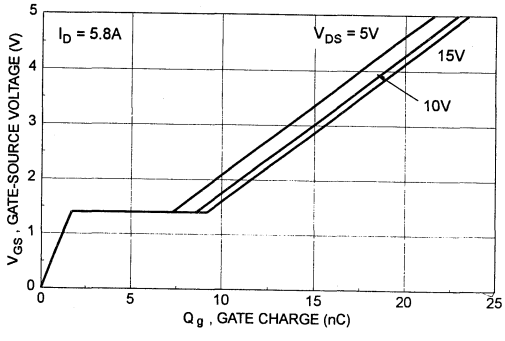


Figure 10. Gate Charge Characteristics.

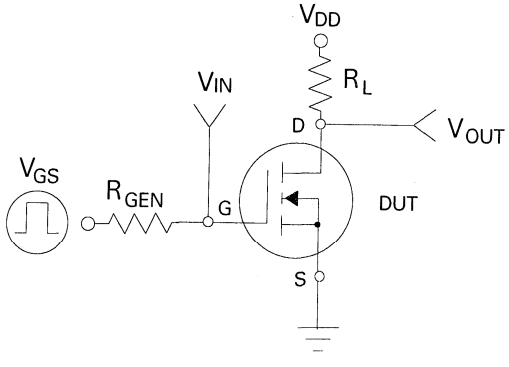


Figure 11. Switching Test Circuit

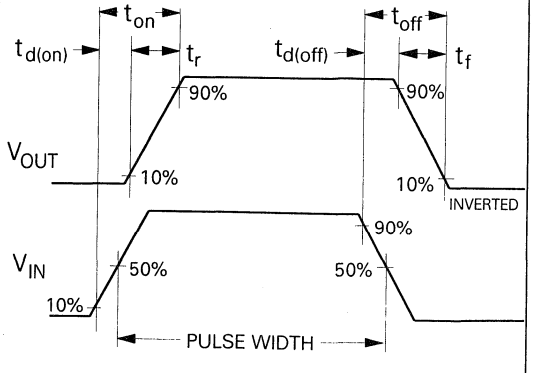


Figure 12. Switching Waveforms

Typical Thermal Characteristics

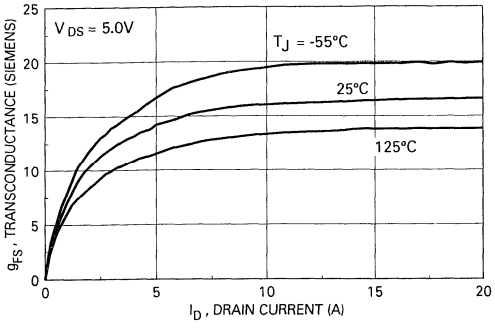


Figure 13. Transconductance Variation with Drain Current and Temperature.

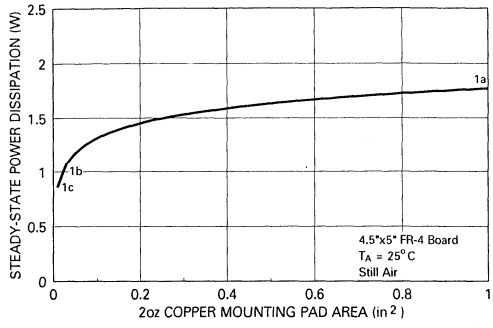


Figure 14. SuperSOT™-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

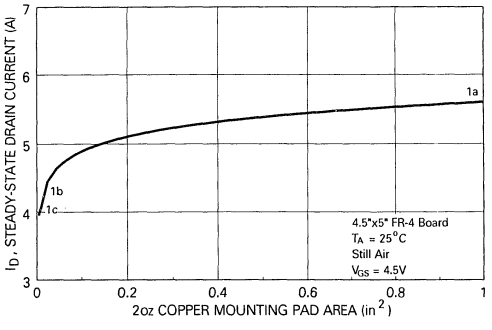


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

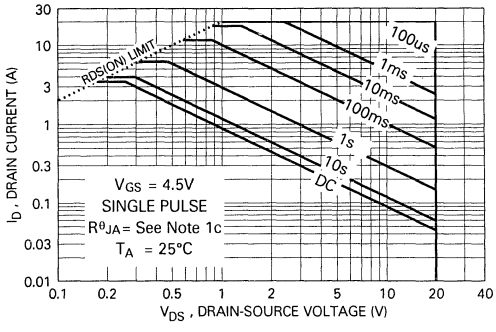


Figure 16. Maximum Safe Operating Area.

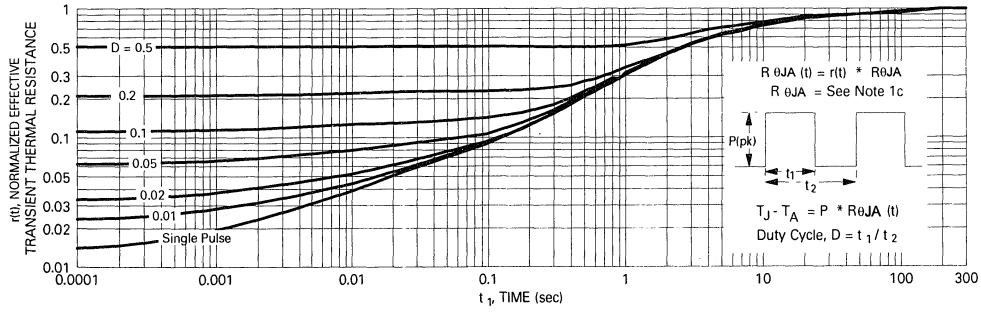


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

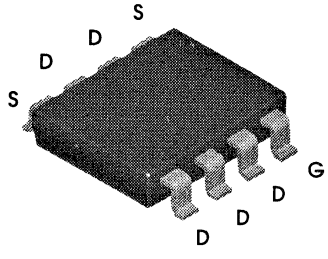
NDH832P
P-Channel Enhancement Mode Field Effect Transistor

General Description

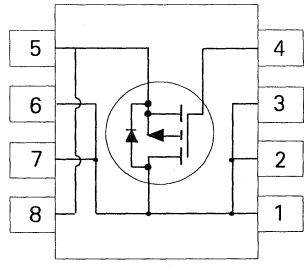
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4.2A, -20V. $R_{DS(ON)}$ = 0.06Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.08Ω @ V_{GS} = -2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- Enhanced SuperSOT™-8 small outline surface mount package with high power and current handling capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDH832P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-8	V
I_D	Drain Current - Continuous	(Note 1a)	-4.2	A
	- Pulsed		-15	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.7	-1	V
		T_J = 125°C	-0.3	-0.5	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -4.2 A		0.045	0.06	Ω
		T_J = 125°C		0.063	0.12	
		V_{GS} = -2.7 V, I_D = -3.7 A		0.064	0.08	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-15			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-5			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -4.2 A		9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1000		pF
C_{oss}	Output Capacitance			530		pF
C_{rss}	Reverse Transfer Capacitance			180		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω		13	20	ns
t_r	Turn - On Rise Time			53	70	ns
$t_{D(off)}$	Turn - Off Delay Time			60	80	ns
t_f	Turn - Off Fall Time			33	40	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -4.2 A, V_{GS} = -4.5 V		18	30	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			6		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.5 A (Note 2)		-0.75	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

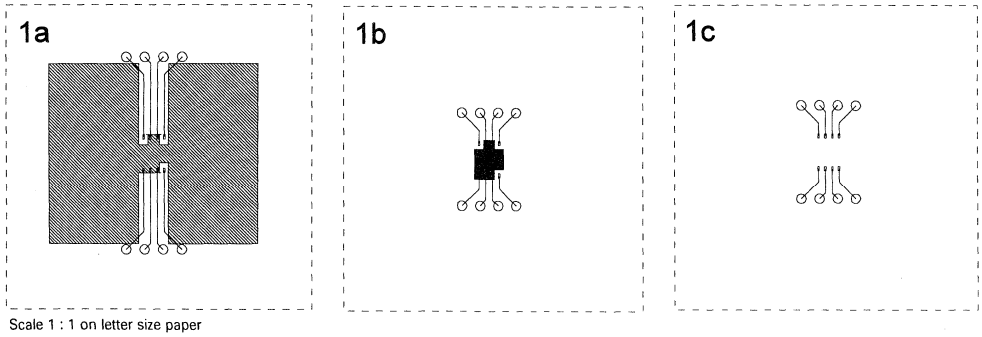
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 70°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.026 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.005 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

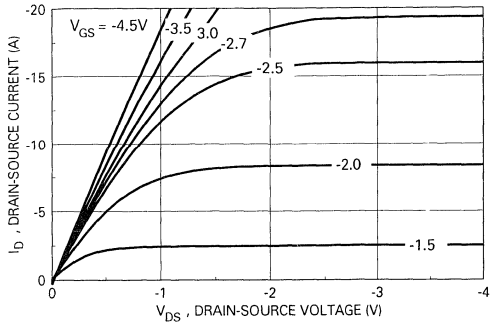


Figure 1. On-Region Characteristics.

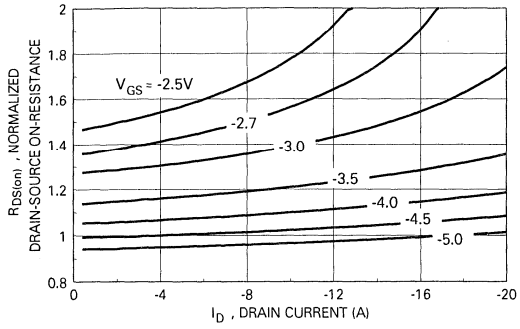


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

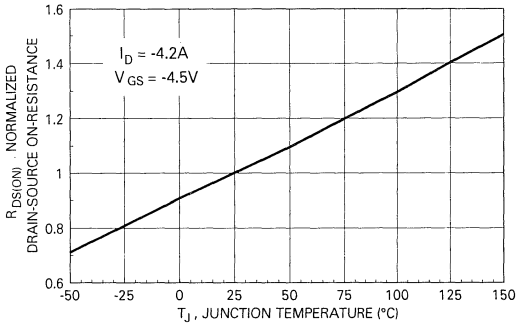


Figure 3. On-Resistance Variation with Temperature.

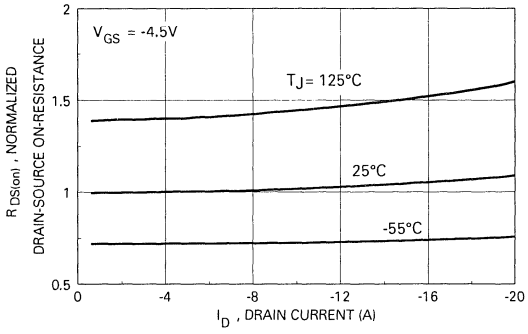


Figure 4. On-Resistance Variation with Drain Current and Temperature.

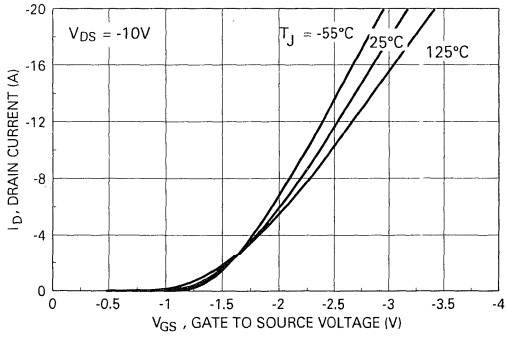


Figure 5. Transfer Characteristics.

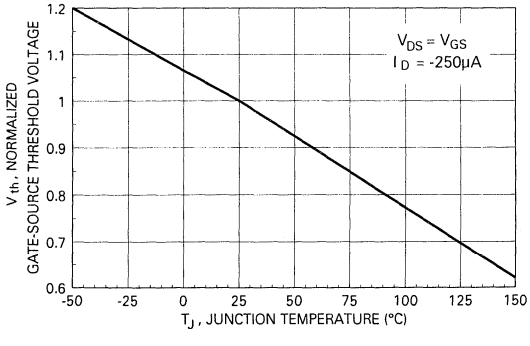


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

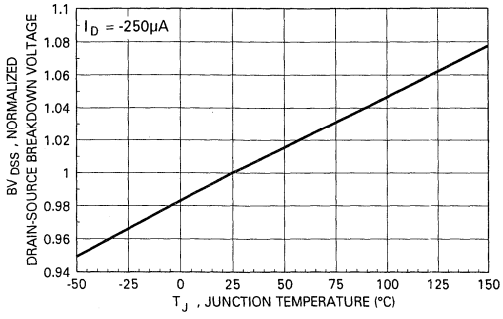


Figure 7. Breakdown Voltage Variation with Temperature.

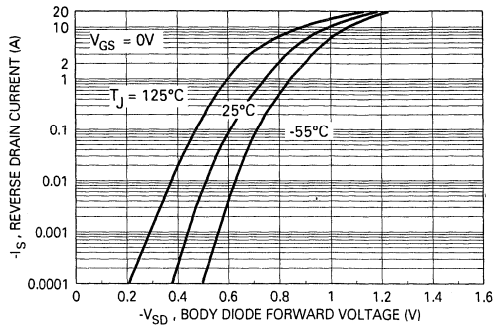


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

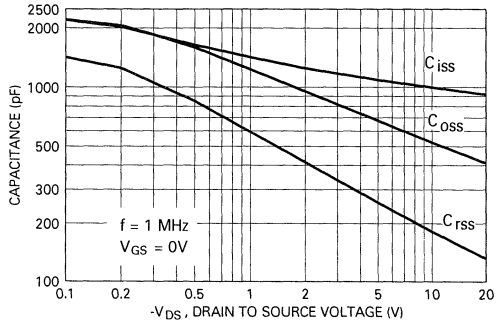


Figure 9. Capacitance Characteristics.

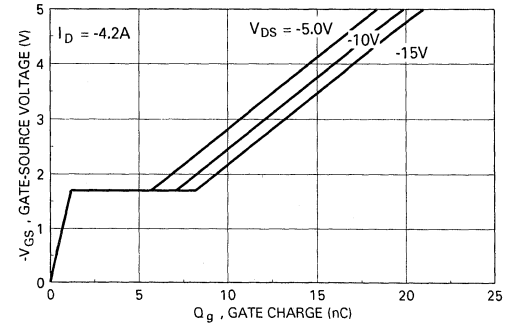


Figure 10. Gate Charge Characteristics.

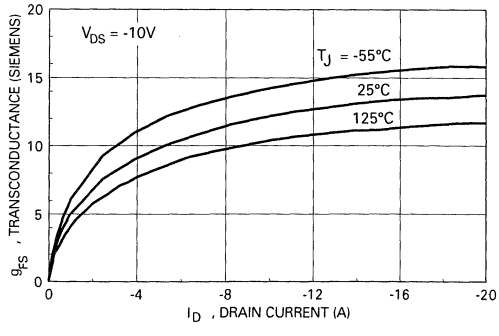


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

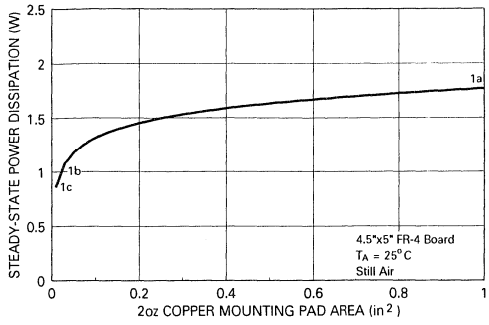


Figure 12. SuperSOT™-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

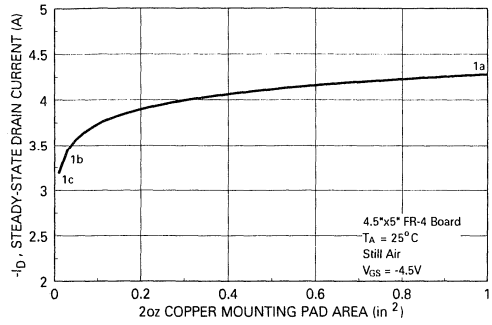


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

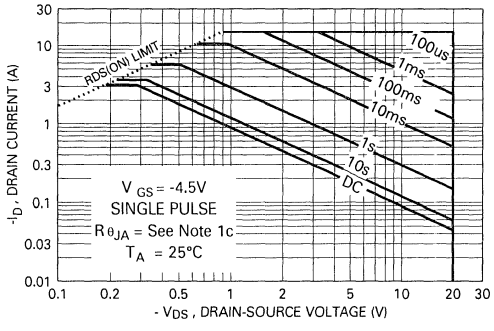


Figure 14. Maximum Safe Operating Area.

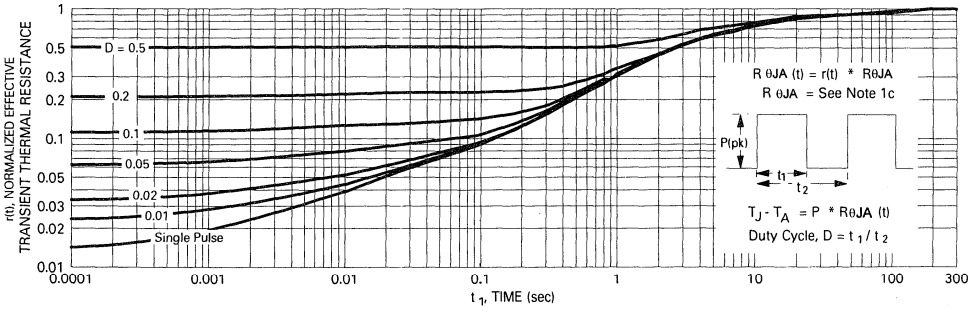


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996
ADVANCE INFORMATION

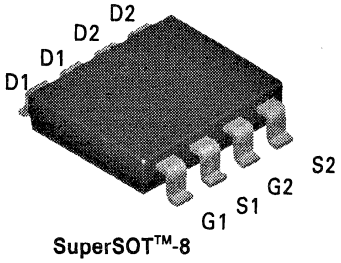
NDH8301N
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

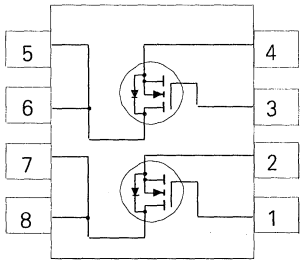
These N-Channel enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- 3A, 30V. $R_{DS(ON)}$ = 0.06Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.075Ω @ V_{GS} = 2.7V.
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDH8301N	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	8	V
I_D	Drain Current - Continuous (Note 1)	3	A
	- Pulsed	9	
P_D	Maximum Power Dissipation (Note 1)	0.9	W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	135	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1	V
		T_J = 125°C	0.3		0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 3 A			0.06	Ω
		T_J = 125°C			0.11	
		V_{GS} = 2.7 V, I_D = 2.7 A			0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	9			A
		V_{GS} = 2.7 V, V_{DS} = 5 V	3			
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				0.75	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.75 A (Note 2)			1.2	V

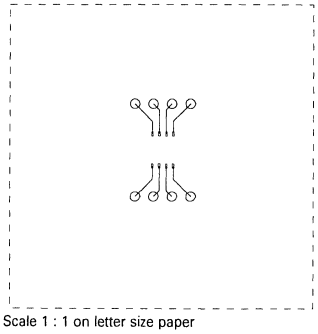
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

135°C/W when mounted on a 0.0025in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

June 1996
ADVANCE INFORMATION

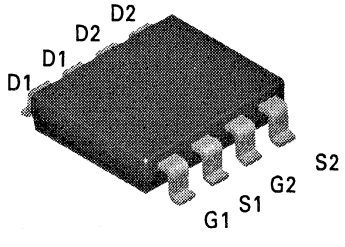
NDH8302P
Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

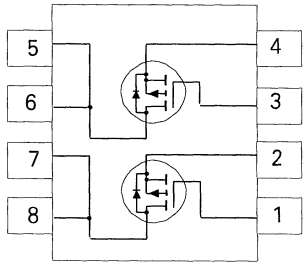
These P-Channel enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast high-side switching, and low in-line power loss are needed in a very small outline surface mount package.

Features

- -2A, -20V. $R_{DS(ON)}$ = 0.13Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.19Ω @ V_{GS} = -2.7V.
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDH8302P	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage - Continuous		-8	V
I_D	Drain Current - Continuous	(Note 1)	-2	A
	- Pulsed		-6	
P_D	Maximum Power Dissipation	(Note 1)	0.9	W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1)	135	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4		-1	V
		T_J = 125°C	-0.3		-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -2 A			0.13	Ω
		T_J = 125°C			0.24	
		V_{GS} = -2.7 V, I_D = -1.7 A			0.19	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-6			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-2			
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				-0.75	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.75 A (Note 2)			-1.2	V

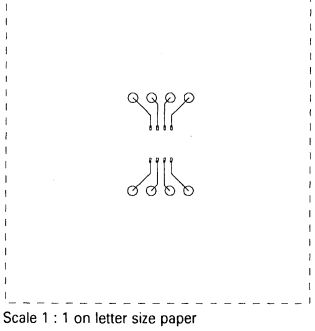
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

135°C/W when mounted on a 0.0025in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

May 1996

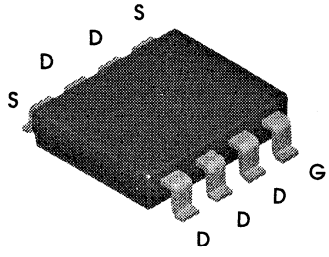
NDH8436
N-Channel Enhancement Mode Field Effect Transistor

General Description

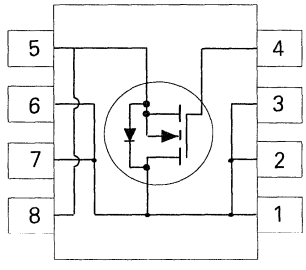
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and portable electronics where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5.8A, 30V. $R_{DS(ON)}$ = 0.03Ω @ V_{GS} = 10V
  $R_{DS(ON)}$ = 0.045Ω @ V_{GS} = 4.5V
- High density cell design for extremely low $R_{DS(ON)}$.
- Enhanced SuperSOT™-8 small outline surface mount package with high power and current handling capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDH8436	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		20	V
I_D	Drain Current - Continuous	(Note 1a)	5.8	A
	- Pulsed		20	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	2.8	V
		T_J = 125°C	0.7	1.2	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5.8 A		0.022	0.03	Ω
		T_J = 125°C		0.032	0.06	
		V_{GS} = 4.5 V, I_D = 5 A		0.035	0.045	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A		11		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		560		pF
C_{oss}	Output Capacitance			360		pF
C_{rss}	Reverse Transfer Capacitance			125		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		12	20	ns
t_r	Turn - On Rise Time			15	25	ns
$t_{D(off)}$	Turn - Off Delay Time			24	40	ns
t_f	Turn - Off Fall Time			12	20	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 5.8 A, V_{GS} = 10 V		20	30	nC
Q_{gs}	Gate-Source Charge			2.2		nC
Q_{gd}	Gate-Drain Charge			5.2		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)			1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

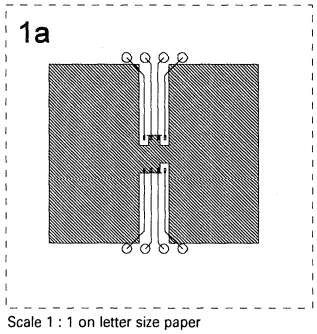
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 70°C/W when mounted on a 1 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.026 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.005 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

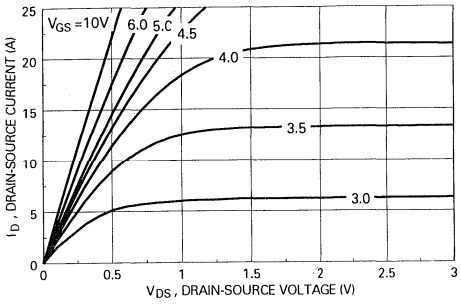


Figure 1. On-Region Characteristics

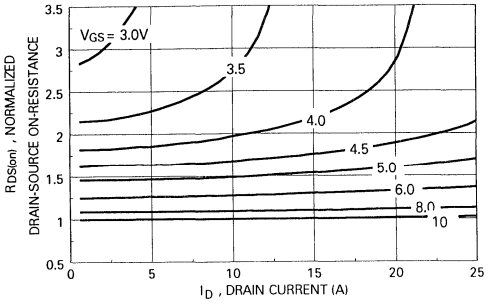


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

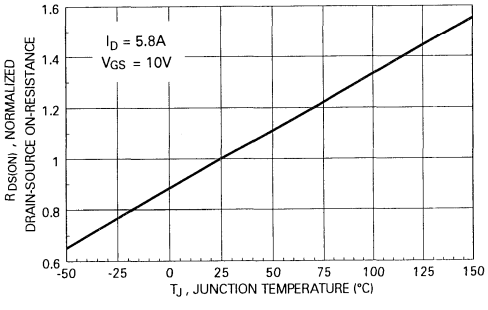


Figure 3. On-Resistance Variation with Temperature

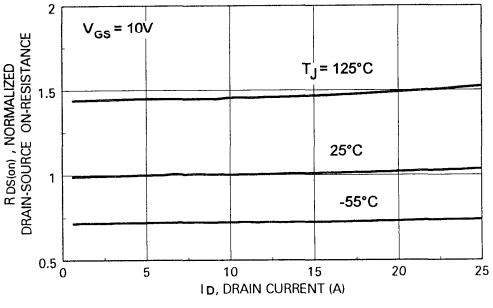


Figure 4. On-Resistance Variation with Drain Current and Temperature

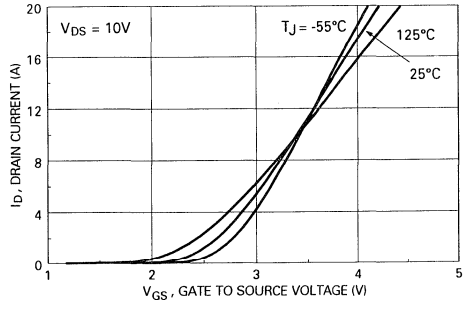


Figure 5. Transfer Characteristics

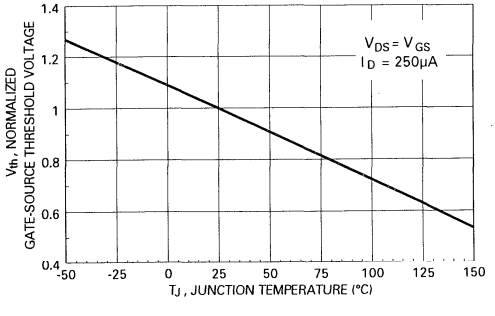


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

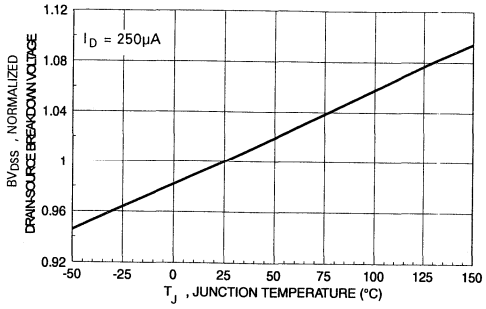


Figure 7. Breakdown Voltage Variation with Temperature

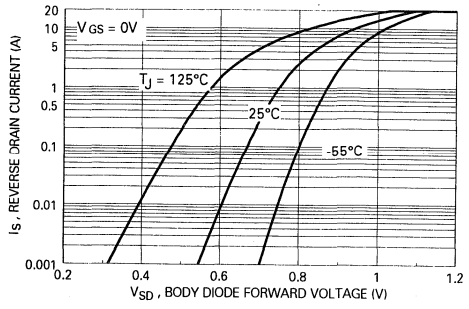


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

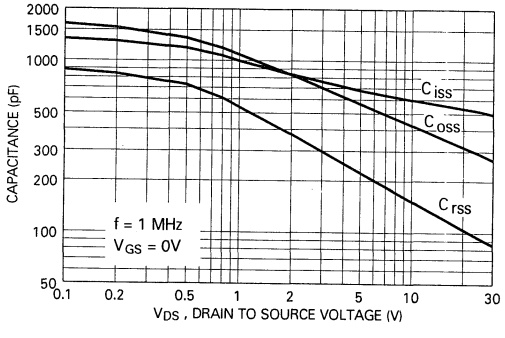


Figure 9. Capacitance Characteristics

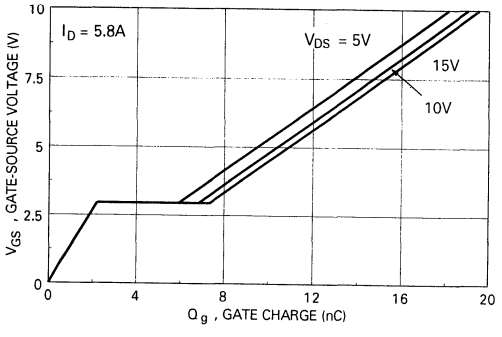


Figure 10. Gate Charge Characteristics

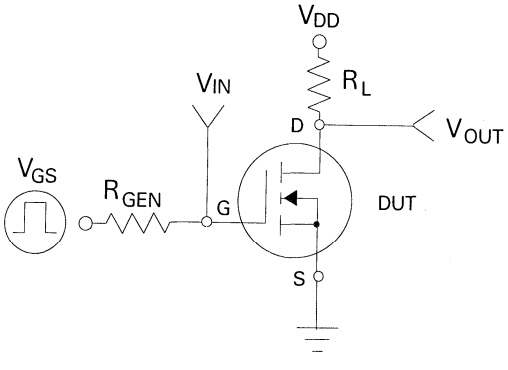


Figure 11. Switching Test Circuit

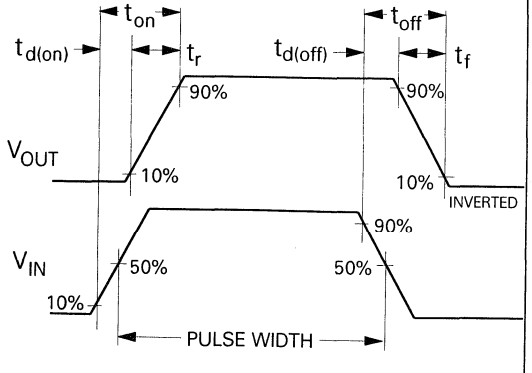


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

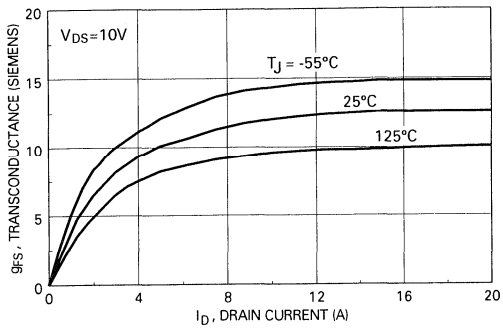


Figure 13. Transconductance Variation with Drain Current and Temperature

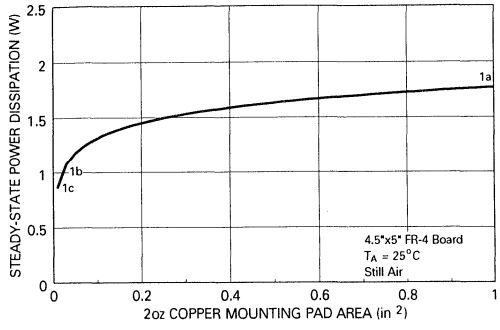


Figure 14. SuperSOT™-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

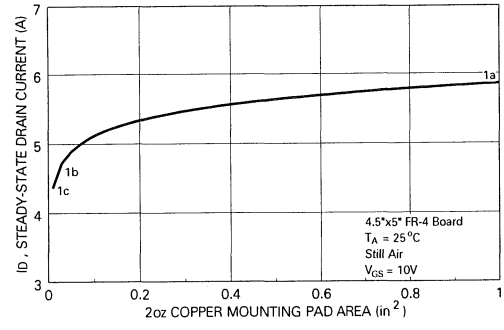


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

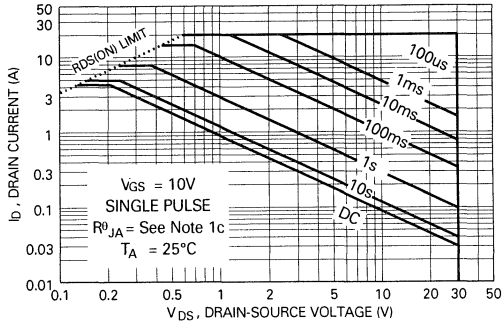


Figure 16. Maximum Safe Operating Area

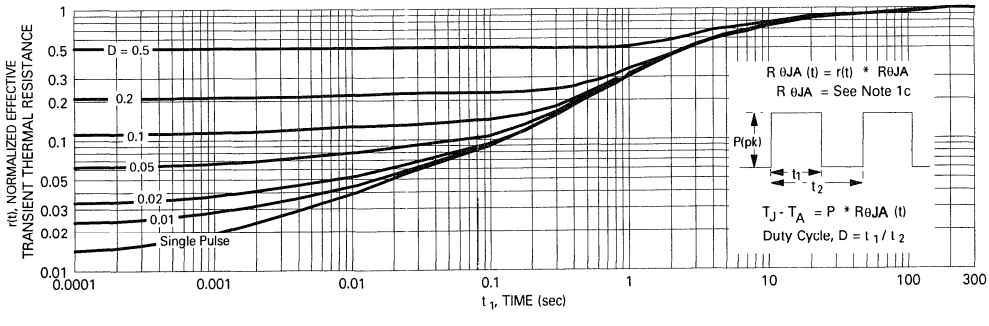


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

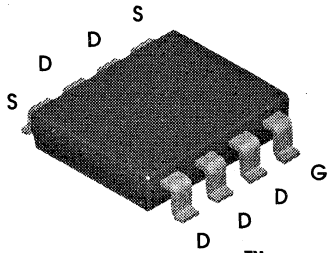
NDH8447
P-Channel Enhancement Mode Field Effect Transistor

General Description

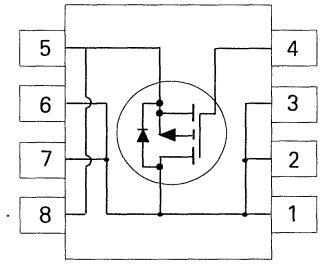
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4.4A, -30V. $R_{DS(ON)}$ = 0.053 @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.095Ω @ V_{GS} = -4.5V
- High density cell design for extremely low $R_{DS(ON)}$.
- Enhanced SuperSOT™-8 small outline surface mount package with high power and current handling capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDH8447	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		-20	V
I_D	Drain Current - Continuous	(Note 1a)	-4.4	A
	- Pulsed		-20	
P_D	Maximum Power Dissipation	(Note 1a)	1.8	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	70	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	20	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.5	-3	V
		T_J = 125°C	-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -4.4 A		0.045	0.053	Ω
		T_J = 125°C		0.075	0.11	
		V_{GS} = -4.5 V, I_D = -3.4 A		0.08	0.095	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -4.4 A		7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		670		pF
C_{oss}	Output Capacitance			430		pF
C_{rss}	Reverse Transfer Capacitance			160		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn - On Rise Time			15	25	ns
$t_{D(off)}$	Turn - Off Delay Time			36	50	ns
t_f	Turn - Off Fall Time			27	40	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -4.4 A, V_{GS} = -10 V		20	30	nC
Q_{gs}	Gate-Source Charge			2.8		nC
Q_{gd}	Gate-Drain Charge			6		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.5 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

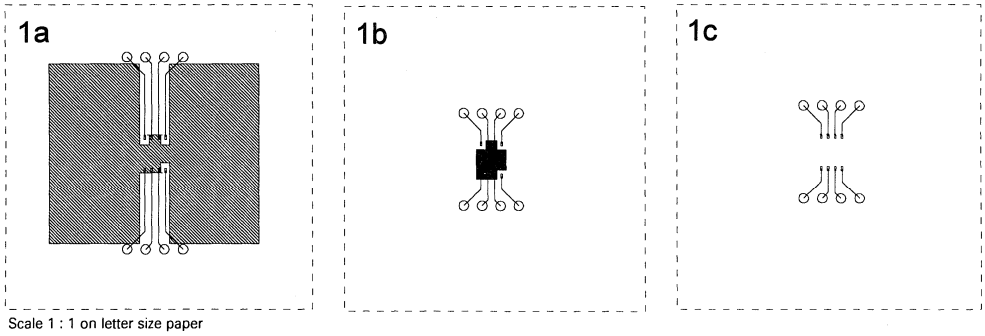
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 70°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.026 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.005 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

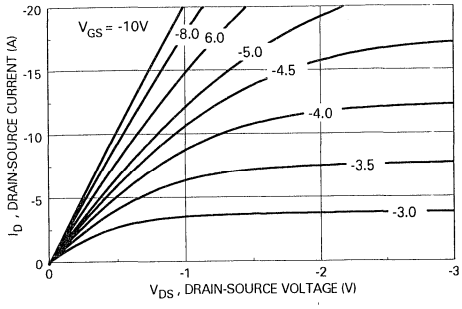


Figure 1. On-Region Characteristics

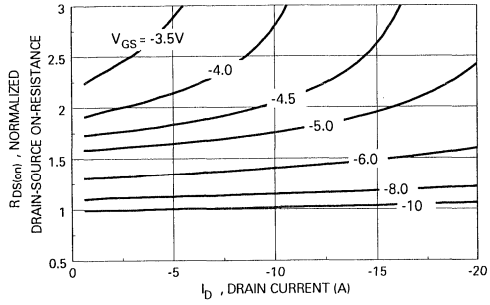


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

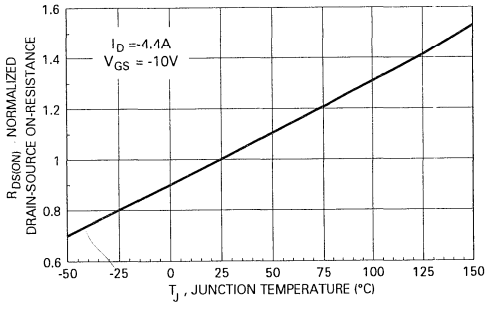


Figure 3. On-Resistance Variation with Temperature

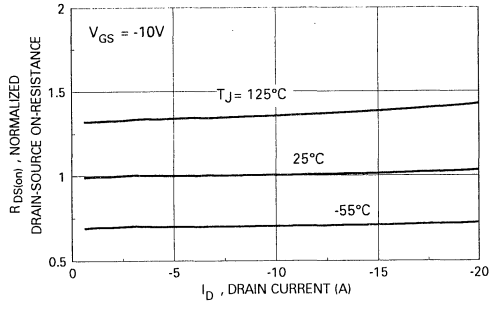


Figure 4. On-Resistance Variation with Drain Current and Temperature

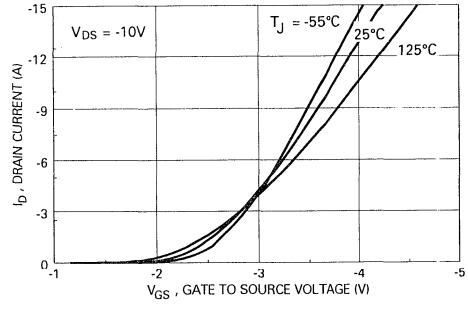


Figure 5. Transfer Characteristics

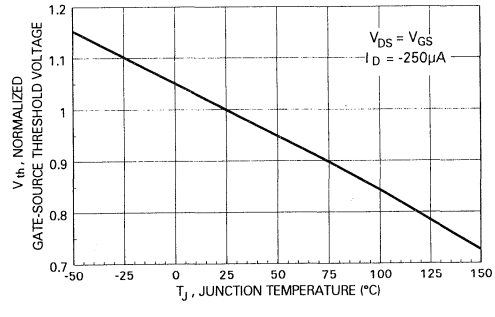


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

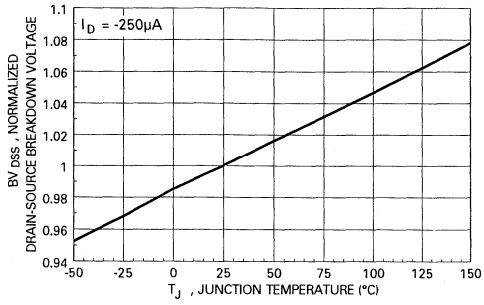


Figure 7. Breakdown Voltage Variation with Temperature

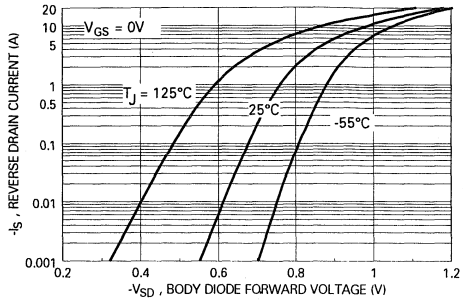


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

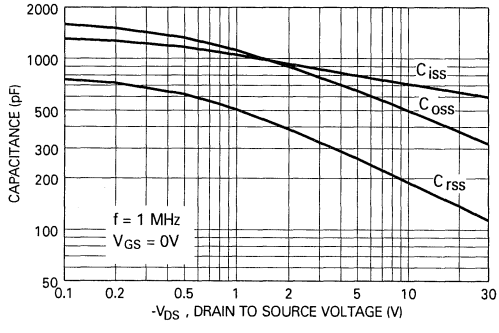


Figure 9. Capacitance Characteristics

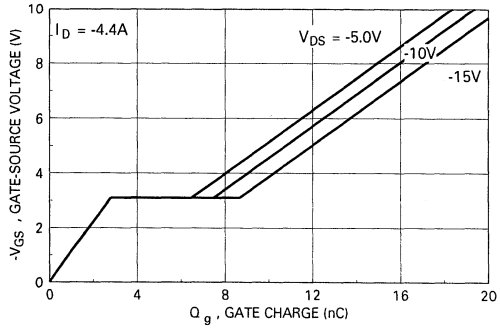


Figure 10. Gate Charge Characteristics

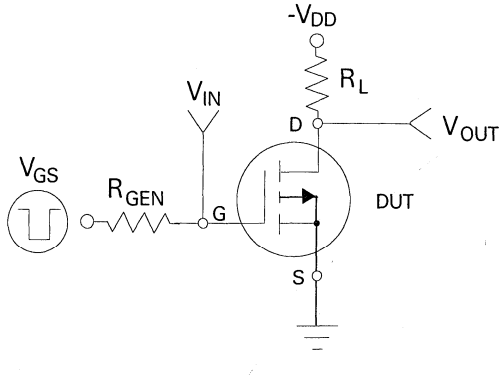


Figure 11. Switching Test Circuit

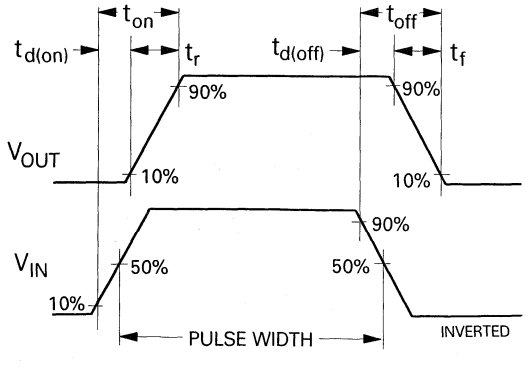


Figure 12. Switching Waveforms

Typical Electrical and ThermalCharacteristics (continued)

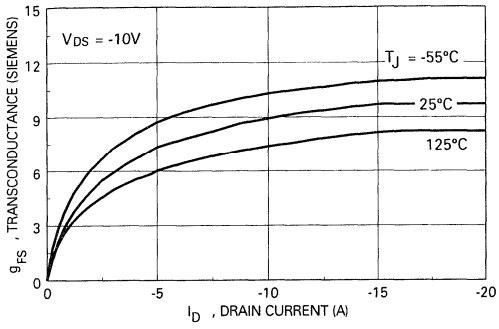


Figure 13. Transconductance Variation with Drain Current and Temperature

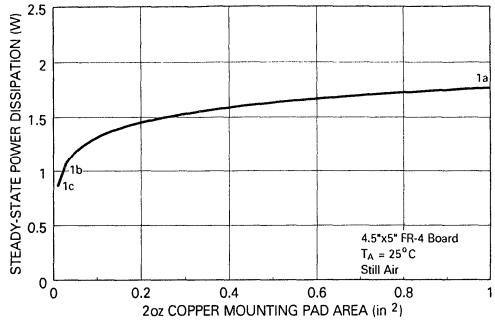


Figure 14. SuperSOT™-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

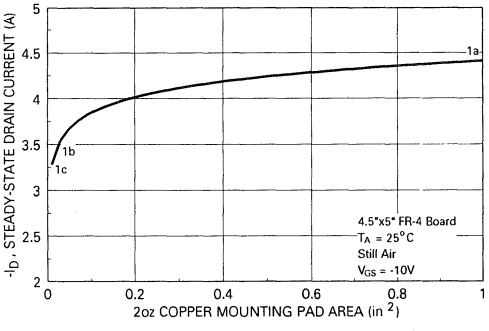


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

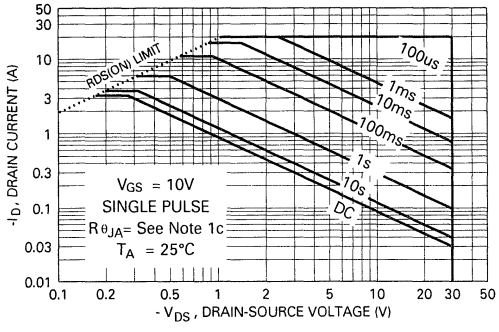


Figure 16. Maximum Safe Operating Area

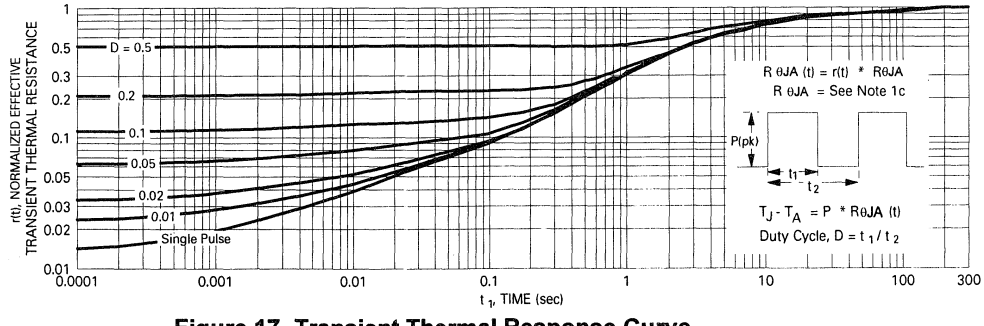


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996
ADVANCE INFORMATION

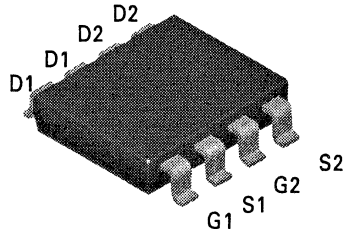
NDH8502P
Dual P-Channel Enhancement Mode Field Effect Transistor

General Description

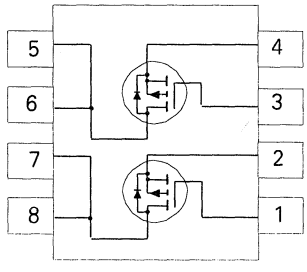
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -2.3A, -30V. $R_{DS(ON)}$ = 0.11Ω @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.18Ω @ V_{GS} = -4.5V
- High density cell design for extremely low $R_{DS(ON)}$.
- Enhanced SuperSOT™-8 small outline surface mount package with high power and current handling capability.



SuperSOT™-8



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDH8502P	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage	-20	V
I_D	Drain Current - Continuous (Note 1)	-2.3	A
	- Pulsed	-7	
P_D	Maximum Power Dissipation (Note 1)	0.9	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	135	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.5	-3	V
		T_J = 125°C	-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.3 A			0.11	Ω
		T_J = 125°C			0.2	
		V_{GS} = -4.5 V, I_D = -1.8 A			0.18	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-7			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2.3 A		3		S
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.75	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.75 A (Note 2)			-1.2	V

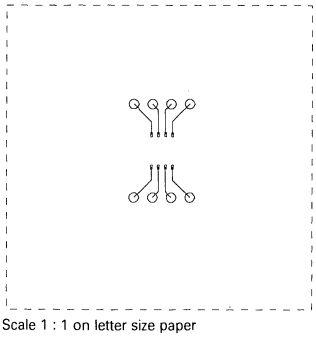
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

135°C/W when mounted on a 0.005 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Section 4

SO-8 Data Sheets

National Semiconductor™

May 1996

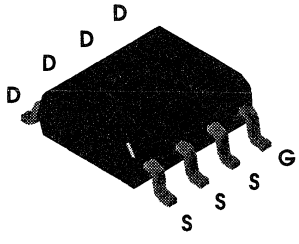
NDS8410
Single N-Channel Enhancement Mode Field Effect Transistor

General Description

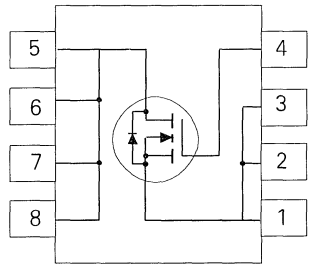
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 10A, 30V. $R_{DS(ON)}$ = 0.015Ω @ V_{GS} = 10V
  $R_{DS(ON)}$ = 0.020Ω @ V_{GS} = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



8-SOIC



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8410	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		20	V
I_D	Drain Current - Continuous	(Note 1a)	± 10	A
	- Pulsed		± 50	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5		V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 10 A		0.013	0.015	Ω
		V_{GS} = 4.5 V, I_D = 9 A		0.018	0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 10 A		22		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1350		pF
C_{oss}	Output Capacitance			800		pF
C_{rss}	Reverse Transfer Capacitance			300		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		14	30	ns
t_r	Turn - On Rise Time			20	25	ns
$t_{D(off)}$	Turn - Off Delay Time			56	100	ns
t_f	Turn - Off Fall Time			31	80	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 10 A, V_{GS} = 10 V		46	60	nC
Q_{gs}	Gate-Source Charge			5.6		nC
Q_{gd}	Gate-Drain Charge			14		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 10 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 2.1 A, dI_F/dt = 100 A/µs			80	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

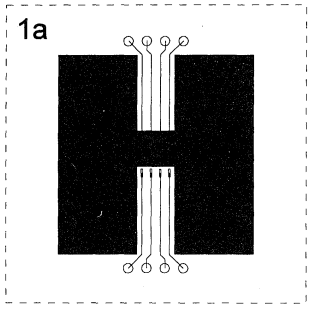
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

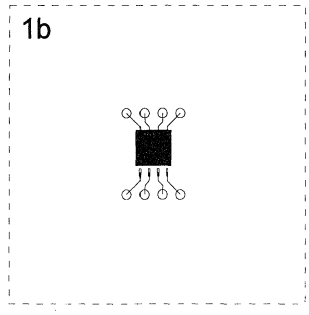
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

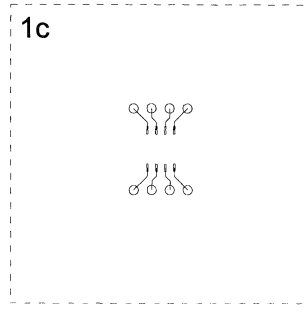
a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

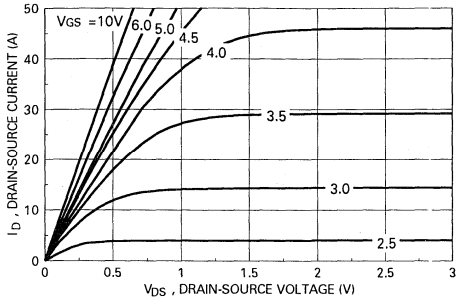


Figure 1. On-Region Characteristics

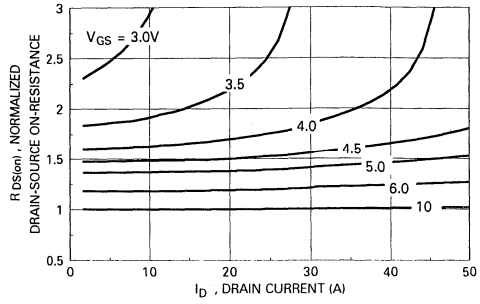


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

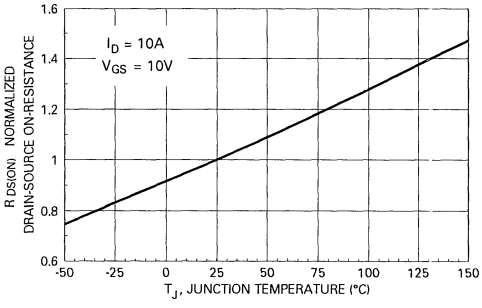


Figure 3. On-Resistance Variation with Temperature

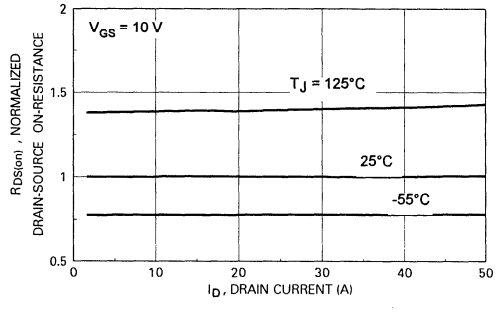


Figure 4. On-Resistance Variation with Drain Current and Temperature

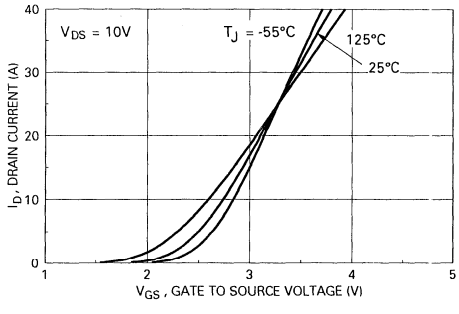


Figure 5. Transfer Characteristics

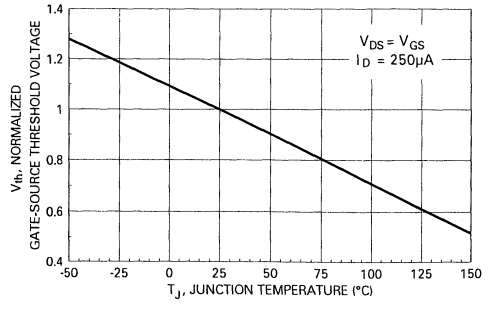


Figure 6. Gate Threshold Variation with Temperature

4

Typical Electrical Characteristics (continued)

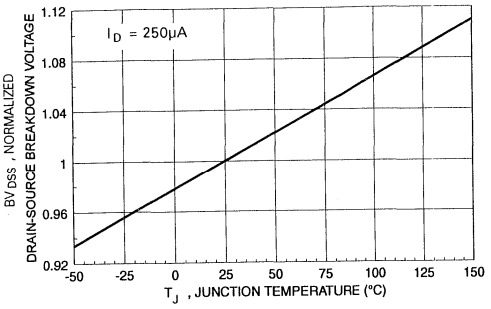


Figure 7. Breakdown Voltage Variation with Temperature

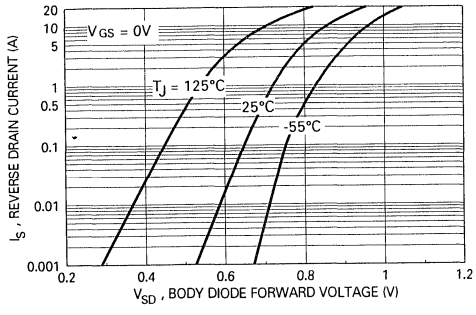


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

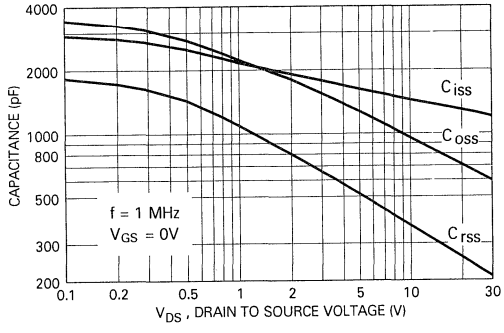


Figure 9. Capacitance Characteristics

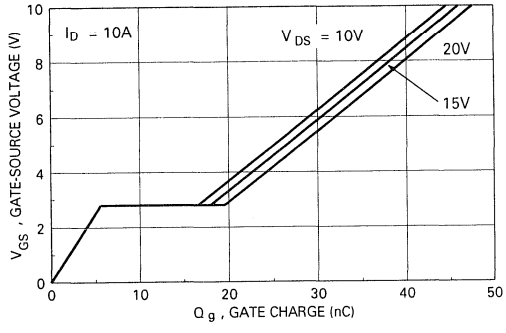


Figure 10. Gate Charge Characteristics

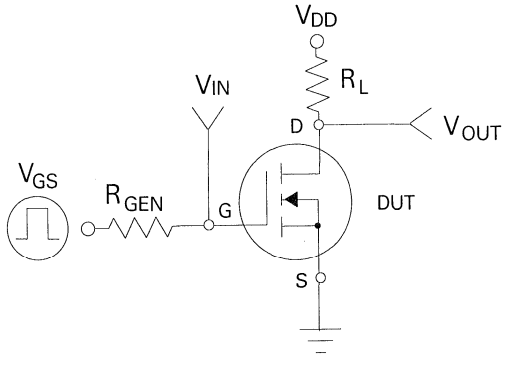


Figure 11. Switching Test Circuit

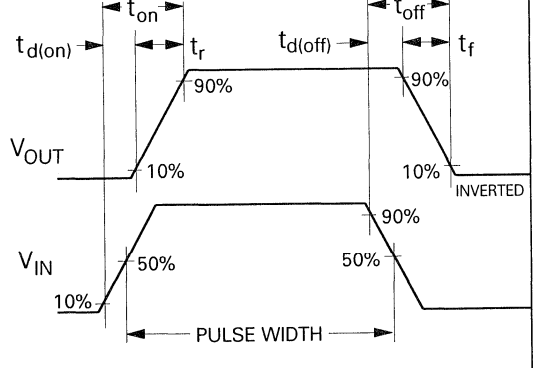


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

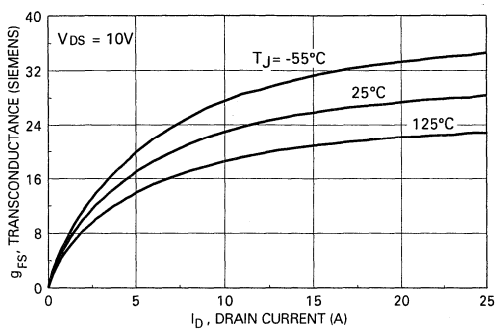


Figure 13. Transconductance Variation with Drain Current and Temperature

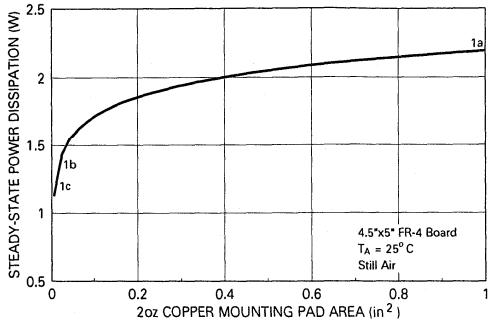


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

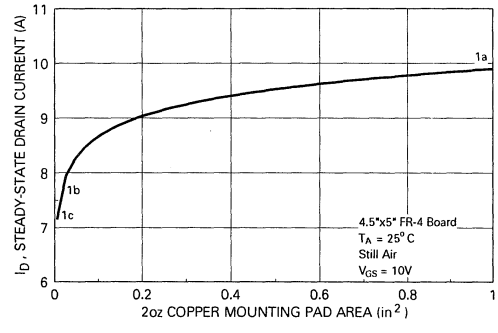


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

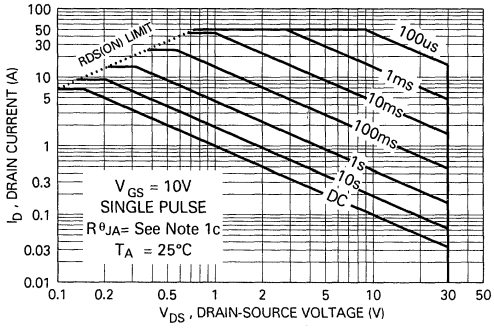


Figure 16. Maximum Safe Operating Area

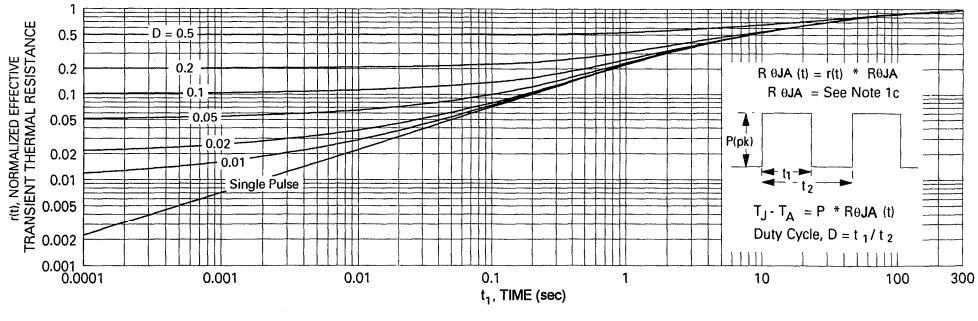


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996
ADVANCE INFORMATION

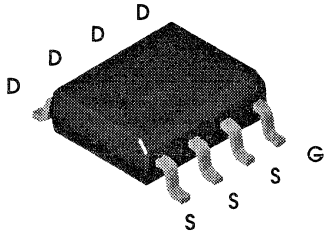
NDS8425
Single N-Channel Enhancement Mode Field Effect Transistor

General Description

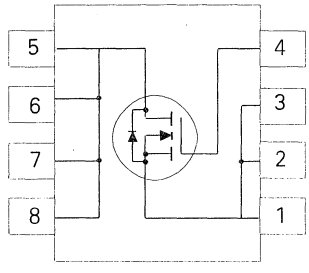
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 7.4 A, 20 V. $R_{DS(ON)}$ = 0.025Ω @ V_{GS}= 4.5 V
  $R_{DS(ON)}$ = 0.03Ω @ V_{GS}= 2.7 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



8-SOIC



ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8425	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		15	V
I_D	Drain Current - Continuous	(Note 1a)	± 7.4	A
	- Pulsed		± 20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4			V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 7.4 A			0.025	Ω
		V_{GS} = 2.7 V, I_D =6.5 A			0.03	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.4 A	5			S
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.4 A (Note 2)			1.3	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

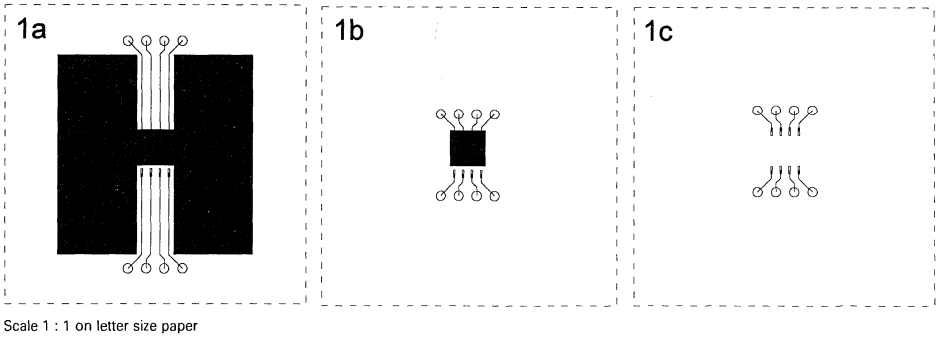
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

July 1996

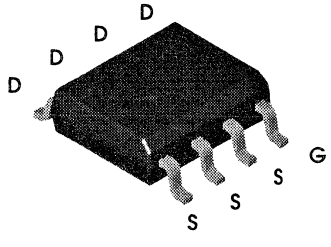
NDS8426
Single N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 9.9A, 20V. $R_{DS(ON)}$ = 0.015Ω @ V_{GS}=4.5V.
  $R_{DS(ON)}$ = 0.020Ω @ V_{GS}=2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



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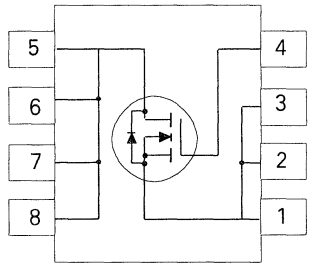


ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8426	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		8	V
I_D	Drain Current - Continuous	(Note 1a)	9.9	A
	- Pulsed		20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.6	1	V
		T_J = 125°C	0.3	0.34	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 9.9 A		0.013	0.015	Ω
		T_J = 125°C		0.017	0.027	
		V_{GS} = 2.7 V, I_D = 8.8 A		0.016	0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 9.9 A		38		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1765		pF
C_{oss}	Output Capacitance			940		pF
C_{rss}	Reverse Transfer Capacitance			360		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 5 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω		15	30	ns
t_r	Turn - On Rise Time			30	55	ns
$t_{D(off)}$	Turn - Off Delay Time			120	220	ns
t_f	Turn - Off Fall Time			58	100	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 9.9 A, V_{GS} = 4.5 V		10.4	15	nC
Q_{gs}	Gate-Source Charge			1		nC
Q_{gd}	Gate-Drain Charge			3.2		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.65	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

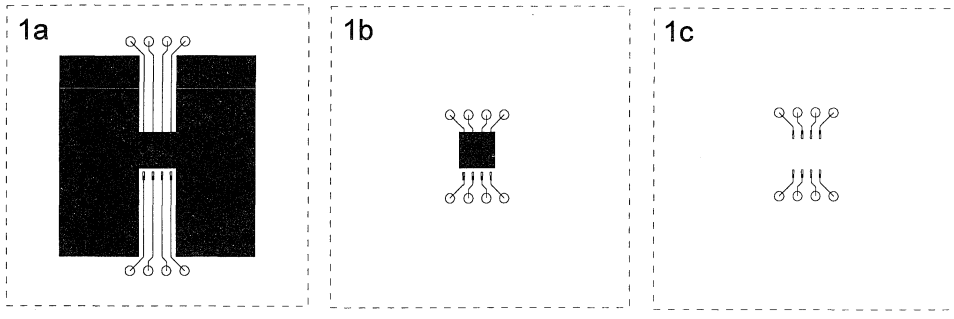
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

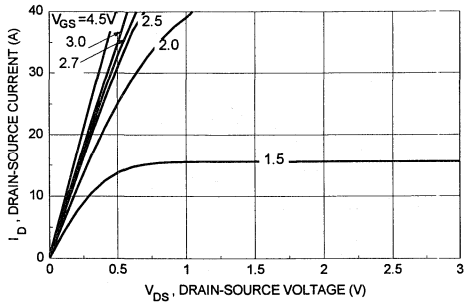


Figure 1. On-Region Characteristics

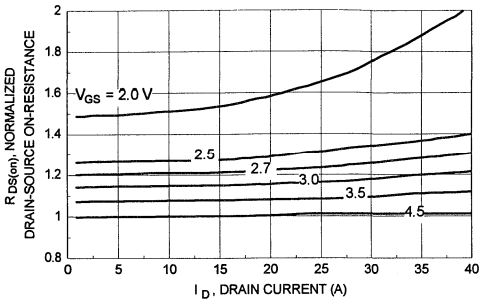


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

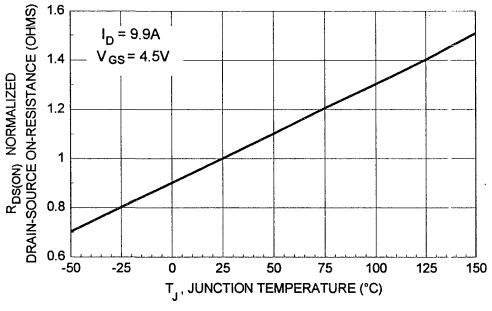


Figure 3. On-Resistance Variation with Temperature

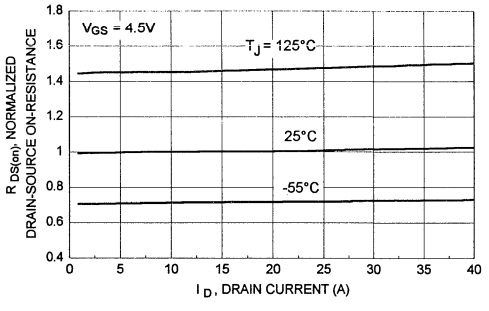


Figure 4. On-Resistance Variation with Drain Current and Temperature

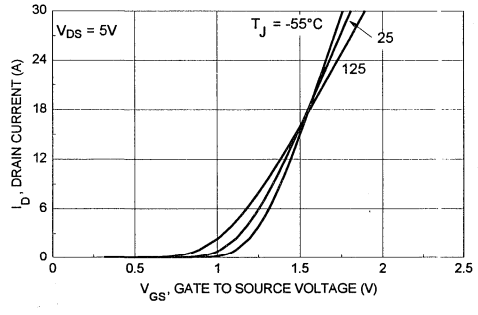


Figure 5. Transfer Characteristics

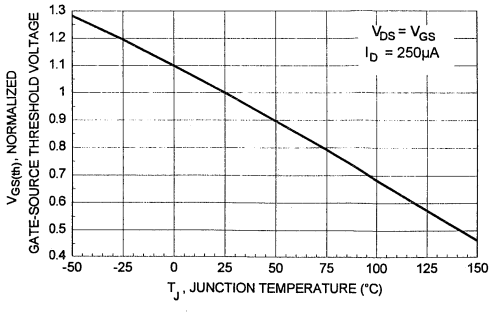


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

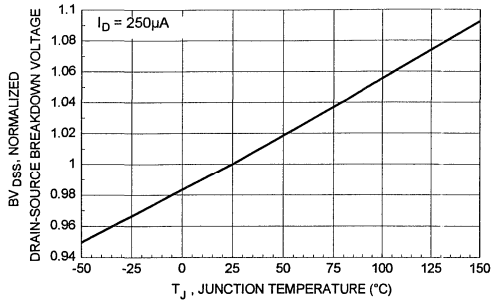


Figure 7. Breakdown Voltage Variation with Temperature

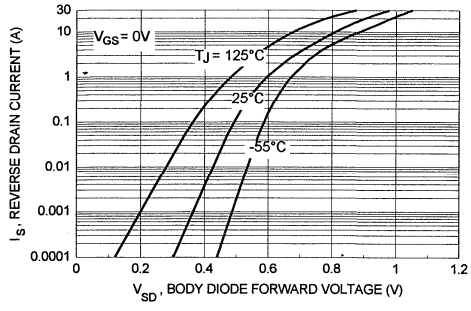


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

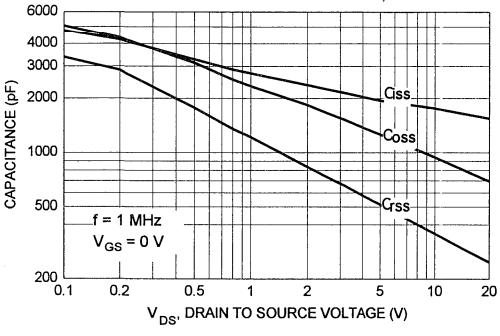


Figure 9. Capacitance Characteristics

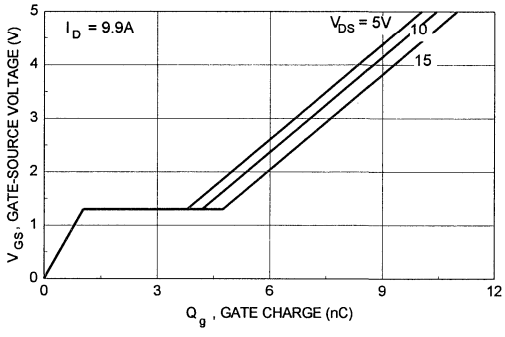


Figure 10. Gate Charge Characteristics

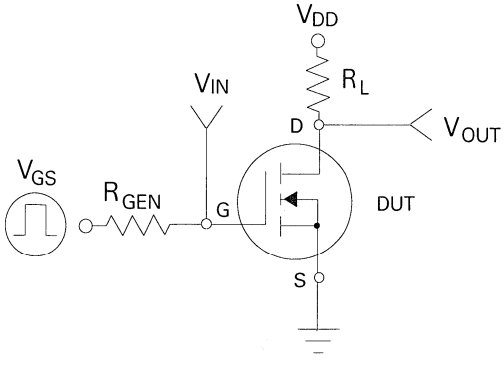


Figure 11. Switching Test Circuit

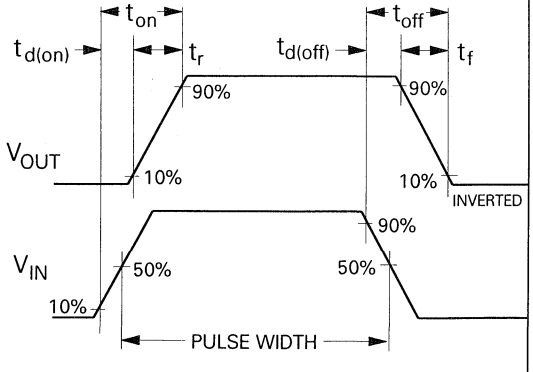


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

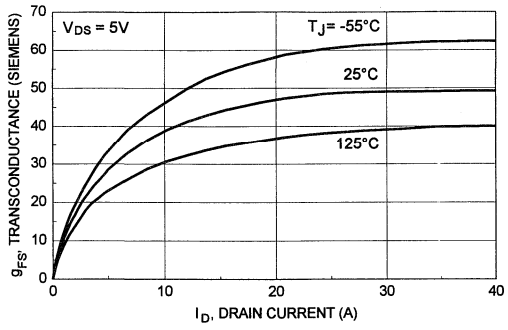


Figure 13. Transconductance Variation with Drain Current and Temperature

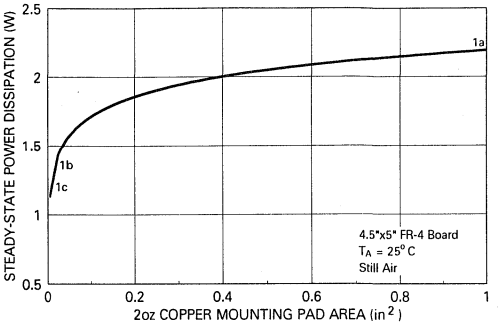


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

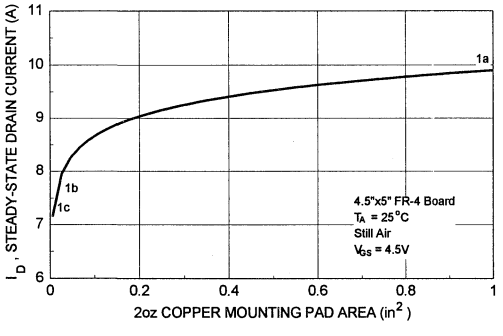


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

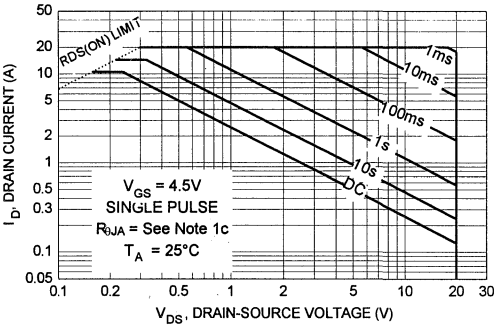


Figure 16. Maximum Safe Operating Area

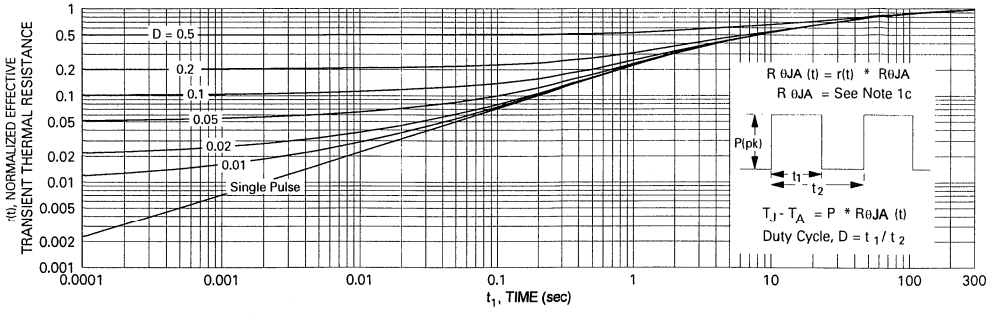


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

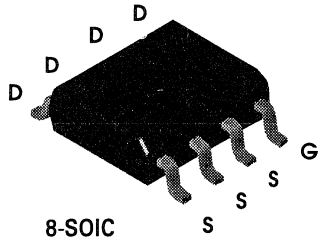
NDS8433
Single P-Channel Enhancement Mode Field Effect Transistor

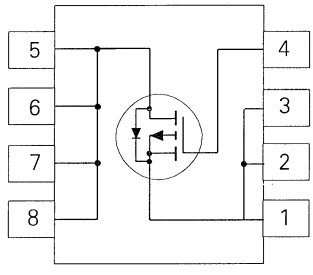
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -5.2A, -20V. $R_{DS(ON)}$ = 0.055Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.075Ω @ V_{GS} = -2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8433	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-8	V
I_D	Drain Current - Continuous	(Note 1a)	-5.2	A
	- Pulsed		-20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.8	-1	V
		T_J = 125°C	-0.3	-0.53	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -5.2 A		0.045	0.055	Ω
		T_J = 125°C		0.06	0.11	
		V_{GS} = -2.7 V, I_D = -4.6 A		0.062	0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-10			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-5			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -5.2 A		13		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1500		pF
C_{oss}	Output Capacitance			710		pF
C_{rss}	Reverse Transfer Capacitance			230		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω		16	30	ns
t_r	Turn - On Rise Time			41	60	ns
$t_{D(off)}$	Turn - Off Delay Time			100	150	ns
t_f	Turn - Off Fall Time			50	80	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -5.2 A, V_{GS} = -4.5 V		25	40	nC
Q_{gs}	Gate-Source Charge			3.6		nC
Q_{gd}	Gate-Drain Charge			7.6		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

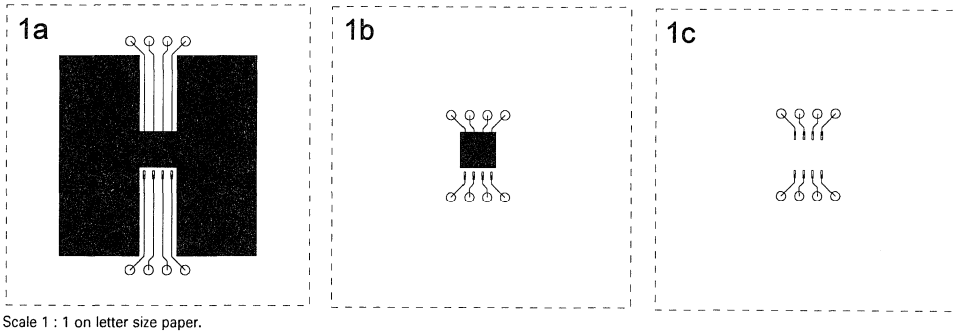
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

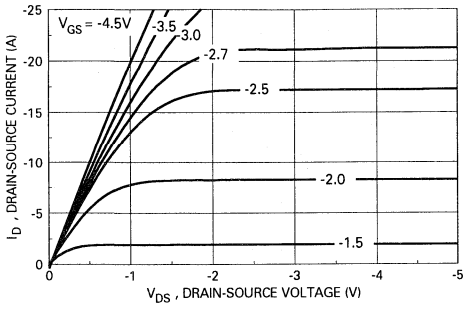


Figure 1. On-Region Characteristics

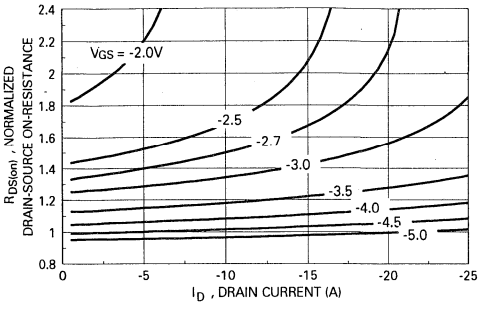


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

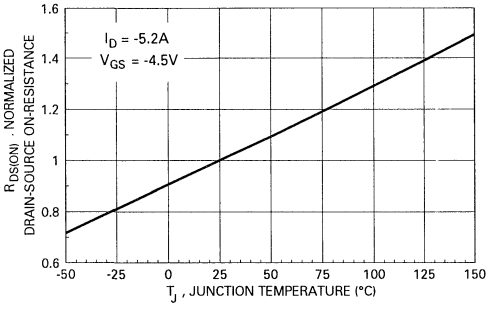


Figure 3. On-Resistance Variation with Temperature

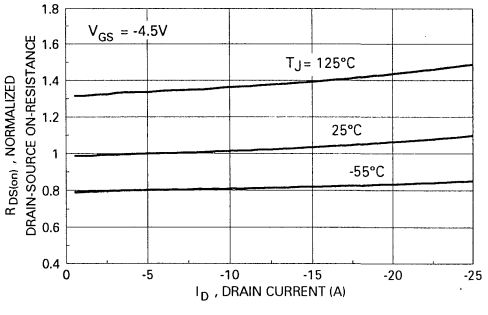


Figure 4. On-Resistance Variation with Drain Current and Temperature

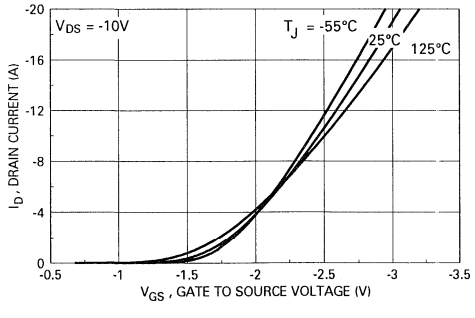


Figure 5. Transfer Characteristics

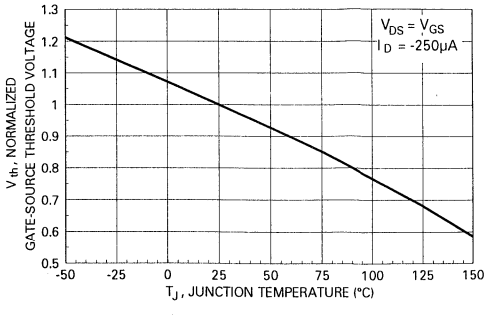


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

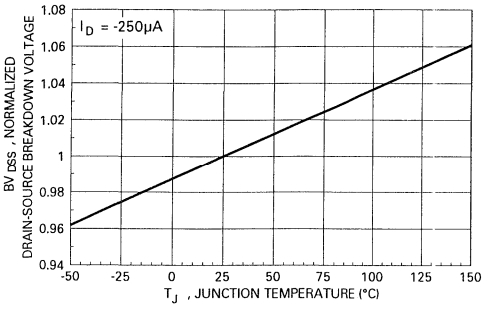


Figure 7. Breakdown Voltage Variation with Temperature

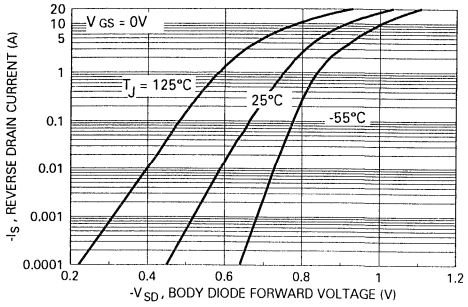


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

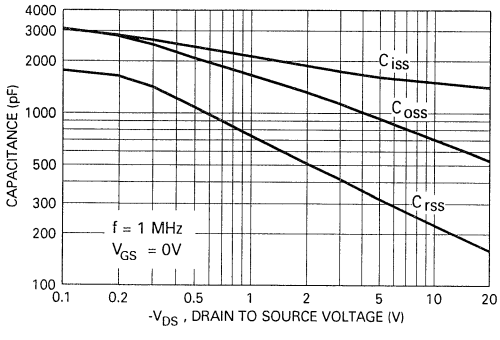


Figure 9. Capacitance Characteristics

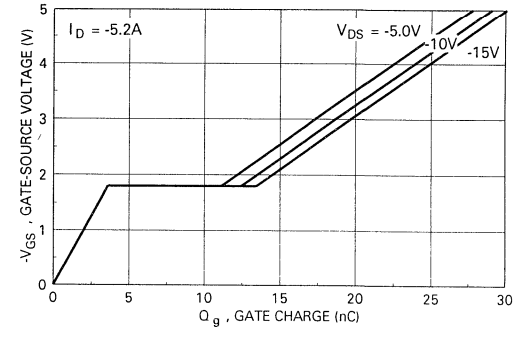


Figure 10. Gate Charge Characteristics

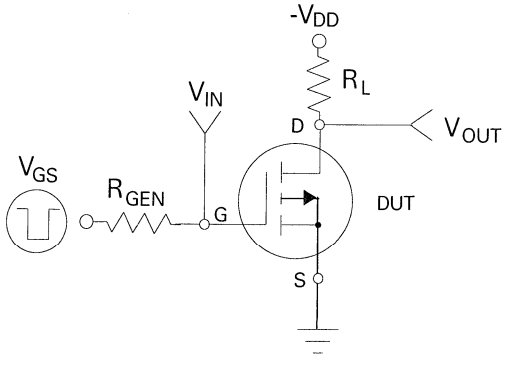


Figure 11. Switching Test Circuit

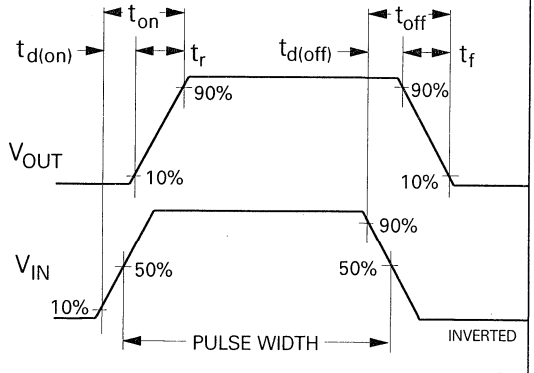


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

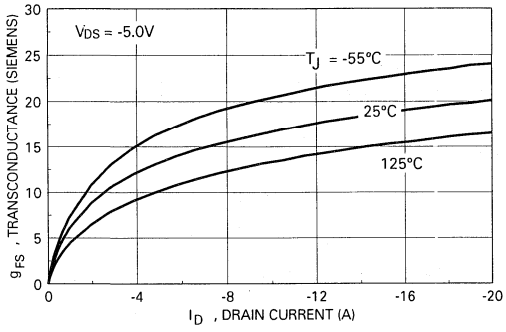


Figure 13. Transconductance Variation with Drain Current and Temperature

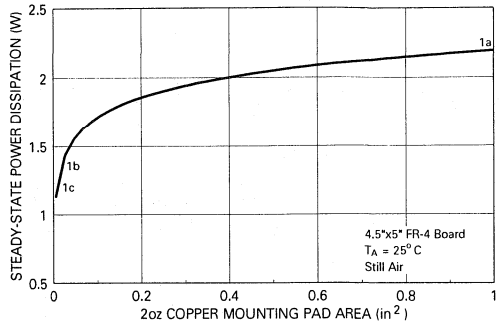


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

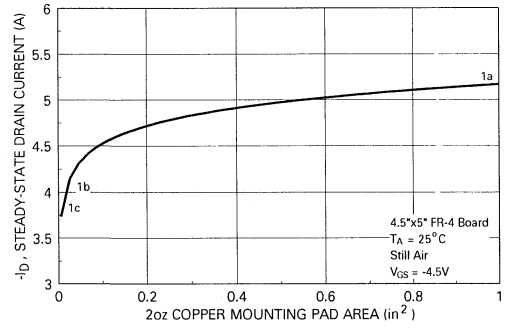


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

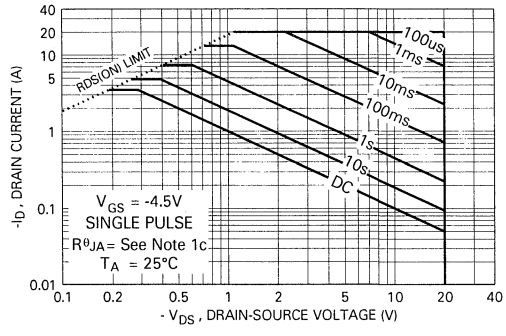


Figure 16. Maximum Safe Operating Area

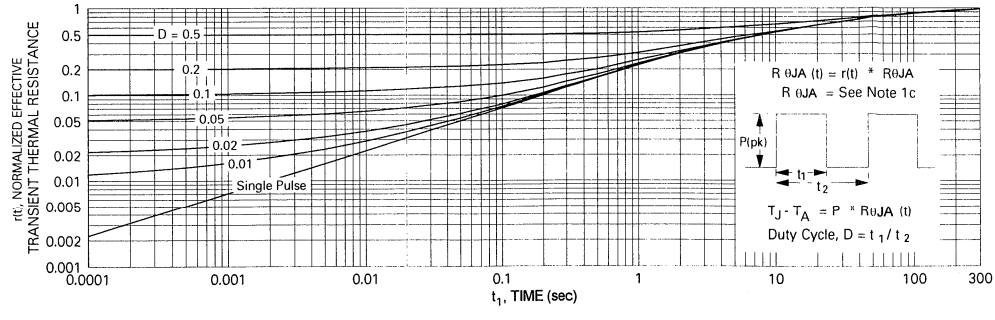


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

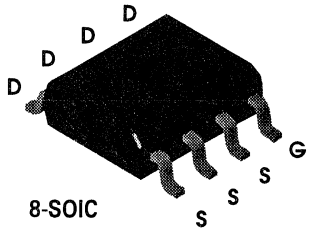
NDS8434
Single P-Channel Enhancement Mode Field Effect Transistor

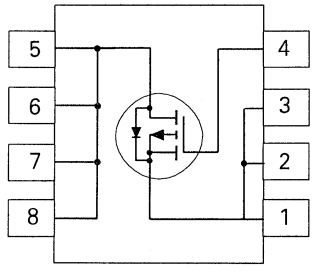
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -6.5A, -20V. $R_{DS(ON)}$ = 0.035Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.05Ω @ V_{GS} = -2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8434	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-8	V
I_D	Drain Current - Continuous	(Note 1a)	-6.5	A
	- Pulsed		-20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.7	-1	V
		T_J = 125°C	-0.3	-0.45	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -6.5 A		0.026	0.035	Ω
		T_J = 125°C		0.037	0.07	
		V_{GS} = -2.7 V, I_D = -5.5 A		0.036	0.05	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-15			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-10			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -6.5 A		18		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		2330		pF
C_{oss}	Output Capacitance			1070		pF
C_{rss}	Reverse Transfer Capacitance			360		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -6 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω		20	40	ns
t_r	Turn - On Rise Time			38	80	ns
$t_{D(off)}$	Turn - Off Delay Time			169	300	ns
t_f	Turn - Off Fall Time			63	120	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -6.5 A, V_{GS} = -4.5 V		40	80	nC
Q_{gs}	Gate-Source Charge			5.3		nC
Q_{gd}	Gate-Drain Charge			11		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

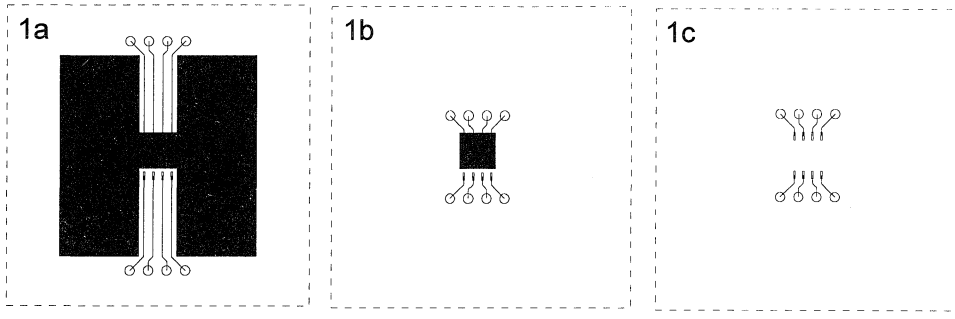
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

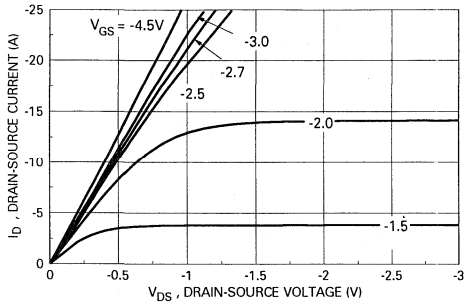


Figure 1. On-Region Characteristics

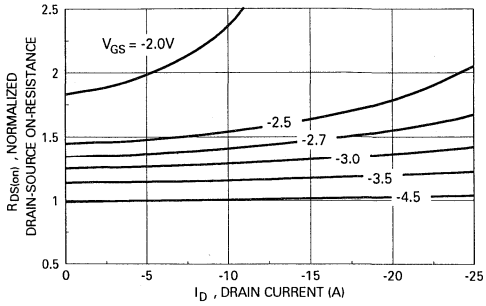


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

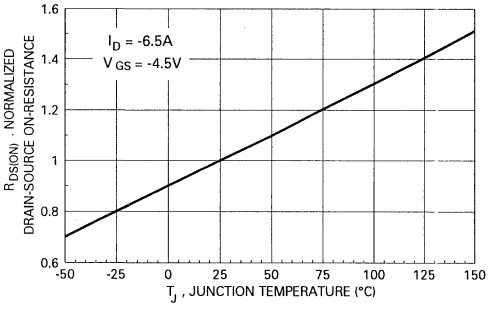


Figure 3. On-Resistance Variation with Temperature

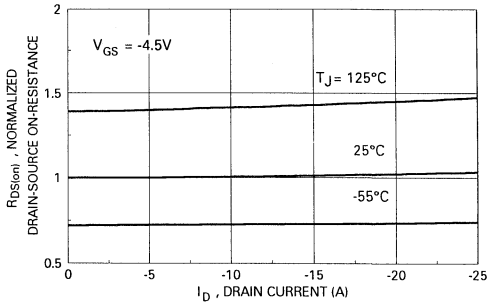


Figure 4. On-Resistance Variation with Drain Current and Temperature

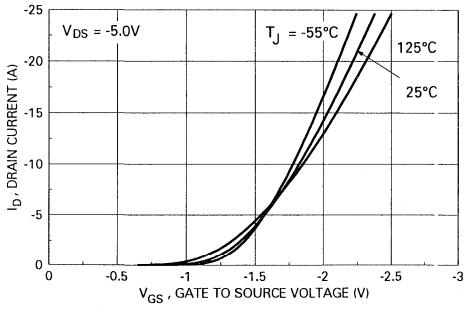


Figure 5. Transfer Characteristics

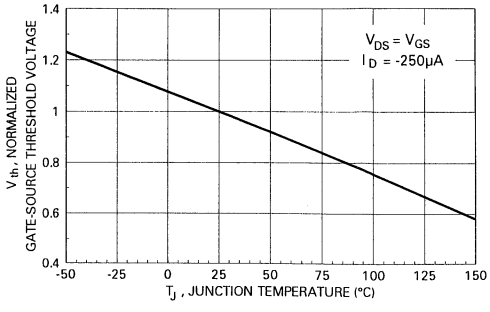


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

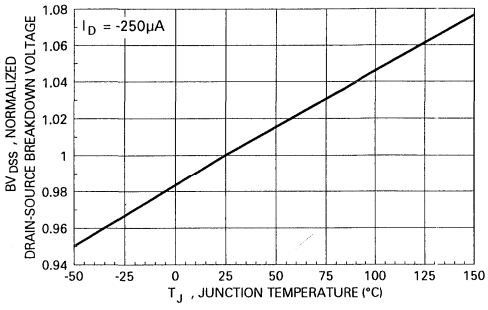


Figure 7. Breakdown Voltage Variation with Temperature

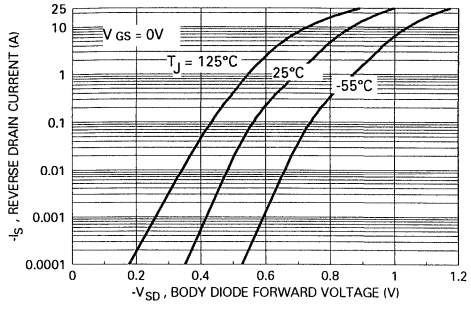


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

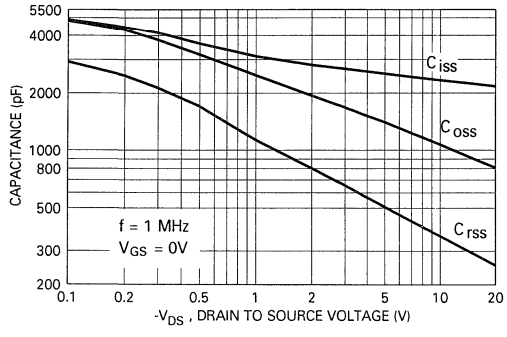


Figure 9. Capacitance Characteristics

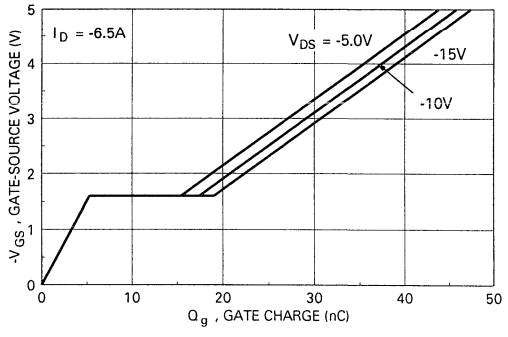


Figure 10. Gate Charge Characteristics

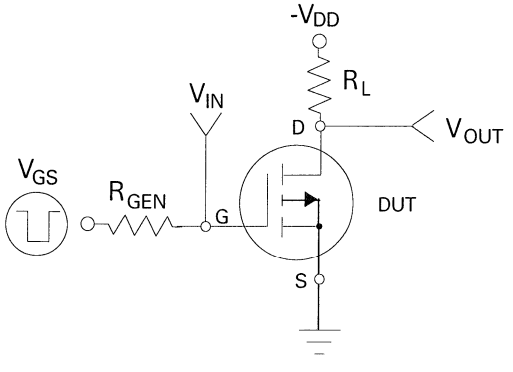


Figure 11. Switching Test Circuit

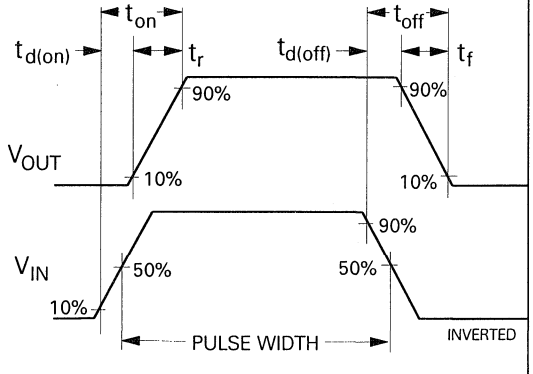


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

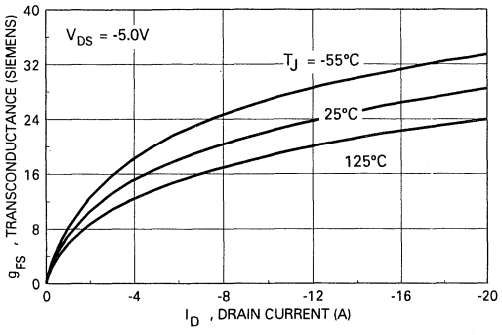


Figure 13. Transconductance Variation with Drain Current and Temperature

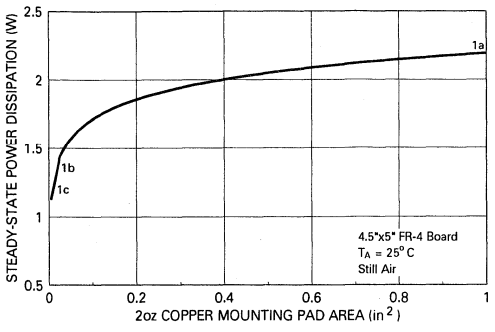


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

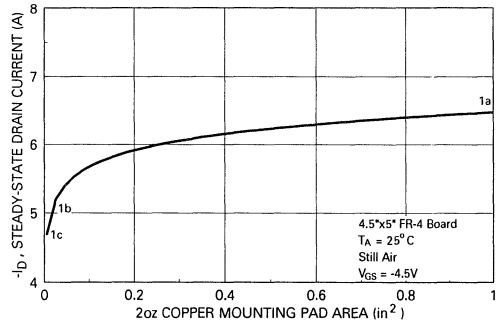


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

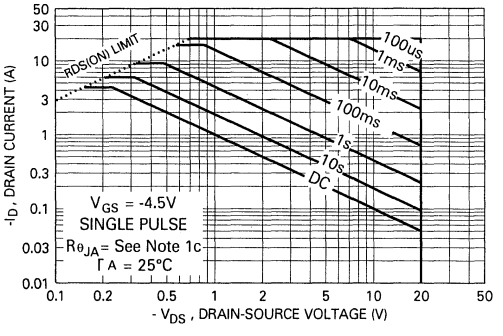


Figure 16. Maximum Safe Operating Area

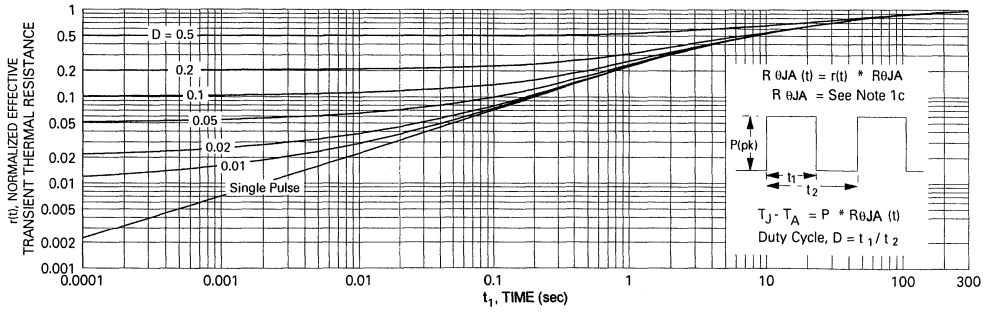


Figure 17. Transient Thermal Response Curve.

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May 1996

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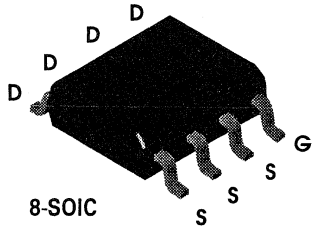
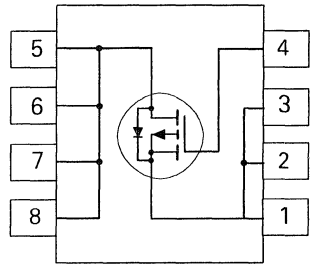
Features

- -7A, -30V. $R_{DS(ON)}$ = 0.028Ω @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.045Ω @ V_{GS} = -4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8435	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		-20	V
I_D	Drain Current - Continuous	(Note 1a)	-7	A
	- Pulsed		-25	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.5	-3	V
		T_J = 125°C	-0.7	-1.1	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -7.0 A		0.023	0.028	Ω
		T_J = 125°C		0.038	0.06	
		V_{GS} = -4.5 V, I_D = -5.8 A		0.037	0.045	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-25			A
		V_{GS} = -4.5, V_{DS} = -5 V	-10			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -7.0 A		10		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		1500		pF
C_{oss}	Output Capacitance			950		pF
C_{rss}	Reverse Transfer Capacitance			370		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		12	30	ns
t_r	Turn - On Rise Time			18	30	ns
$t_{D(off)}$	Turn - Off Delay Time			65	120	ns
t_f	Turn - Off Fall Time			49	80	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -7.0 A, V_{GS} = -10 V		47	60	nC
Q_{gs}	Gate-Source Charge			5.5		nC
Q_{gd}	Gate-Drain Charge			14		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		-0.8	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

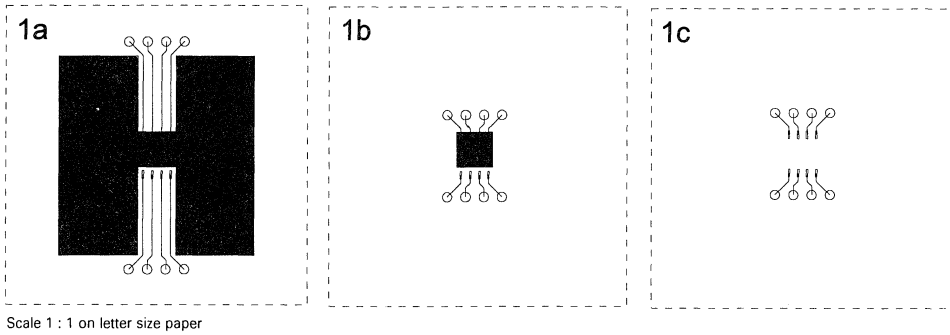
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

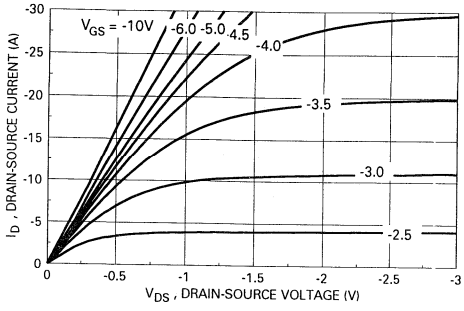


Figure 1. On-Region Characteristics

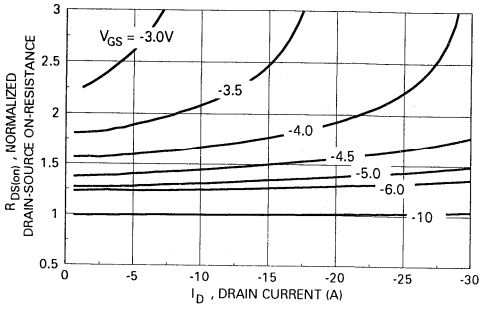


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

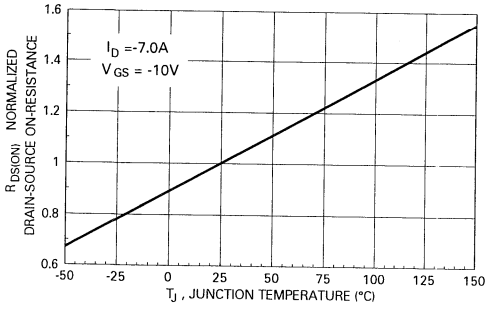


Figure 3. On-Resistance Variation with Temperature

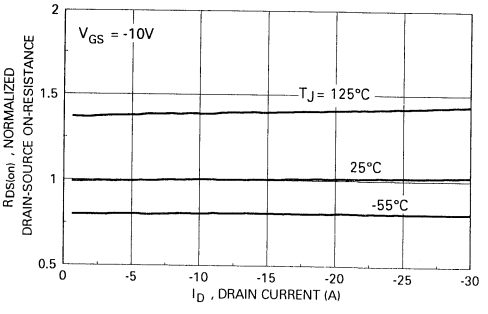


Figure 4. On-Resistance Variation with Drain Current and Temperature

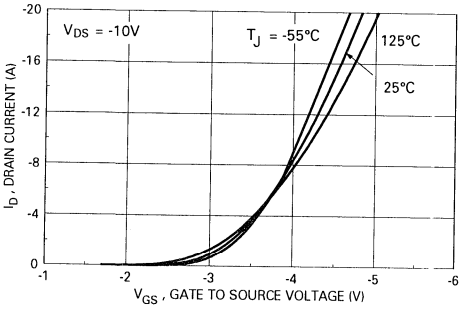


Figure 5. Transfer Characteristics

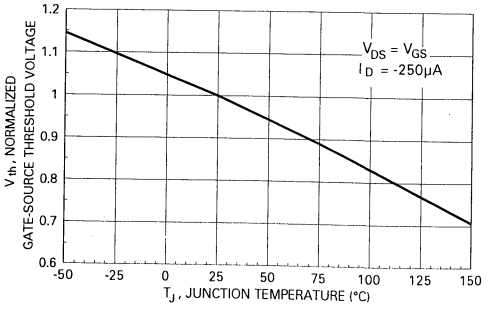


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

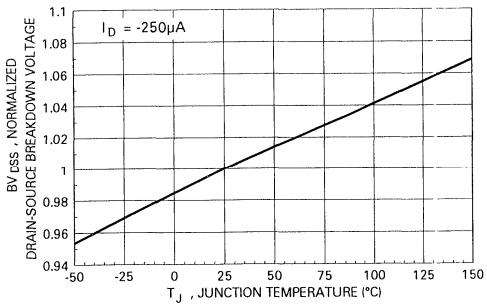


Figure 7. Breakdown Voltage Variation with Temperature

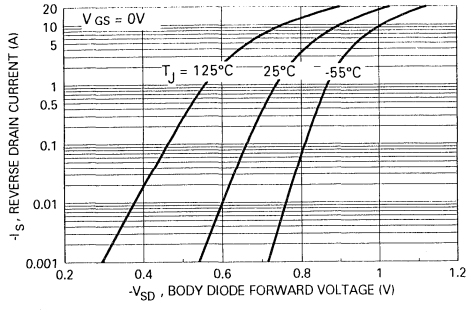


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

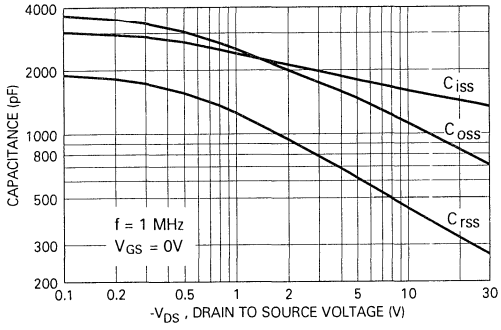


Figure 9. Capacitance Characteristics

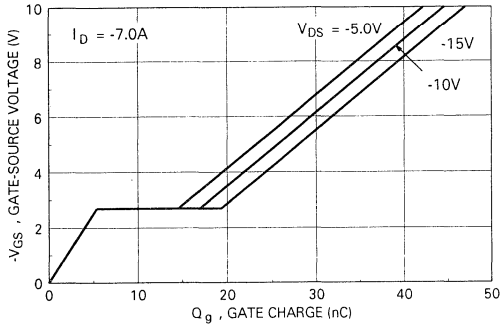


Figure 10. Gate Charge Characteristics

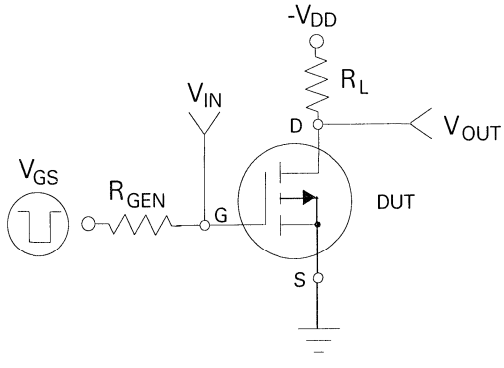


Figure 11. Switching Test Circuit

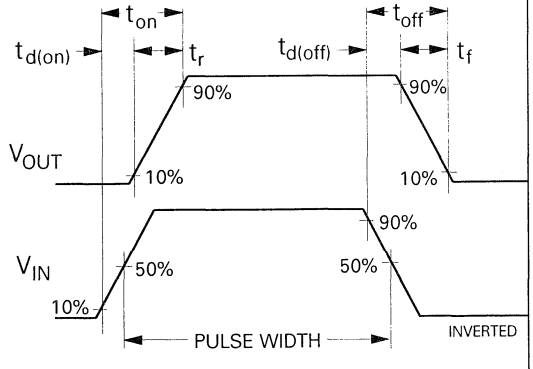


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

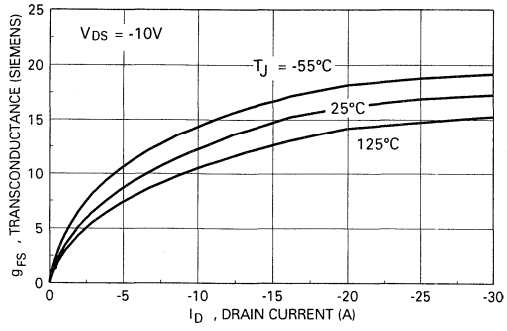


Figure 13. Tranconductance Variation with Drain Current and Temperature

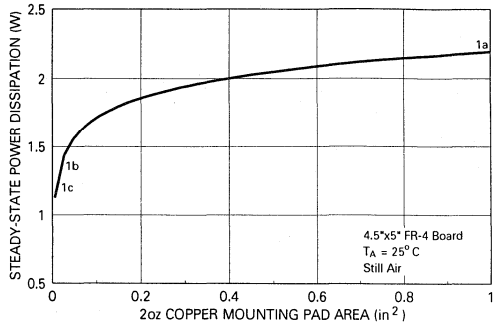


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

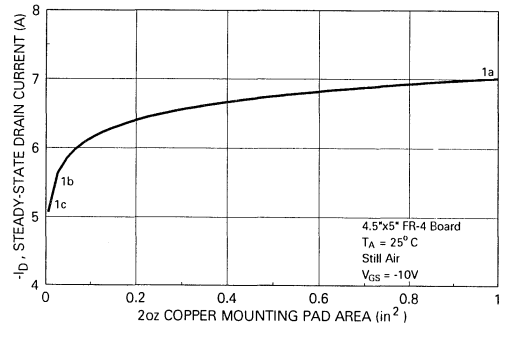


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

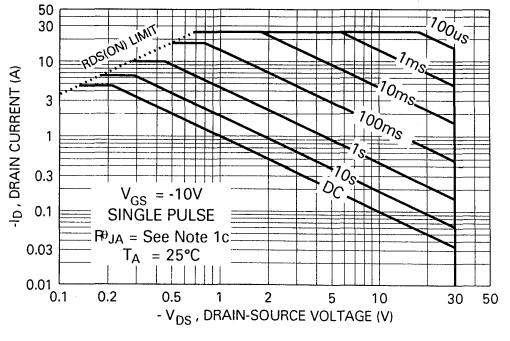


Figure 16. Maximum Safe Operating Area

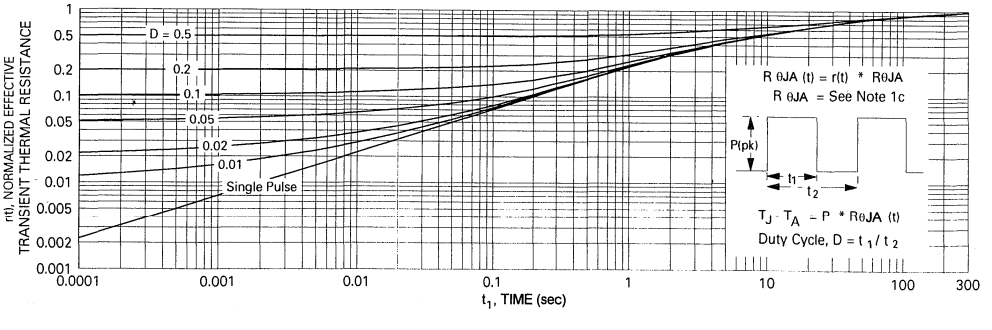


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

March 1996

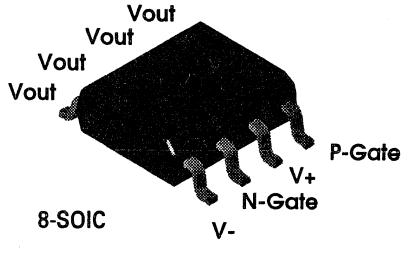
NDS8839H
Complementary MOSFET Half Bridge

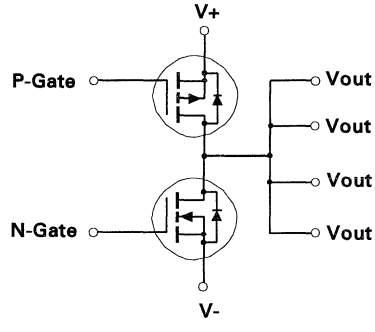
General Description

These Complementary MOSFET half bridge devices are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage half bridge applications or CMOS applications when both gates are connected together.

Features

- N-Channel 5.7A, 30V, $R_{DS(ON)}$=0.045Ω @ V_{GS}=10V.
  P-Channel -4.0A, -30V, $R_{DS(ON)}$=0.09Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Matched pair for equal input capacitance and power capability .





Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		20	-20	V
I_D	Drain Current - Continuous	(Note 1a & 2)	5.7	-4	A
	- Pulsed		15	15	
P_D	Maximum Power Dissipation	(Note 1a)	2.5		W
	(Single Device)	(Note 1b)	1.2		
		(Note 1c)	1		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Single Device)	(Note 1a)	50		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Single Device)	(Note 1)	25		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 55°C				10	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-1	µA
		T_J = 55°C				-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 3)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.6	2.8	V
		T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.6	-2.8	
		T_J = 125°C		-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.0 A	N-Ch		0.04	0.045	Ω
		T_J = 125°C			0.055	0.09	
		V_{GS} = 4.5 V, I_D = 3.2 A			0.053	0.075	
		V_{GS} = -10 V, I_D = -4.0 A	P-Ch		0.066	0.09	
		T_J = 125°C			0.092	0.18	
		V_{GS} = -4.5 V, I_D = -3.2 A			0.1	0.15	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	20			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-20			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.0 A	N-Ch		10		S
		V_{DS} = -10 V, I_D = -4.0 A	P-Ch		7		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		720		pF
			P-Ch		690		
C_{oss}	Output Capacitance	P-Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		370		pF
			P-Ch		430		
C_{rss}	Reverse Transfer Capacitance		N-Ch		250		pF
			P-Ch		160		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	N-Ch		12	20	ns
			P-Ch		9	20	
t_r	Turn - On Rise Time		N-Ch		13	30	ns
			P-Ch		20	25	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		29	50	ns
			P-Ch		40	50	
t_f	Turn - Off Fall Time		N-Ch		10	20	ns
			P-Ch		19	40	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 4.0 A, V_{GS} = 10 V P-Channel V_{DS} = -10 V, I_D = -4.0 A, V_{GS} = -10 V	N-Ch		19	30	nC
			P-Ch		21	30	
Q_{gs}	Gate-Source Charge		N-Ch		2.1		nC
			P-Ch		3.1		
Q_{gd}	Gate-Drain Charge		N-Ch		5.2		nC
			P-Ch		5.1		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			2	A
			P-Ch			-2	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 2)	N-Ch		0.9	1.2	V
		V_{GS} = 0 V, I_S = -2.0 A (Note 2)	P-Ch		-0.85	-1.2	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 2.0 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
		P-Channel V_{GS} = 0 V, I_F = -2.0 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

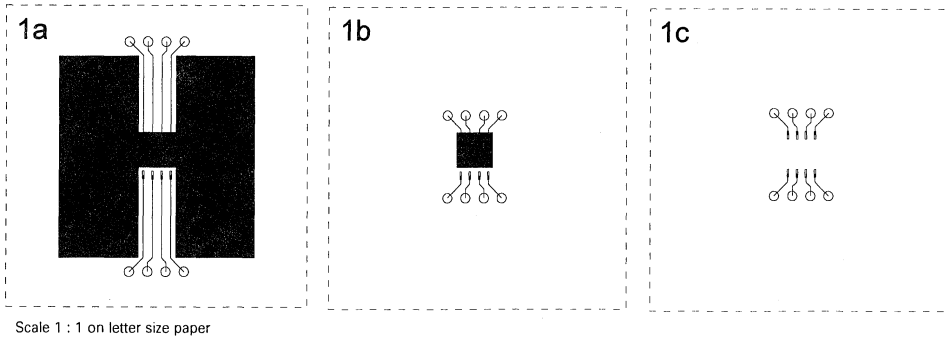
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

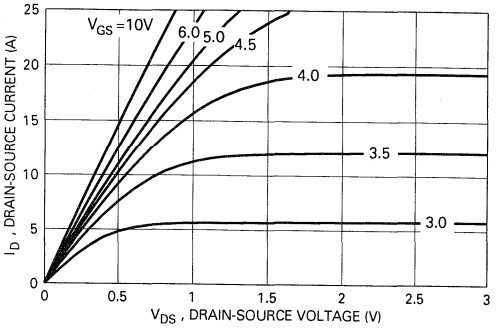


Figure 1. N-Channel On-Region Characteristics.

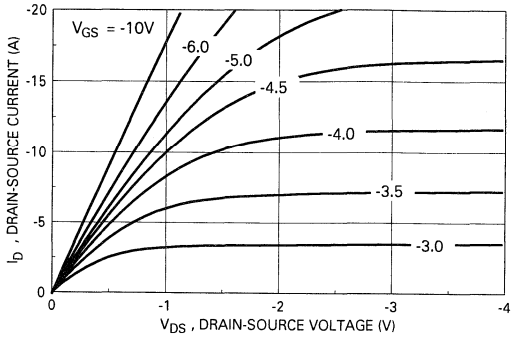


Figure 2. P-Channel On-Region Characteristics.

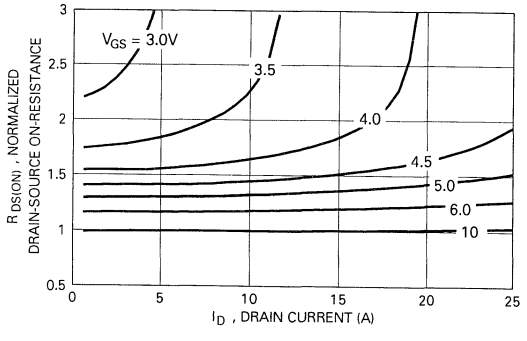


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

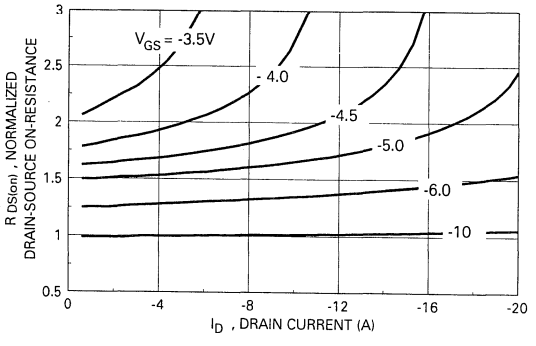


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

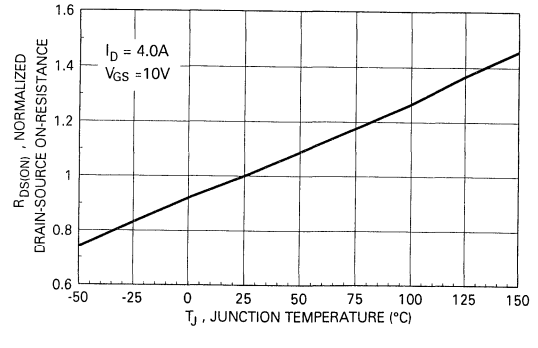


Figure 5. N-Channel On-Resistance Variation with Temperature.

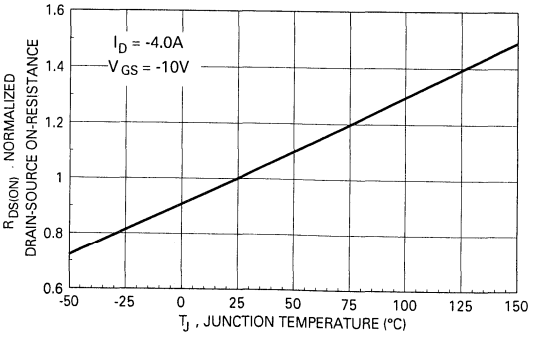


Figure 6. P-Channel On-Resistance Variation with Temperature.

4

Typical Electrical Characteristics

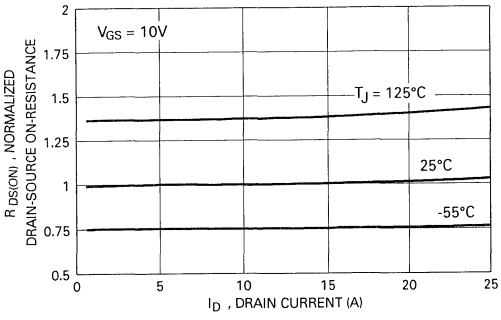


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

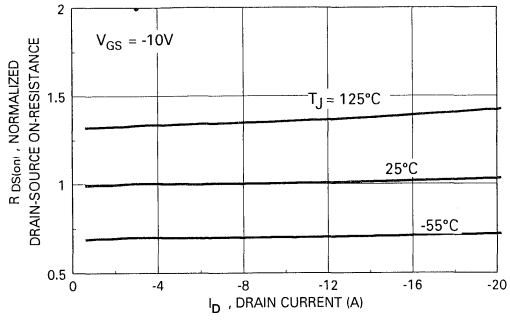


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

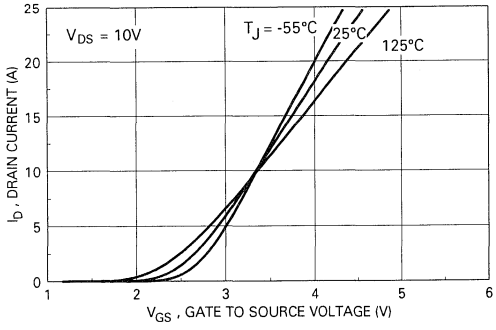


Figure 9. N-Channel Transfer Characteristics.

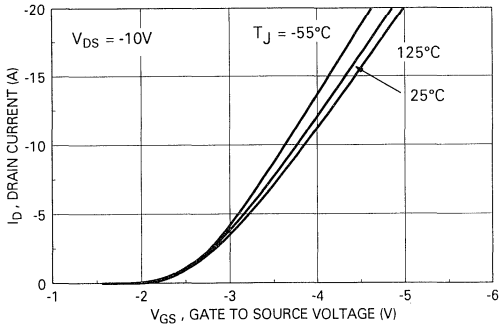


Figure 10. P-Channel Transfer Characteristics.

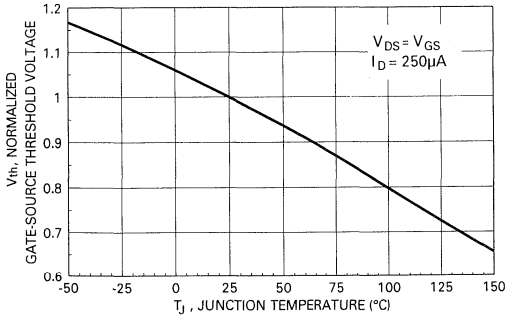


Figure 11. N-Channel Gate Threshold Variation with Temperature.

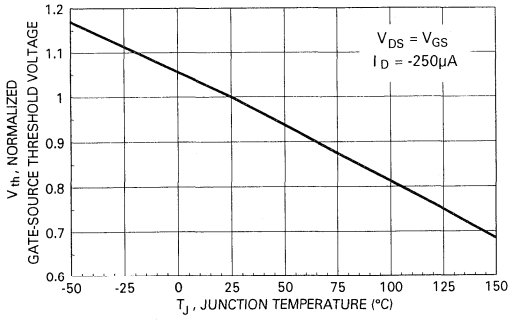


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

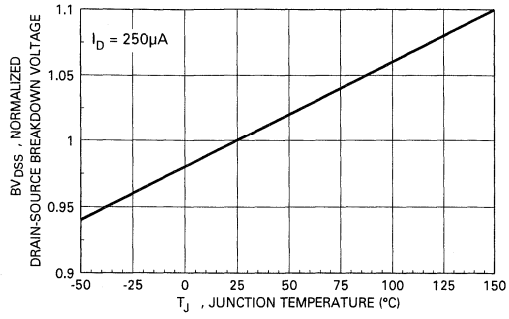


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

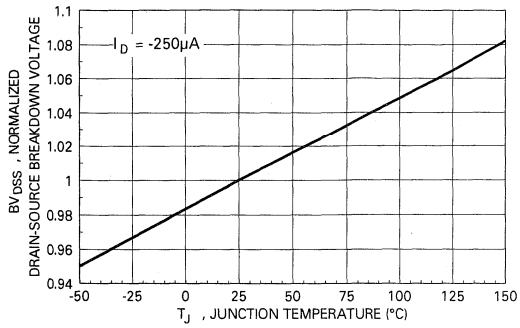


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

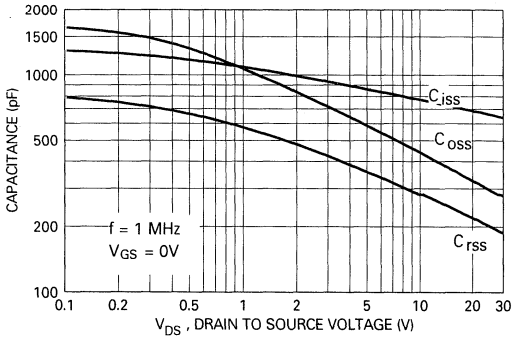


Figure 15. N-Channel Capacitance Characteristics.

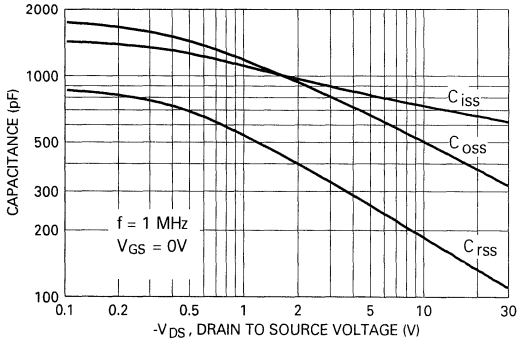


Figure 16. P-Channel Capacitance Characteristics.

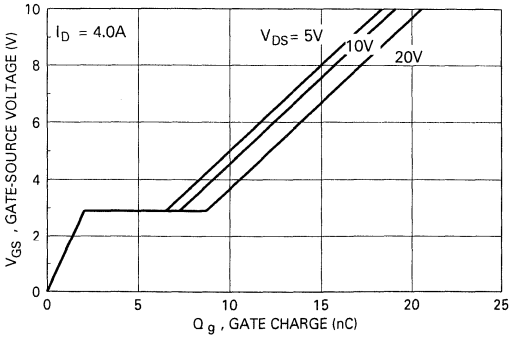


Figure 17. N-Channel Gate Charge Characteristics.

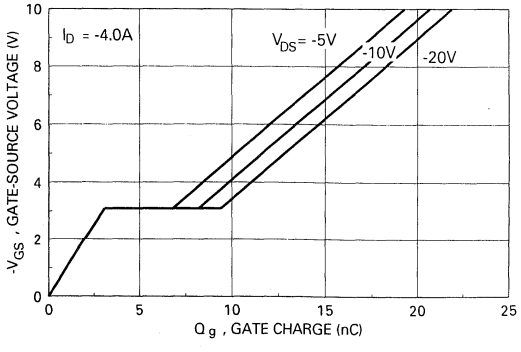


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical and Thermal Characteristics

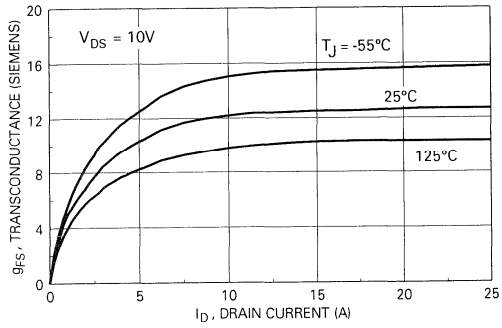


Figure 19. N-Channel Transconductance Variation with Drain Current and Temperature.

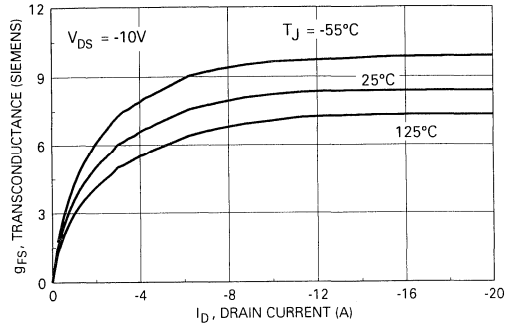


Figure 20. P-Channel Transconductance Variation with Drain Current and Temperature.

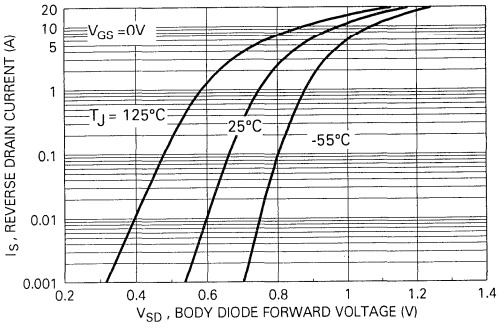


Figure 21. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

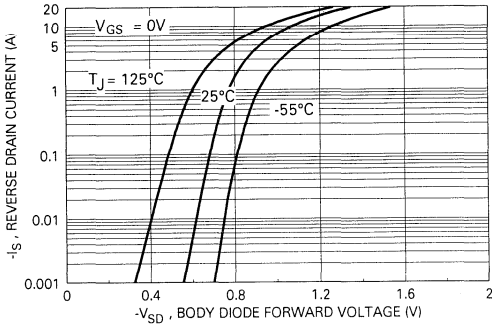


Figure 22. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

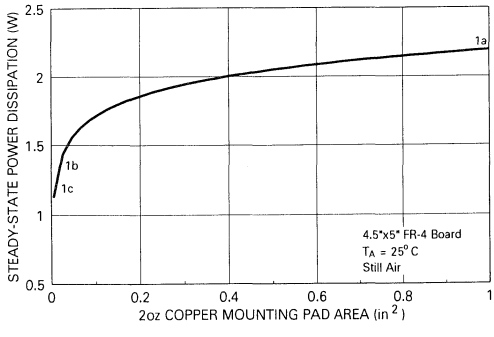


Figure 23. SO-8 Single Device DC Power Dissipation versus Copper Mounting Pad Area.

Typical Thermal Characteristics

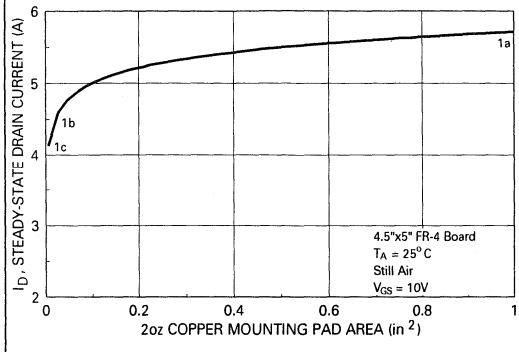


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

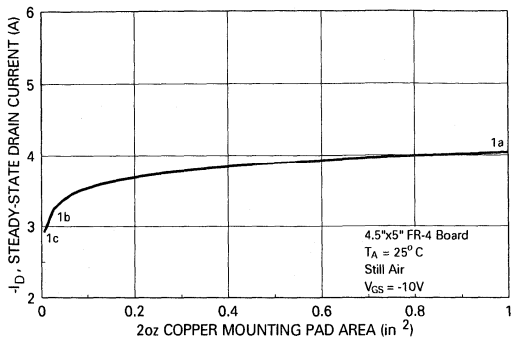


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

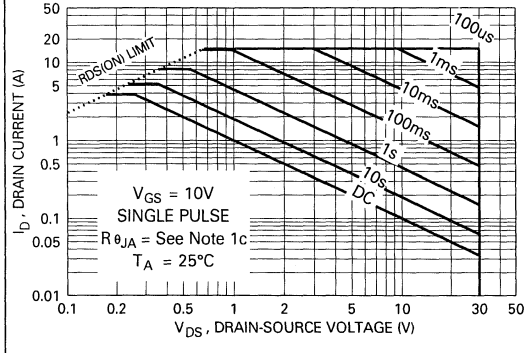


Figure 26. N-Ch Maximum Safe Operating Area.

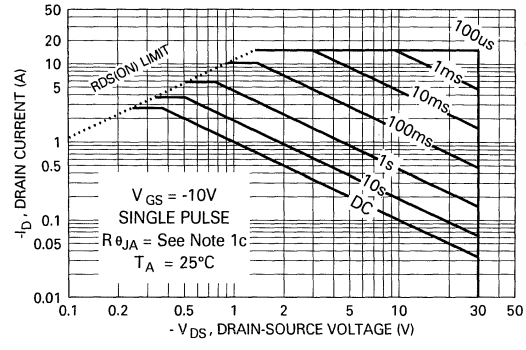


Figure 27. P-Ch Maximum Safe Operating Area.

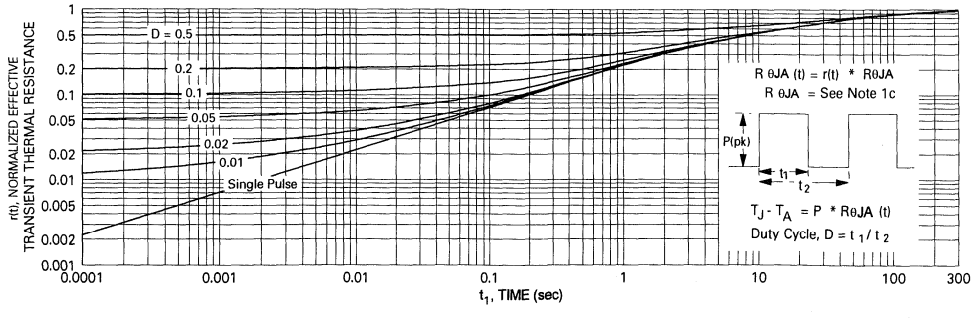


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

February 1996

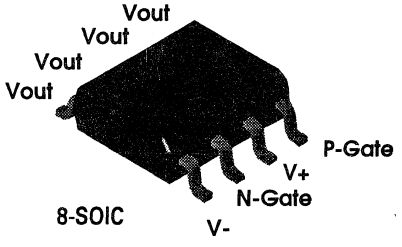
NDS8852H
Complementary MOSFET Half Bridge

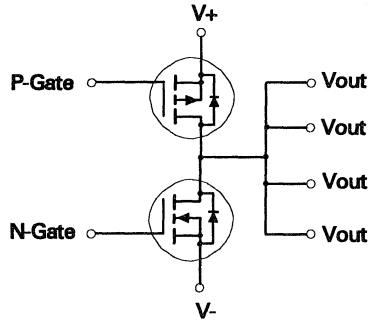
General Description

These Complementary MOSFET half bridge devices are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage half bridge applications or CMOS applications when both gates are connected together.

Features

- N-Channel 4.3A, 30V, $R_{DS(ON)}$=0.08Ω @ V_{GS}=10V. P-Channel -3.4A, -30V, $R_{DS(ON)}$=0.13Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Matched pair for equal input capacitance and power capability .





Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	30	-30	V
V_{GSS}	Gate-Source Voltage	20	-20	V
I_D	Drain Current - Continuous (Note 1a & 2)	4.3	-3.4	A
	- Pulsed	15	-10	
P_D	Maximum Power Dissipation (Note 1a)	2.5		W
	(Single Device) (Note 1b)	1.2		
	(Note 1c)	1		
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Single Device) (Note 1a)	50		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Single Device) (Note 1)	25		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			2	µA
		T_J = 55°C				25	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_J = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 3)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.7	2.8	V
		T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.6	-2.8	
		T_J = 125°C		-0.85	-1.25	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.4 A	N-Ch		0.06	0.08	Ω
		T_J = 125°C			0.08	0.13	
		V_{GS} = 4.5 V, I_D = 2.8 A			0.08	0.11	
		V_{GS} = -10 V, I_D = -3.4 A	P-Ch		0.11	0.13	
		T_J = 125°C			0.15	0.21	
		V_{GS} = -4.5 V, I_D = -2.8 A			0.17	0.2	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.4 A	N-Ch		6		S
		V_{DS} = -15 V, I_D = -3.4 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		300		pF
			P-Ch		330		
C_{oss}	Output Capacitance	P-Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		190		pF
			P-Ch		190		
C_{rss}	Reverse Transfer Capacitance		N-Ch		70		pF
			P-Ch		70		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 3)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t_r	Turn - On Rise Time		N-Ch		13	20	ns
			P-Ch		21	40	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		21	50	ns
			P-Ch		21	90	
t_f	Turn - Off Fall Time		N-Ch		5	50	ns
			P-Ch		8	50	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 3.4 A, V_{GS} = 10 V P-Channel V_{DS} = -10 V, I_D = -3.4 A, V_{GS} = -10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q_{gs}	Gate-Source Charge		N-Ch		1.5		nC
			P-Ch		1.6		
Q_{gd}	Gate-Drain Charge		N-Ch		2.6		nC
			P-Ch		2.7		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			2.1	A
			P-Ch			-2.1	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -2.1 A (Note 2)	P-Ch		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 2.1 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
		P-Channel V_{GS} = 0 V, I_F = -2.1 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

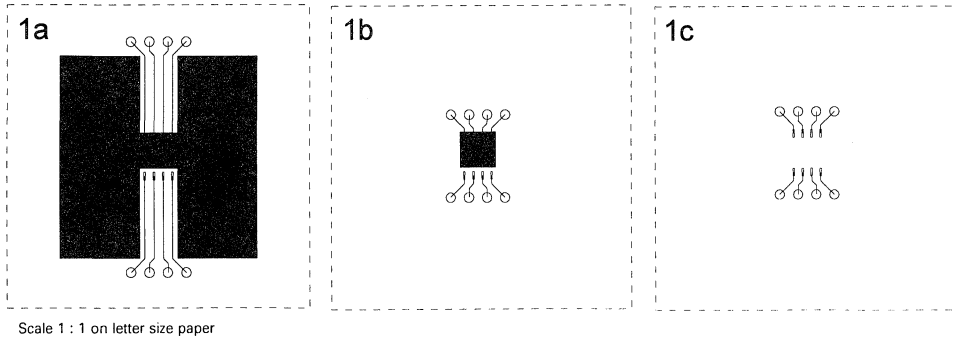
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

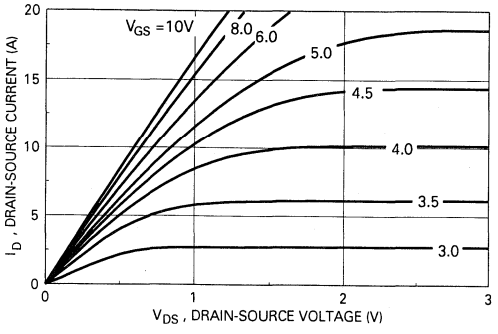


Figure 1. N-Channel On-Region Characteristics.

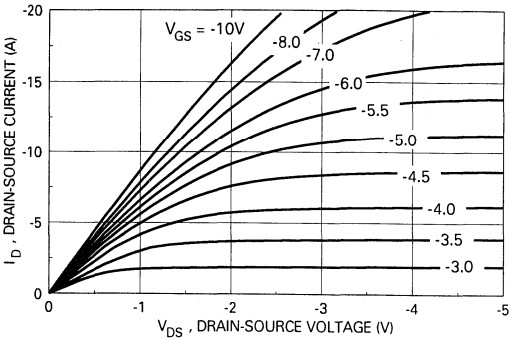


Figure 2. P-Channel On-Region Characteristics.

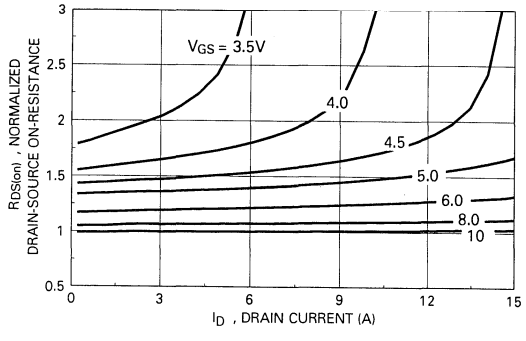


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

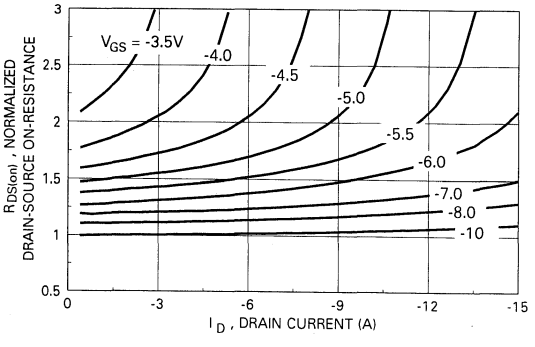


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

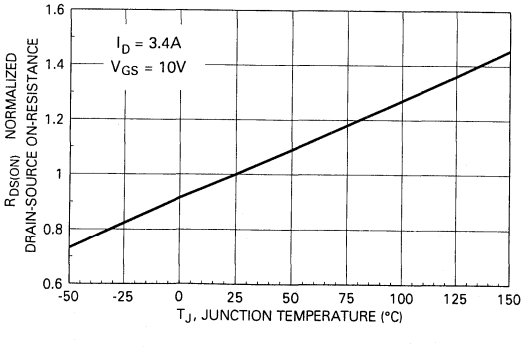


Figure 5. N-Channel On-Resistance Variation with Temperature.

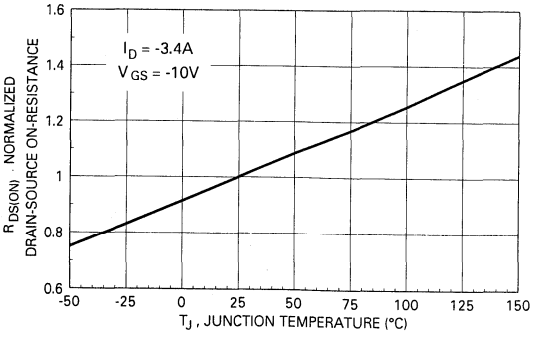


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

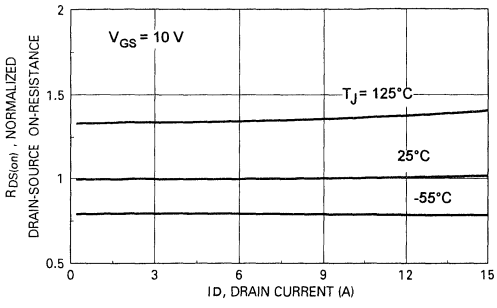


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

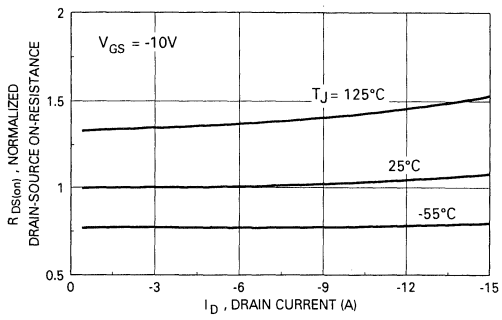


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

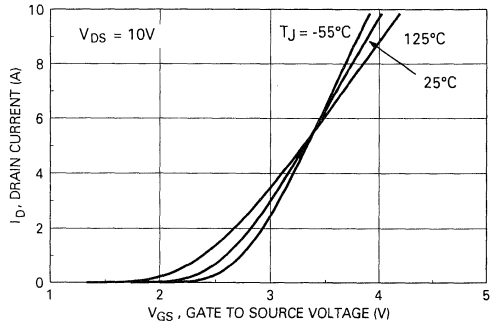


Figure 9. N-Channel Transfer Characteristics.

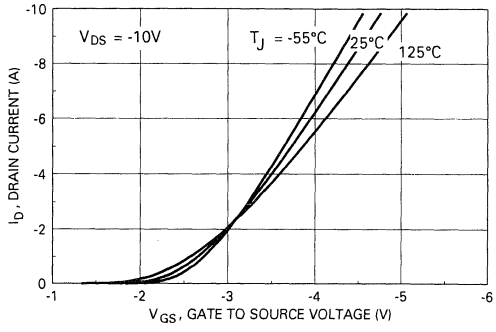


Figure 10. P-Channel Transfer Characteristics.

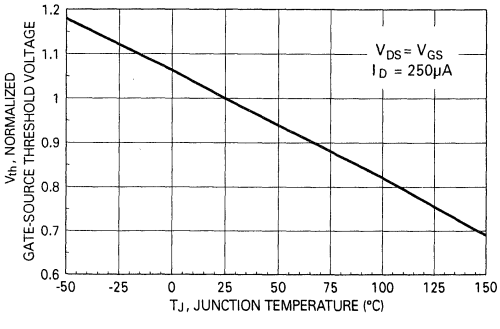


Figure 11. N-Channel Gate Threshold Variation with Temperature.

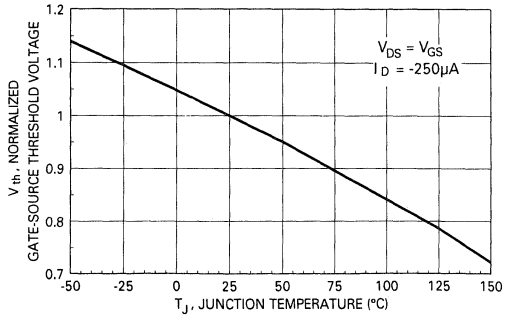


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

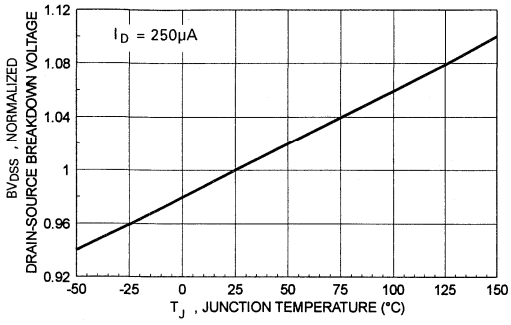


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

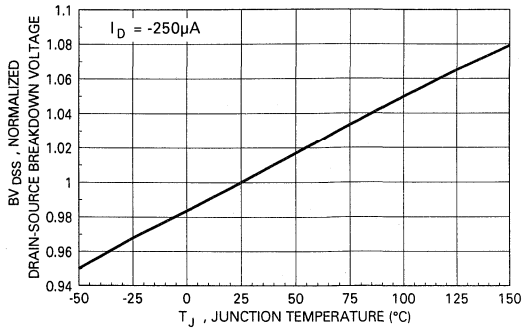


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

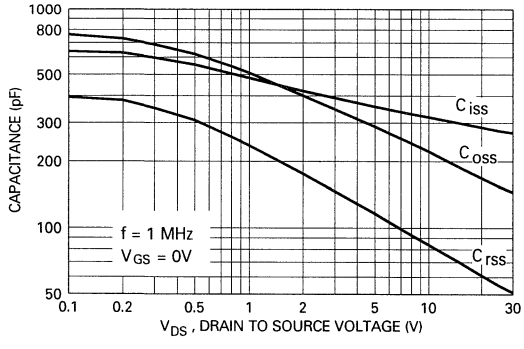


Figure 15. N-Channel Capacitance Characteristics.

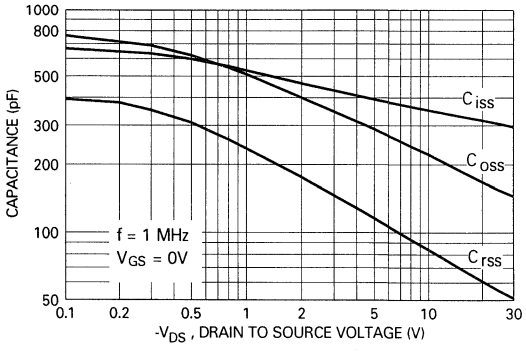


Figure 16. P-Channel Capacitance Characteristics.

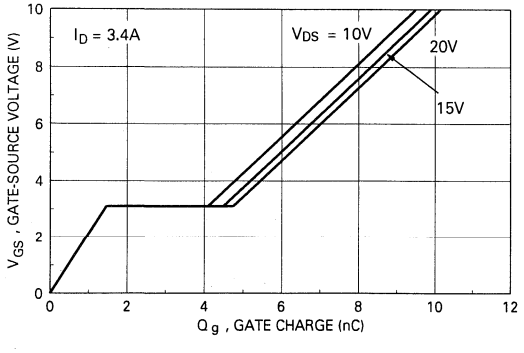


Figure 17. N-Channel Gate Charge Characteristics.

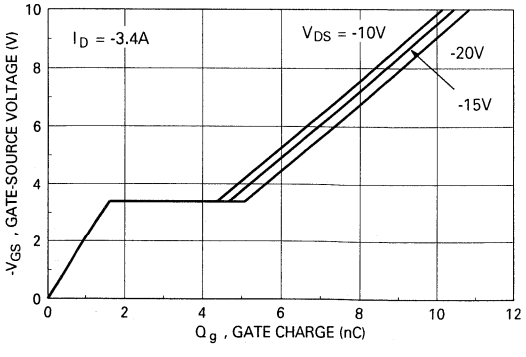


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical and Thermal Characteristics

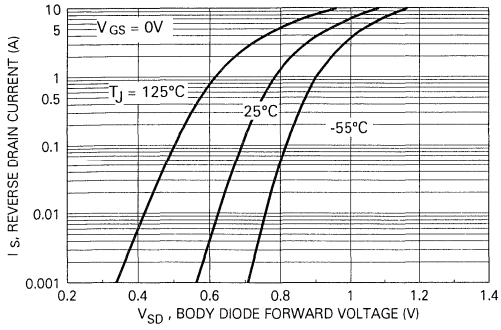


Figure 19. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

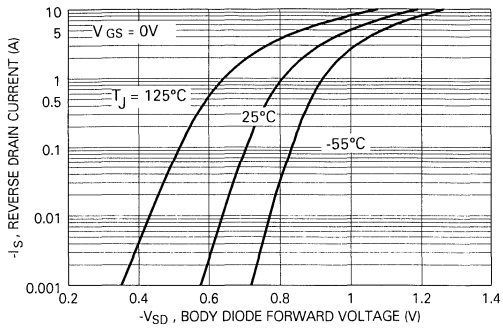


Figure 20. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

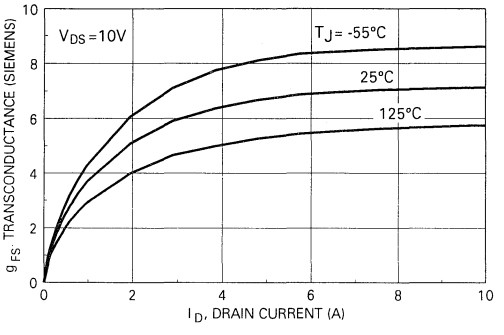


Figure 21. N-Channel Transconductance Variation with Drain Current and Temperature.

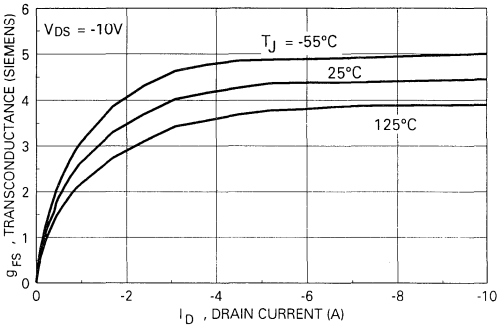


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

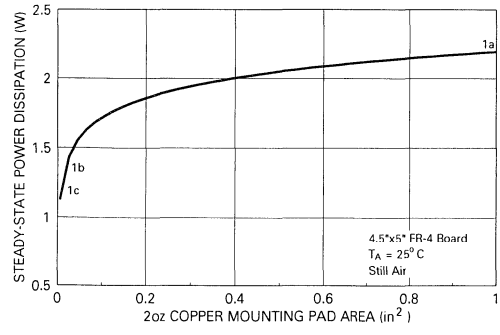


Figure 23. SO-8 Single Device DC Power Dissipation versus Copper Mounting Pad Area.

Typical Thermal Characteristics

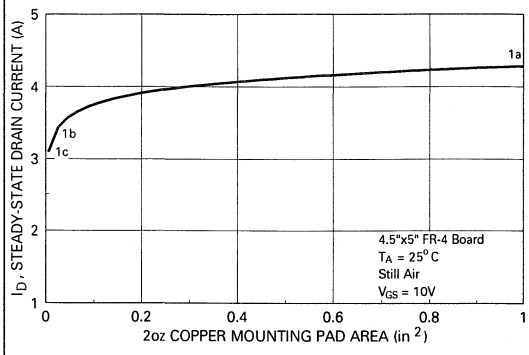


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

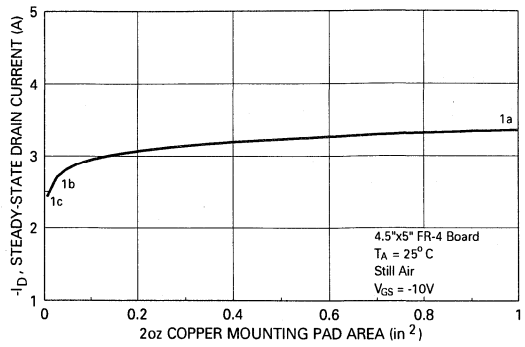


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

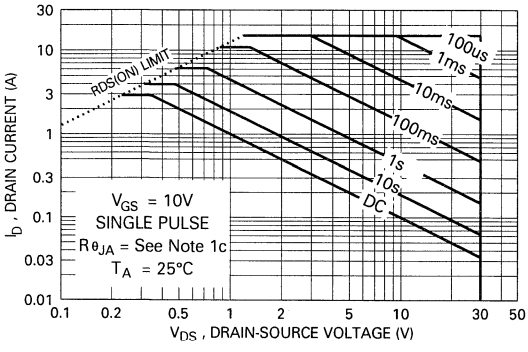


Figure 26. N-Ch Maximum Safe Operating Area.

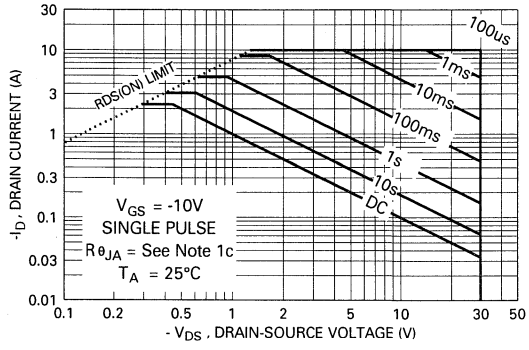


Figure 27. P-Ch Maximum Safe Operating Area.

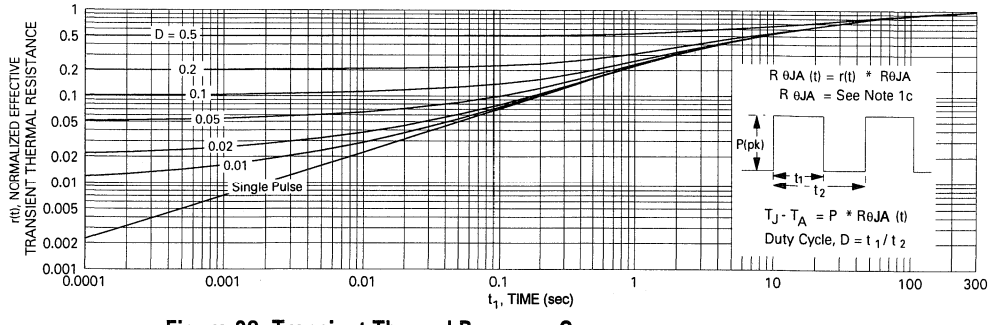


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

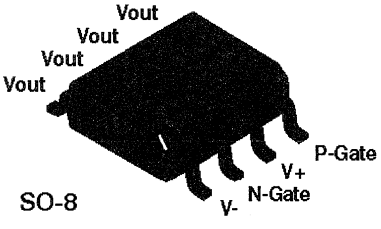
NDS8858H
Complementary MOSFET Half Bridge

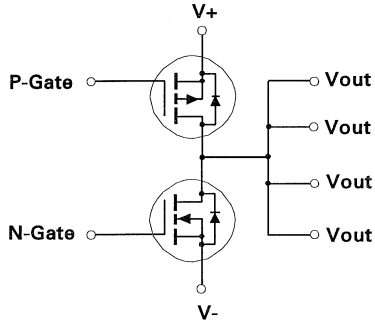
General Description

These Complementary MOSFET half bridge devices are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage half bridge applications or CMOS applications when both gates are connected together.

Features

- N-Channel 6.3A, 30V, $R_{DS(ON)}$=0.035Ω @ V_{GS}=10V.
  P-Channel -4.8A, -30V, $R_{DS(ON)}$=0.065Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Matched pair for equal input capacitance and power capability .





Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		20	-20	V
I_D	Drain Current - Continuous	(Note 1a & 2)	6.3	-4.8	A
	- Pulsed		20	20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5		W
	(Single Device)	(Note 1b)	1.2		
		(Note 1c)	1		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Single Device)	(Note 1a)	50		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Single Device)	(Note 1a)	25		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 55°C				10	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-1	µA
		T_J = 55°C				-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V	All			-100	nA
ON CHARACTERISTICS (Note 3)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.6	2.8	V
		T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.6	-2.8	
		T_J = 125°C		-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.8 A	N-Ch		0.033	0.035	Ω
		T_J = 125°C			0.046	0.063	
		V_{GS} = 4.5 V, I_D = 3.7 A			0.046	0.05	
		V_{GS} = -10 V, I_D = -4.8 A	P-Ch		0.052	0.065	
		T_J = 125°C			0.075	0.13	
		V_{GS} = -4.5 V, I_D = -3.7 A			0.085	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	20			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-20			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.8 A	N-Ch		10		S
		V_{DS} = -10 V, I_D = -4.8 A	P-Ch		7		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		720		pF
			P-Ch		690		
C_{oss}	Output Capacitance		N-Ch		370		pF
		P-Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		430		
C_{rss}	Reverse Transfer Capacitance		N-Ch		250		pF
			P-Ch		160		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		12	20	ns
			P-Ch		9	20	
t_r	Turn - On Rise Time		N-Ch		13	30	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		20	25	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		29	50	ns
			P-Ch		40	50	
t_f	Turn - Off Fall Time		N-Ch		10	20	ns
			P-Ch		19	40	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 4.8 A, V_{GS} = 10 V	N-Ch		19	30	nC
			P-Ch		21	30	
Q_{gs}	Gate-Source Charge		N-Ch		2.1		nC
		P-Channel V_{DS} = -10 V, I_D = -4.8 A, V_{GS} = -10 V	P-Ch		3.2		
Q_{gd}	Gate-Drain Charge		N-Ch		5.2		nC
			P-Ch		5.2		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			2	A
			P-Ch			-2	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.0 A (Note 2)	N-Ch		0.9	1.2	V
		V_{GS} = 0 V, I_S = -2.0 A (Note 2)	P-Ch		-0.85	-1.2	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 2.0 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
		P-Channel V_{GS} = 0 V, I_F = -2.0 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

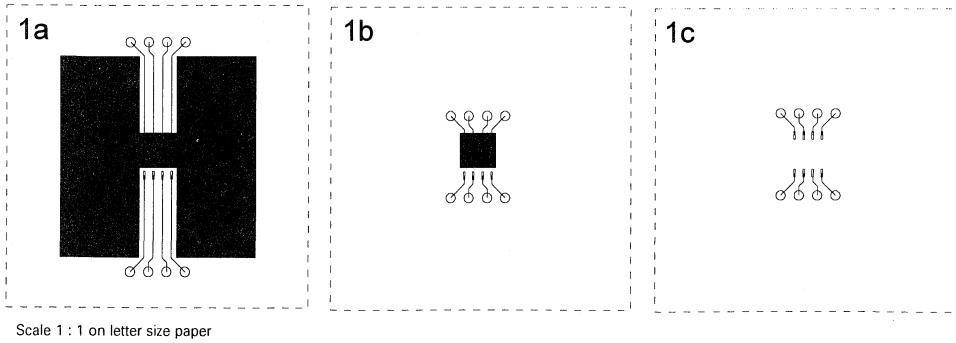
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

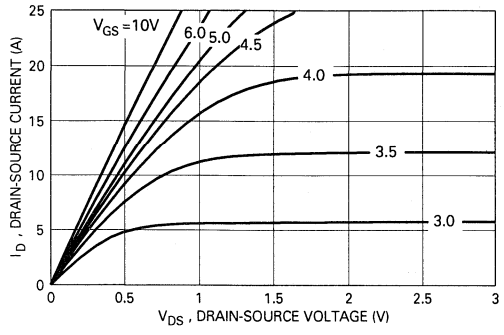


Figure 1. N-Channel On-Region Characteristics.

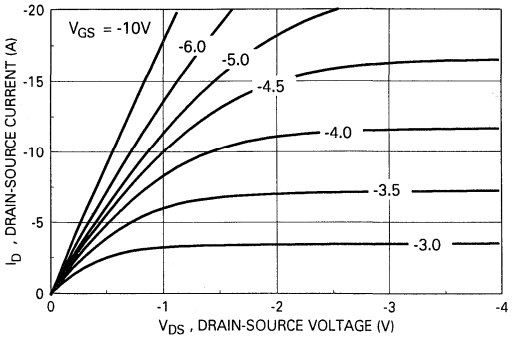


Figure 2. P-Channel On-Region Characteristics.

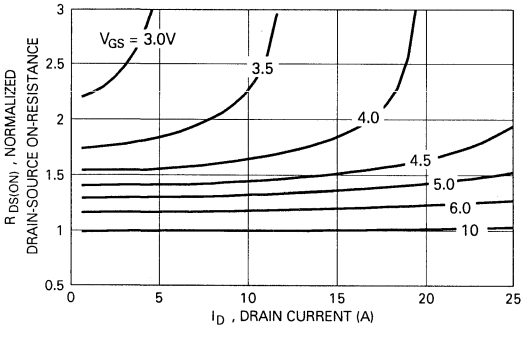


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

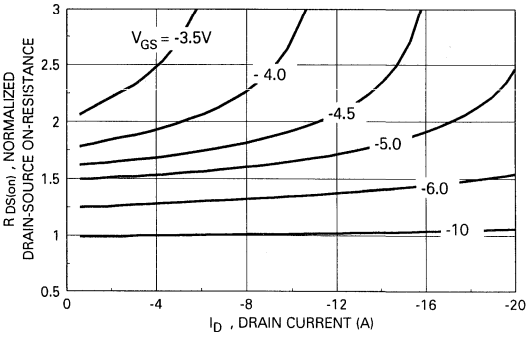


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

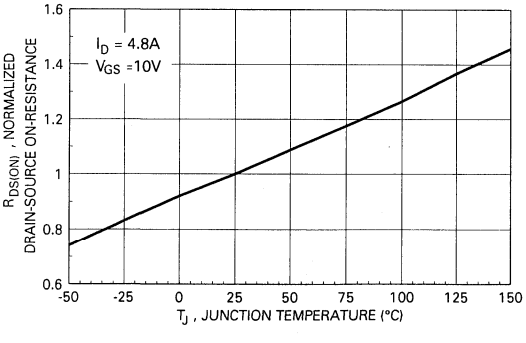


Figure 5. N-Channel On-Resistance Variation with Temperature.

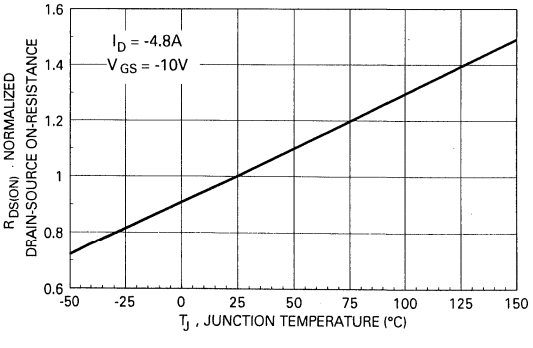


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

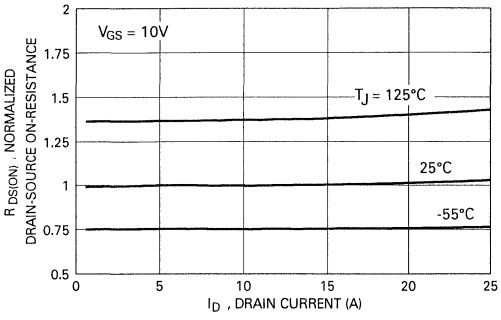


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

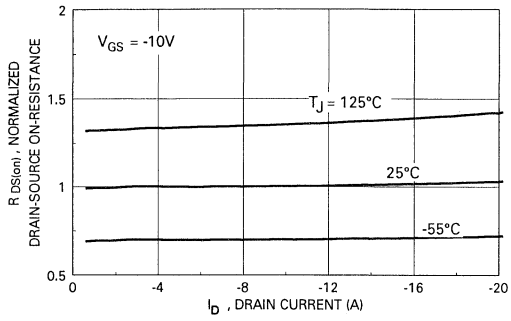


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

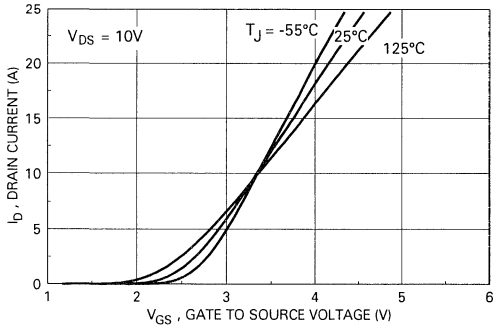


Figure 9. N-Channel Transfer Characteristics.

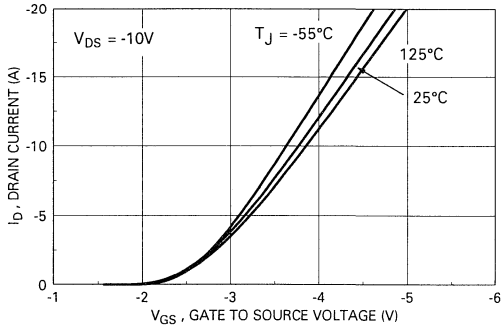


Figure 10. P-Channel Transfer Characteristics.

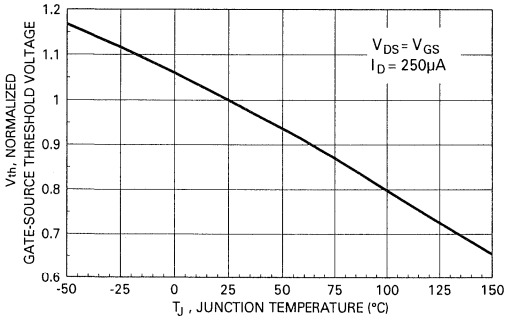


Figure 11. N-Channel Gate Threshold Variation with Temperature.

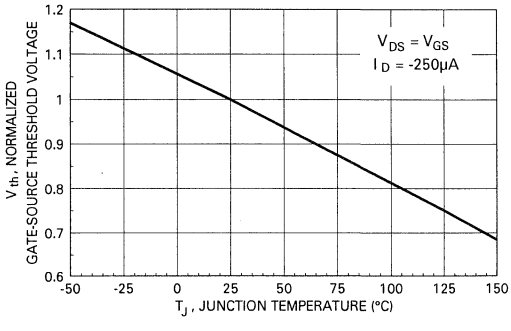


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

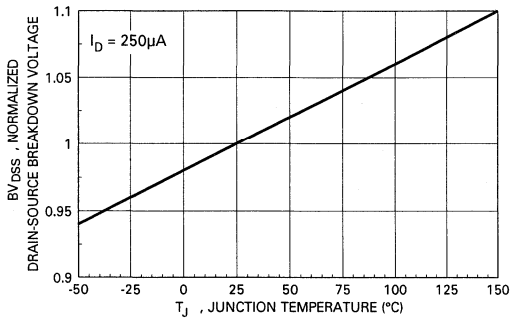


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

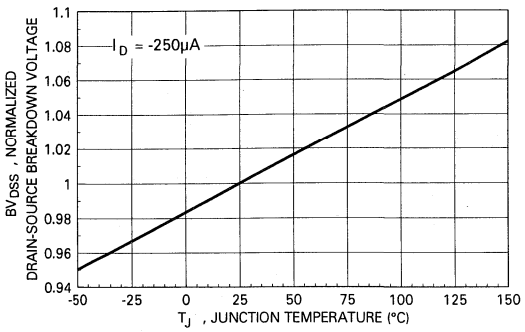


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

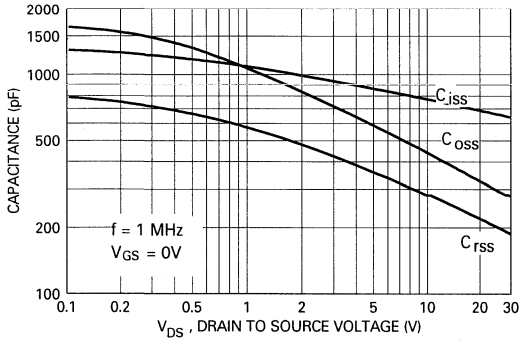


Figure 15. N-Channel Capacitance Characteristics.

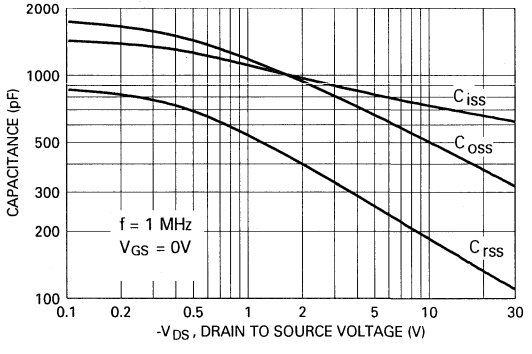


Figure 16. P-Channel Capacitance Characteristics.

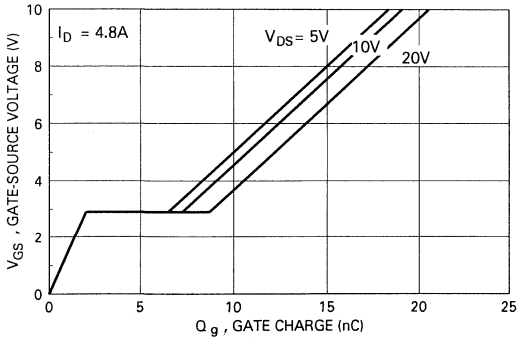


Figure 17. N-Channel Gate Charge Characteristics.

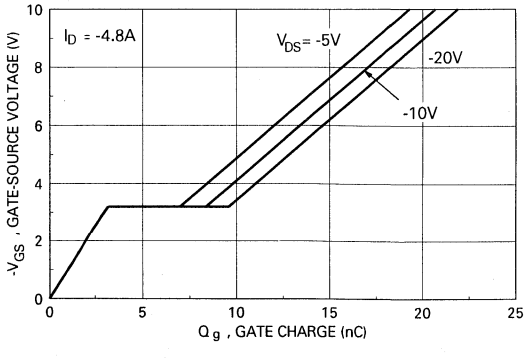


Figure 18. P-Channel Gate Charge Characteristics.

Typical Electrical and Thermal Characteristics

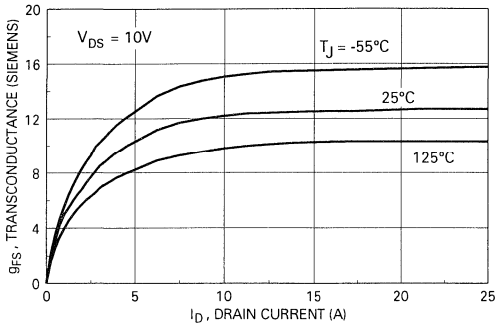


Figure 19. N-Channel Transconductance Variation with Drain Current and Temperature.

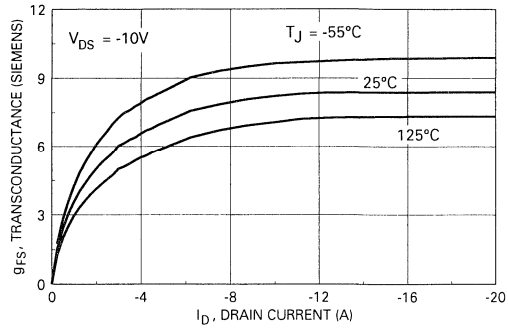


Figure 20. P-Channel Transconductance Variation with Drain Current and Temperature.

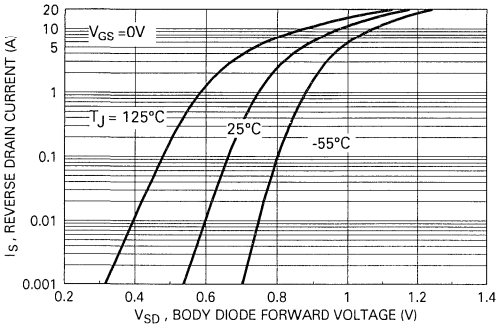


Figure 21. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

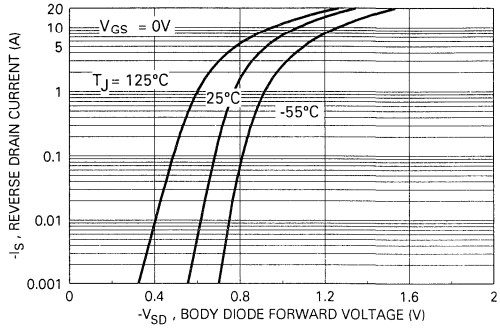


Figure 22. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

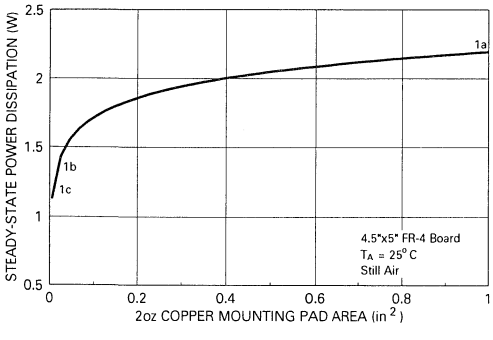


Figure 23. SO-8 Single Device DC Power Dissipation versus Copper Mounting Pad Area.

Typical Thermal Characteristics

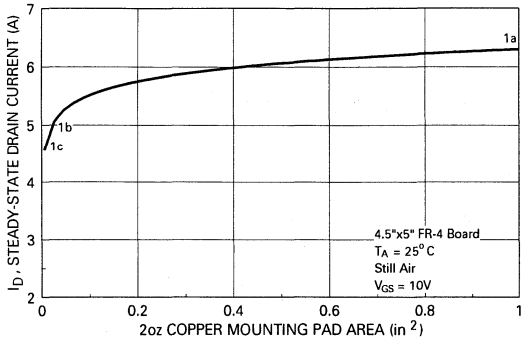


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

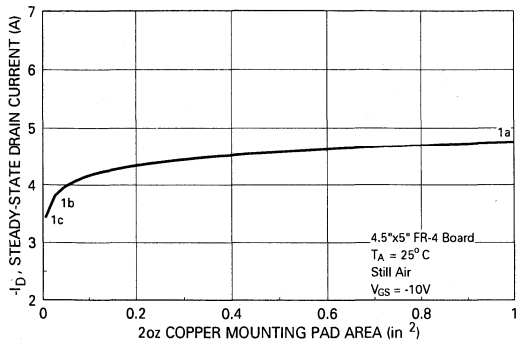


Figure 25. P-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

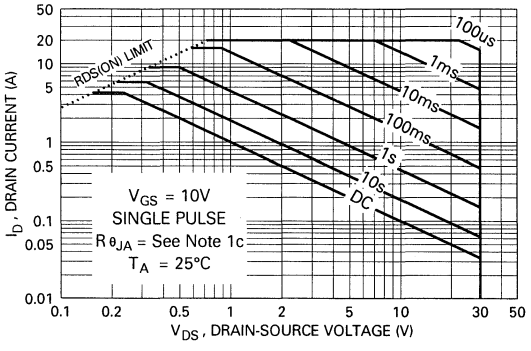


Figure 26. N-Ch Maximum Safe Operating Area.

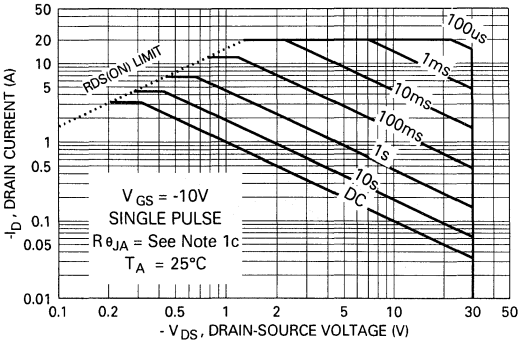


Figure 27. P-Ch Maximum Safe Operating Area.

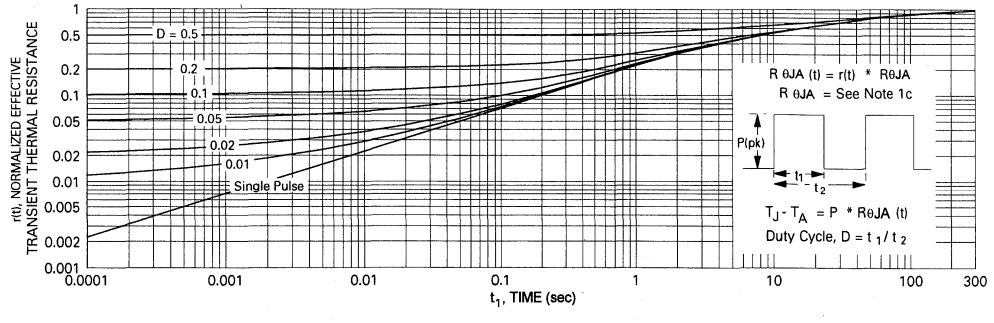


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

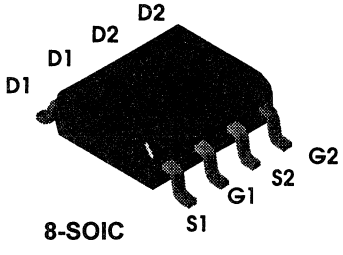
NDS8926
Dual N-Channel Enhancement Mode Field Effect Transistor

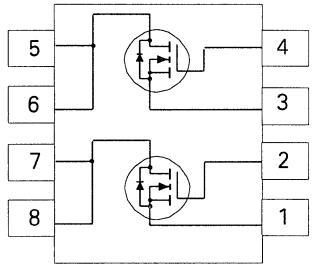
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5.5A, 20V. $R_{DS(ON)}$ = 0.035Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.045Ω @ V_{GS} = 2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise note

Symbol	Parameter	NDS8926	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	8	V
I_D	Drain Current - Continuous (Note 1a)	5.5	A
	- Pulsed	20	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4	0.6	1	V
		T_J = 125°C	0.3	0.35	0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 5.5 A		0.029	0.035	Ω
		T_J = 125°C		0.04	0.063	
		V_{GS} = 2.7 V, I_D = 5 A		0.035	0.045	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	20			A
		V_{GS} = 2.7 V, V_{DS} = 5 V	10			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.5 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		760		pF
C_{oss}	Output Capacitance			440		pF
C_{rss}	Reverse Transfer Capacitance			160		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 6 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn - On Rise Time			30	50	ns
$t_{D(off)}$	Turn - Off Delay Time			55	80	ns
t_f	Turn - Off Fall Time			20	40	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 5.5 A, V_{GS} = 4.5 V		21	30	nC
Q_{gs}	Gate-Source Charge			2.3		nC
Q_{gd}	Gate-Drain Charge			6.8		nC

4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

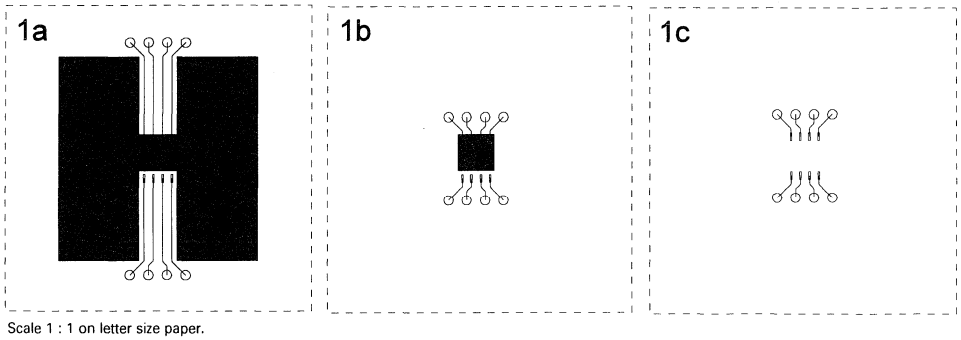
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

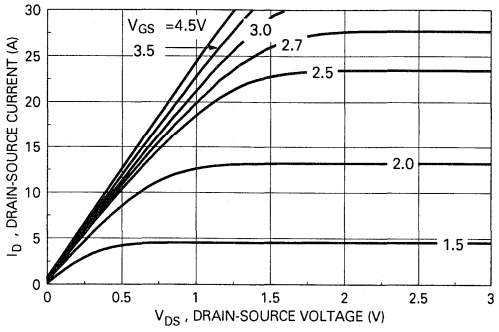


Figure 1. On-Region Characteristics.

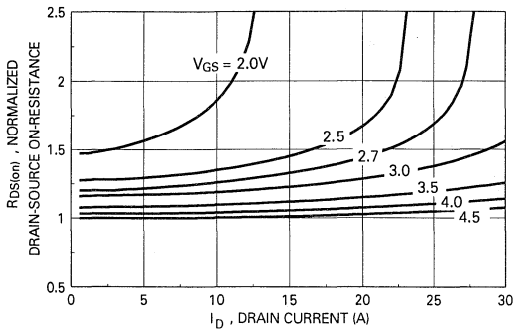


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

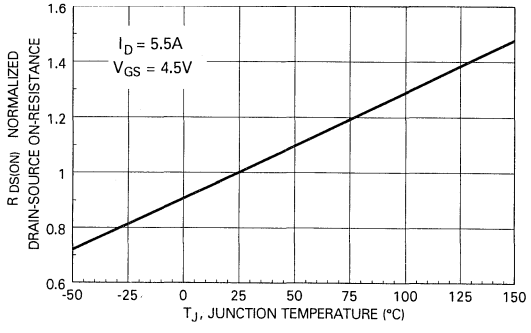


Figure 3. On-Resistance Variation with Temperature.

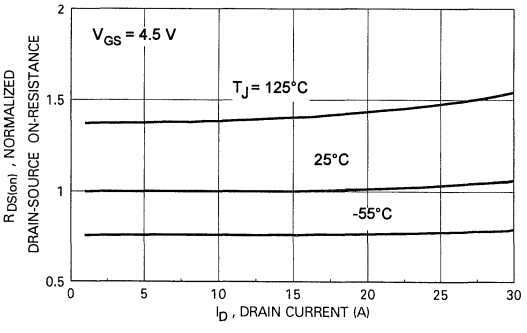


Figure 4. On-Resistance Variation with Drain Current and Temperature.

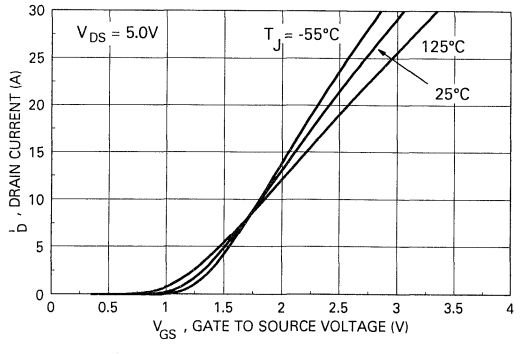


Figure 5. Transfer Characteristics.

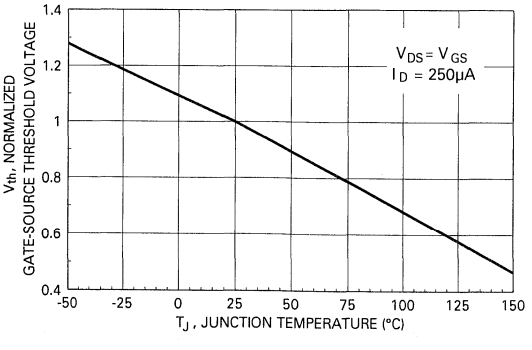


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

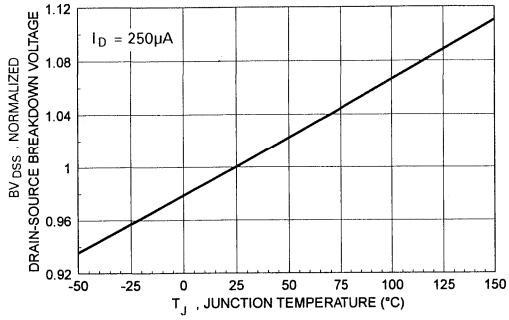


Figure 7. Breakdown Voltage Variation with Temperature.

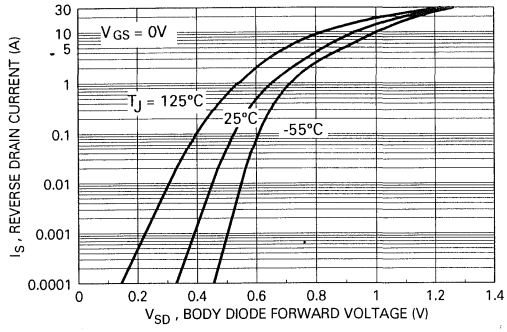


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

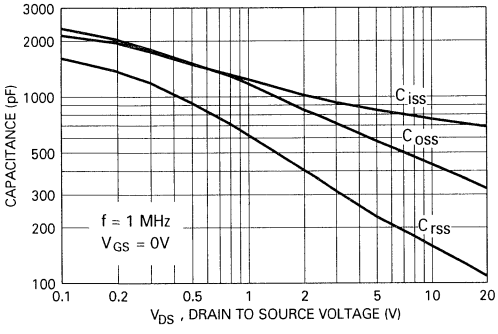


Figure 9. Capacitance Characteristics.

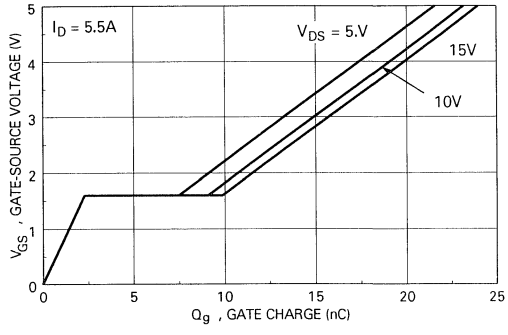


Figure 10. Gate Charge Characteristics.

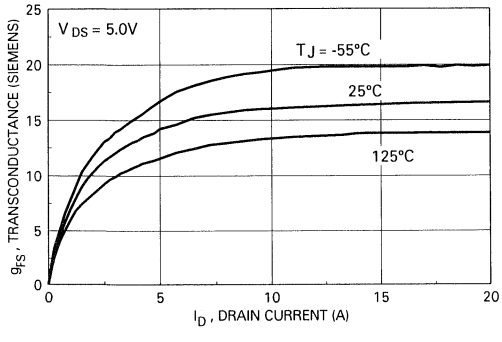


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

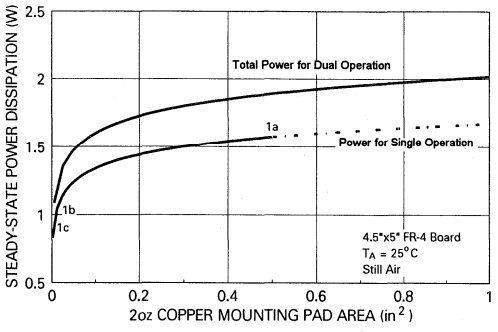


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

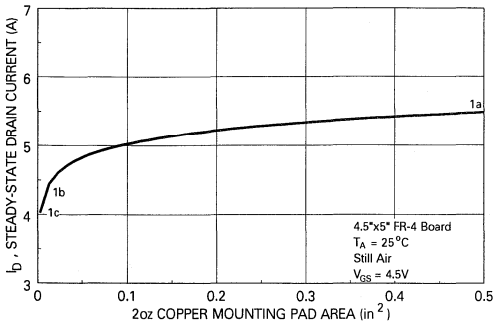


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

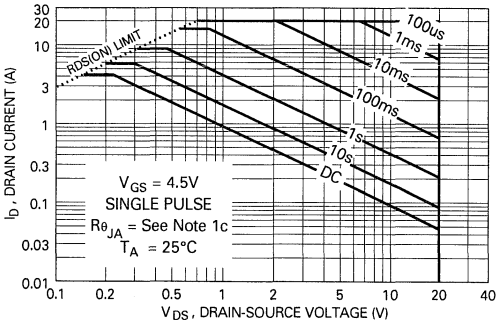


Figure 14. Maximum Safe Operating Area.

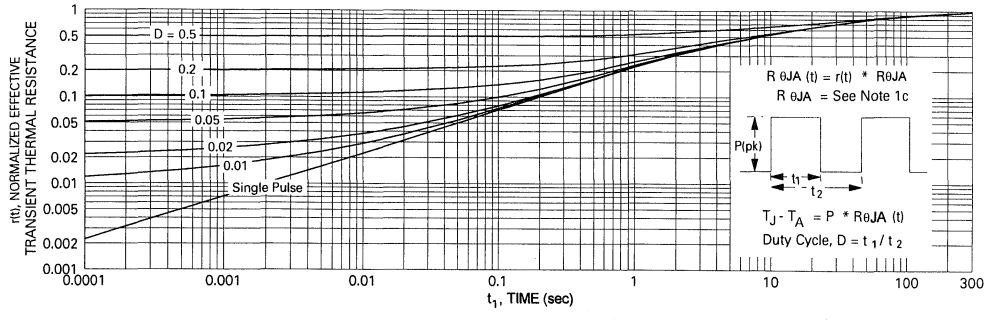


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

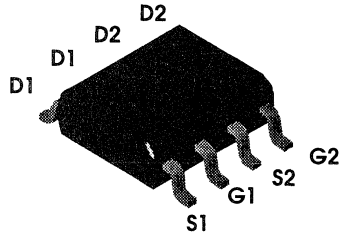
NDS8928
Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

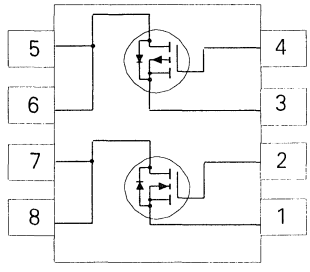
These dual N- and P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 5.5A, 20V, $R_{DS(ON)}$=0.035Ω @ V_{GS}=4.5V
  $R_{DS(ON)}$=0.045Ω @ V_{GS}=2.7V
  P-Channel -3.8A, -20V, $R_{DS(ON)}$=0.07Ω @ V_{GS}=-4.5V
  $R_{DS(ON)}$=0.1Ω @ V_{GS}=-2.7V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.



8-SOIC



Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		20	-20	V
V_{GSS}	Gate-Source Voltage		8	-8	V
I_D	Drain Current - Continuous	(Note 1a)	5.5	-3.8	A
	- Pulsed		20	-15	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 55°C				10	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	µA
		T_J = 55°C				-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.4	0.6	1	V
		T_J = 125°C		0.3	0.35	0.8	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-0.4	-0.7	-1	
		T_J = 125°C		-0.3	-0.5	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 5.5 A	N-Ch			0.035	Ω
		T_J = 125°C				0.063	
		V_{GS} = 2.7 V, I_D = 5 A				0.045	
		V_{GS} = -4.5 V, I_D = -3.8 A	P-Ch		0.06	0.07	
		T_J = 125°C			0.085	0.14	
		V_{GS} = -2.7 V, I_D = -3.2 A			0.082	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	N-Ch	20			A
		V_{GS} = 2.7 V, V_{DS} = 5 V		10			
		V_{GS} = -4.5 V, V_{DS} = -5 V	P-Ch	-15			
		V_{GS} = -2.7 V, V_{DS} = -5 V		-5			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.5 A	N-Ch		14		S
		V_{DS} = -10 V, I_D = -3.8 A	P-Ch		9		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel	N-Ch		760		pF
		V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		1120		
C_{oss}	Output Capacitance		N-Ch		440		pF
		P-Channel	P-Ch		470		
C_{rss}	Reverse Transfer Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		160		pF
			P-Ch		145		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 5 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω	N-Ch		10	20	ns
			P-Ch		13	20	
t_r	Turn - On Rise Time		N-Ch		30	50	ns
		P-Channel V_{DD} = -5 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω	P-Ch		53	70	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		55	80	ns
			P-Ch		60	80	
t_f	Turn - Off Fall Time		N-Ch		20	40	ns
			P-Ch		33	40	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 5.5 A, V_{GS} = 4.5 V	N-Ch		21	30	nC
			P-Ch		19	30	
Q_{gs}	Gate-Source Charge		N-Ch		2.3		nC
		P-Channel V_{DS} = -10 V, I_D = -3.8 A, V_{GS} = -4.5 V	P-Ch		2.4		
Q_{gd}	Gate-Drain Charge		N-Ch		6.8		nC
			P-Ch		5.5		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.3	A
			P-Ch			-1.3	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	N-Ch		0.8	1.2	V
		V_{GS} = 0 V, I_S = -1.3 A (Note 2)	P-Ch		-0.75	-1.2	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

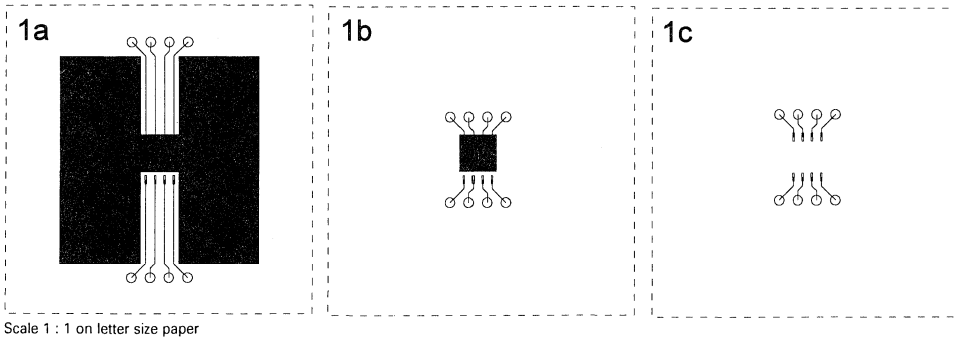
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

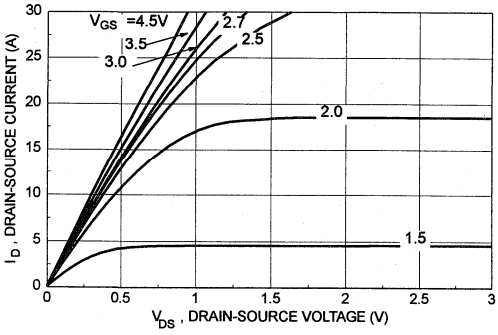


Figure 1. N-Channel On-Region Characteristics.

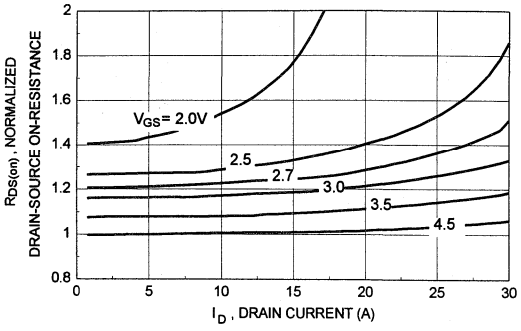


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

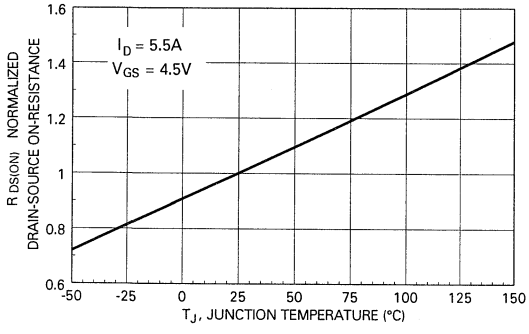


Figure 3. N-Channel On-Resistance Variation with Temperature.

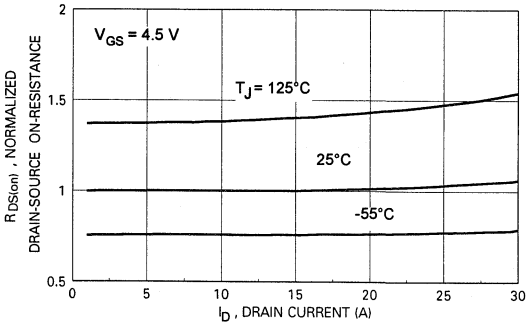


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

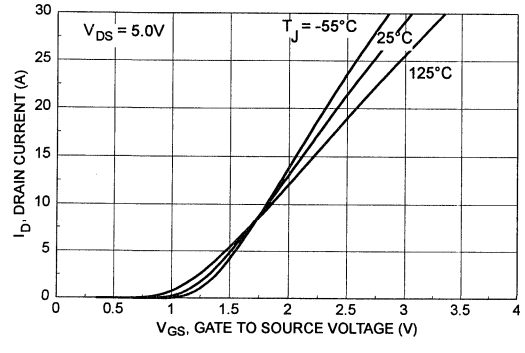


Figure 5. N-Channel Transfer Characteristics.

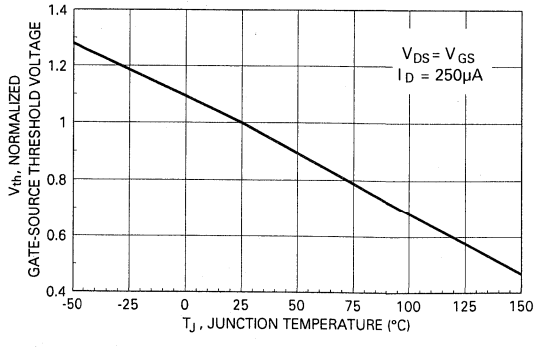


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

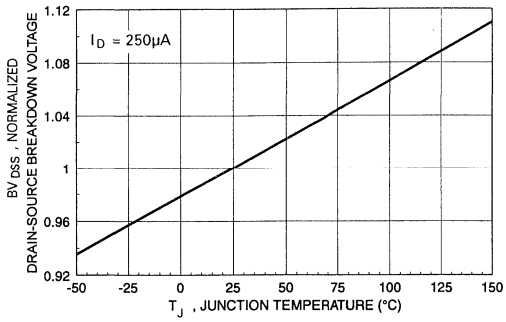


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

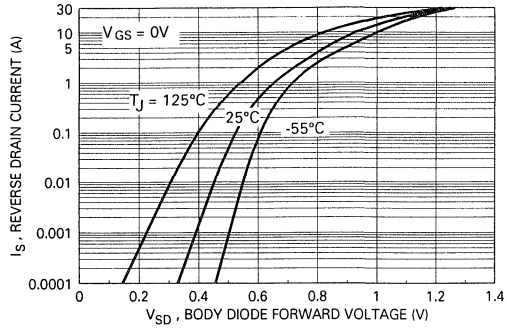


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

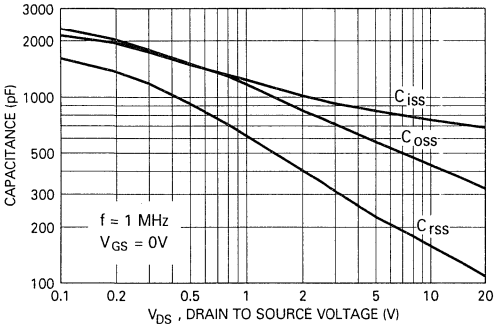


Figure 9. N-Channel Capacitance Characteristics.

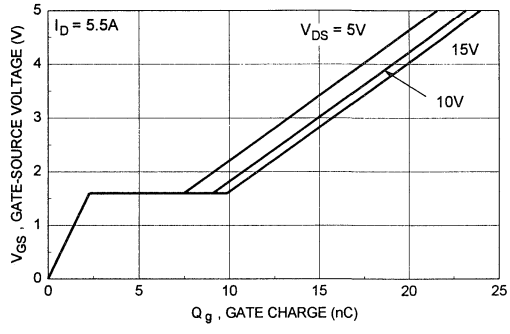


Figure 10. N-Channel Gate Charge Characteristics.

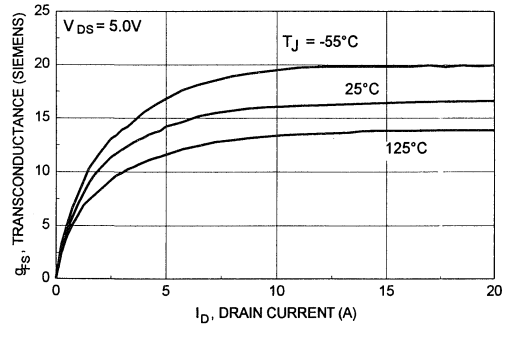


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

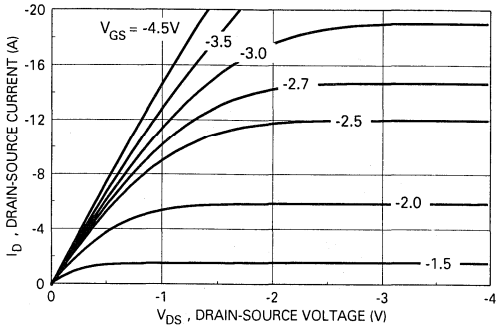


Figure 12. P-Channel On-Region Characteristics.

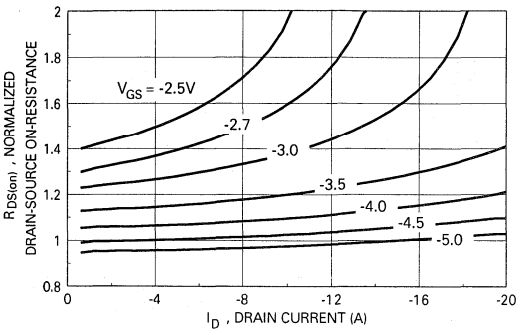


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

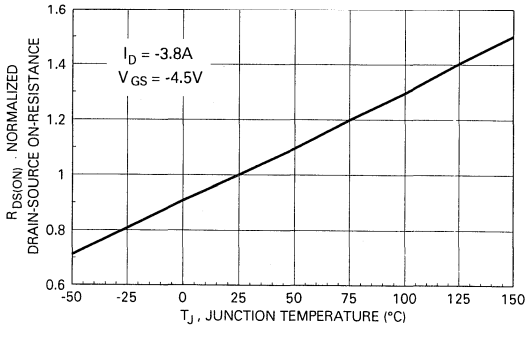


Figure 14. P-Channel On-Resistance Variation with Temperature.

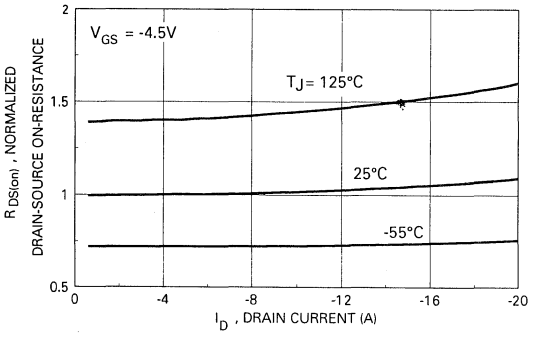


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

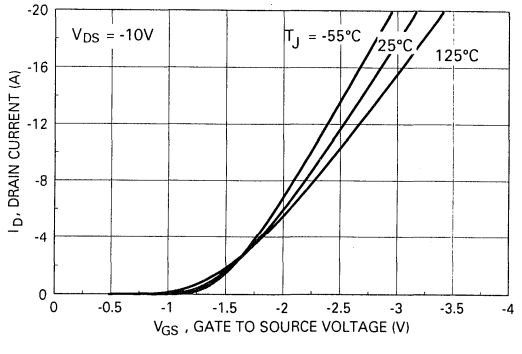


Figure 16. P-Channel Transfer Characteristics.

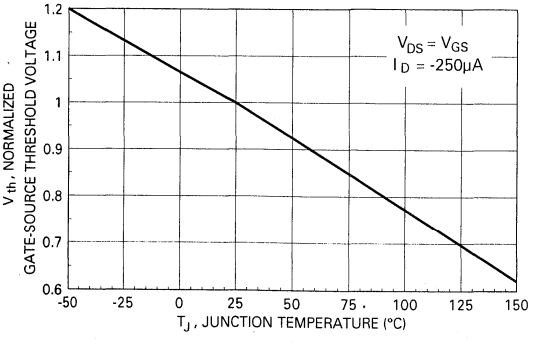


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

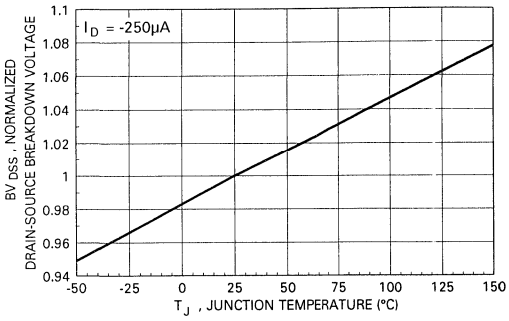


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

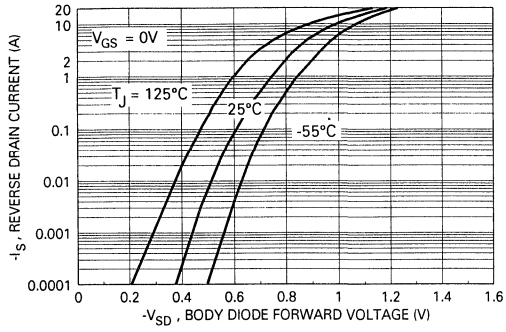


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

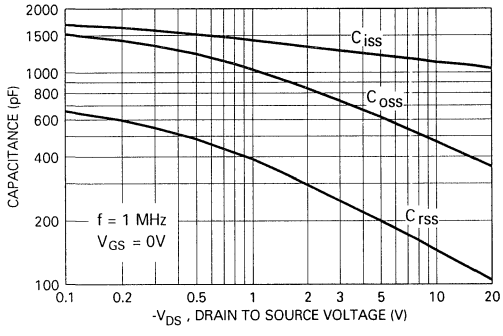


Figure 20. P-Channel Capacitance Characteristics.

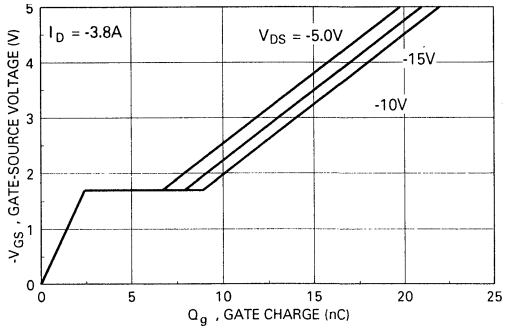


Figure 21. P-Channel Gate Charge Characteristics.

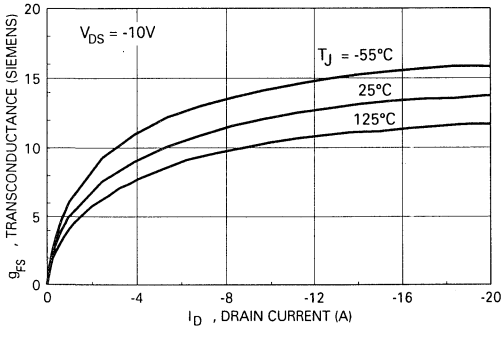


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

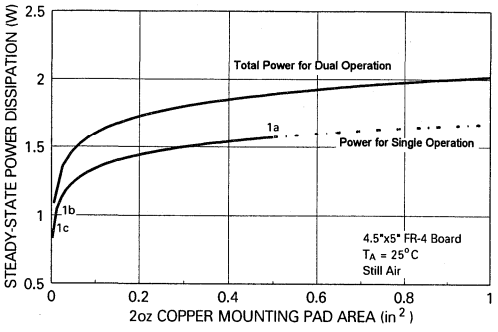


Figure 23. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

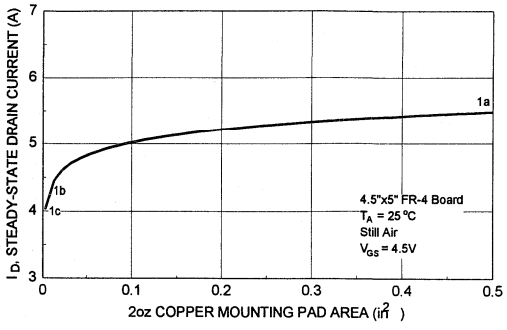


Figure 24. N-Ch Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

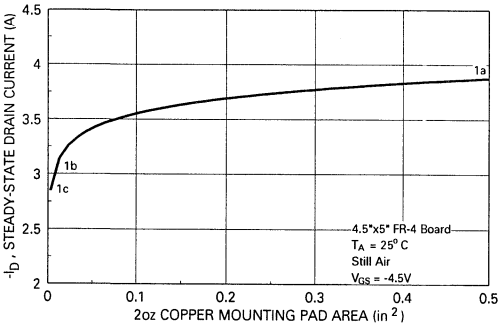


Figure 25. P-Ch Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

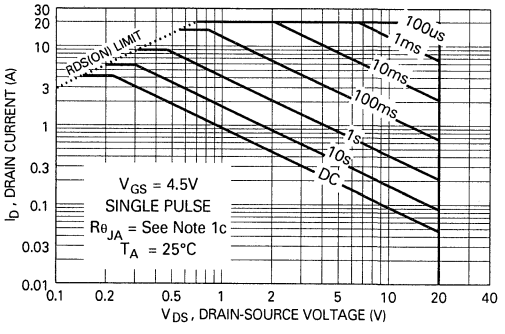


Figure 26. N-Channel Maximum Safe Operating Area.

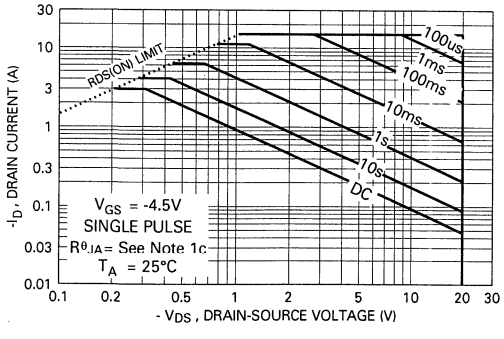


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

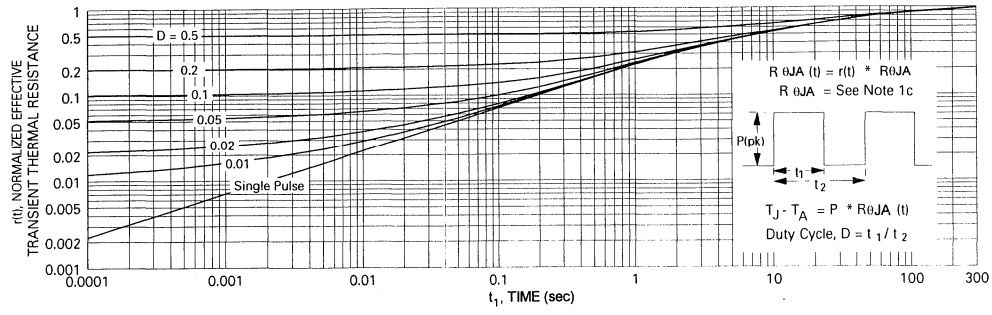


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

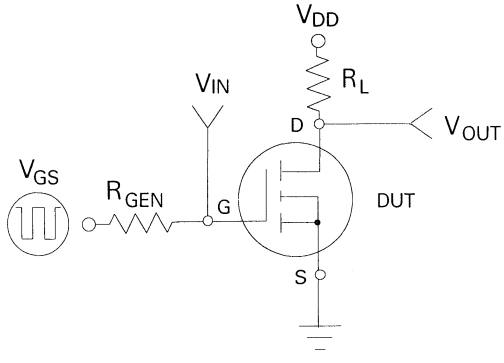


Figure 29. N or P-Channel Switching Test Circuit.

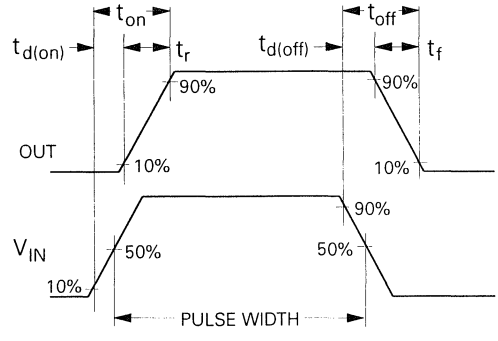


Figure 30. N or P-Channel Switching Waveforms.

National Semiconductor™

June 1996

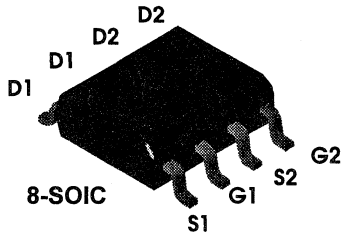
NDS8934
Dual P-Channel Enhancement Mode Field Effect Transistor

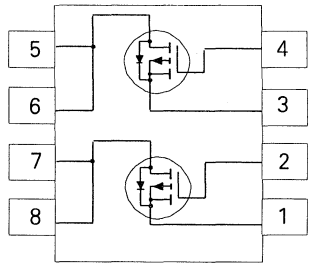
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.8A, -20V. $R_{DS(ON)}$ = 0.07Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = -2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8934	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-8	V
I_D	Drain Current - Continuous	(Note 1a)	-3.8	A
	- Pulsed		-15	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -10 V, V_{GS} = 0 V, T_J = 70°C			-5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.7	-1	V
		T_J = 125°C	-0.3	-0.5	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -3.8 A		0.06	0.07	Ω
		T_J = 125°C		0.085	0.14	
		V_{GS} = -2.7 V, I_D = -3.2 A		0.082	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-15			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-5			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = -3.8 A		9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1120		pF
C_{oss}	Output Capacitance			470		pF
C_{rss}	Reverse Transfer Capacitance			145		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω		13	20	ns
t_r	Turn - On Rise Time			53	70	ns
$t_{D(off)}$	Turn - Off Delay Time			60	80	ns
t_f	Turn - Off Fall Time			33	40	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -3.8 A, V_{GS} = -4.5 V		19	30	nC
Q_{gs}	Gate-Source Charge			2.4		nC
Q_{gd}	Gate-Drain Charge			5.5		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)		-0.75	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

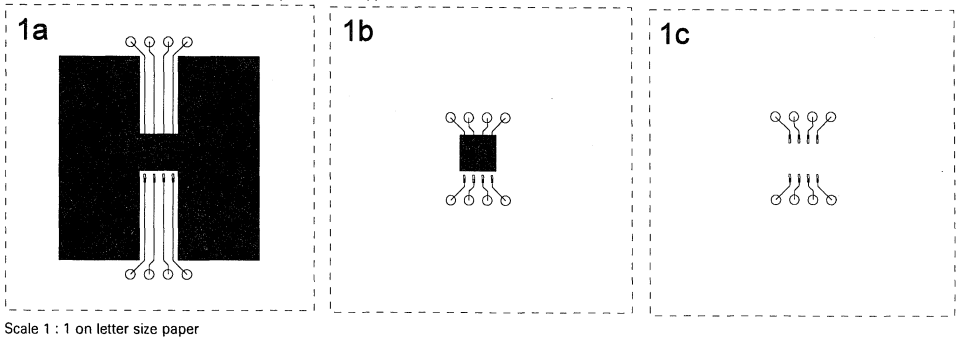
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%..

Typical Electrical Characteristics

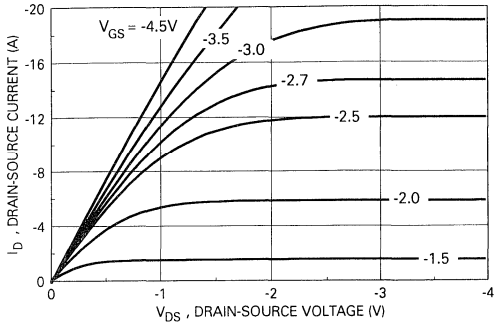


Figure 1. On-Region Characteristics.

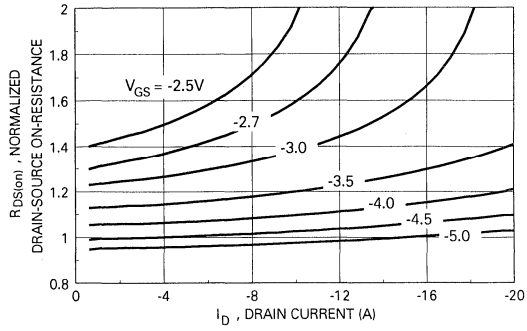


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

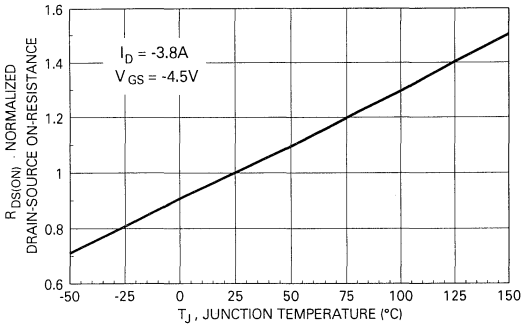


Figure 3. On-Resistance Variation with Temperature.

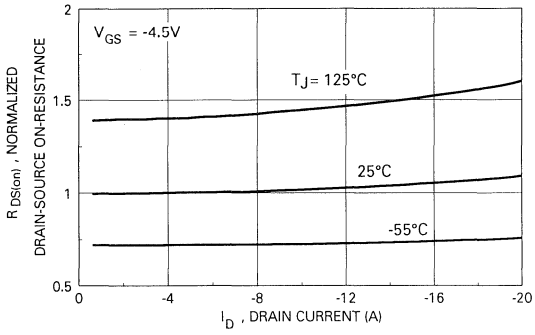


Figure 4. On-Resistance Variation with Drain Current and Temperature.

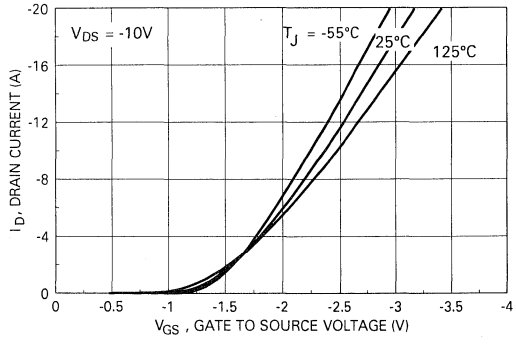


Figure 5. Transfer Characteristics.

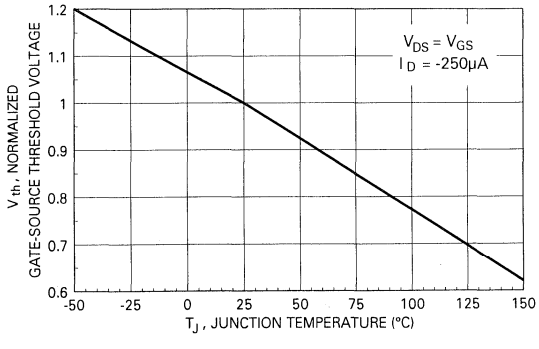


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

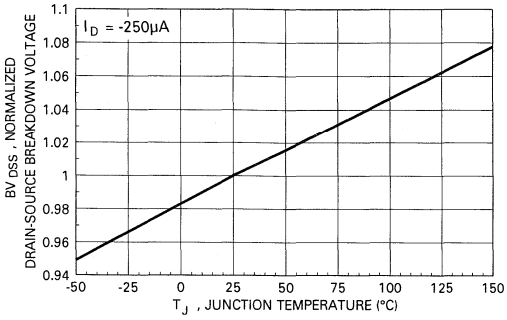


Figure 7. Breakdown Voltage Variation with Temperature.

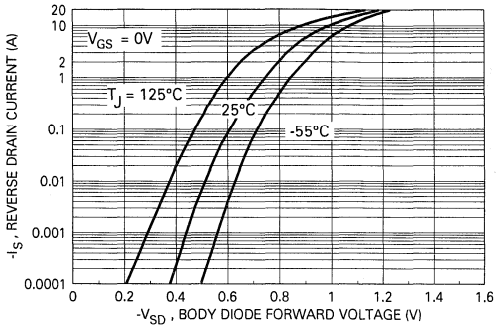


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

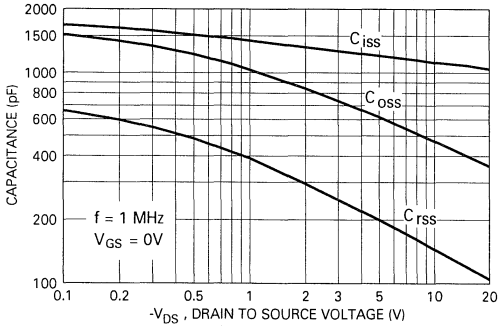


Figure 9. Capacitance Characteristics.

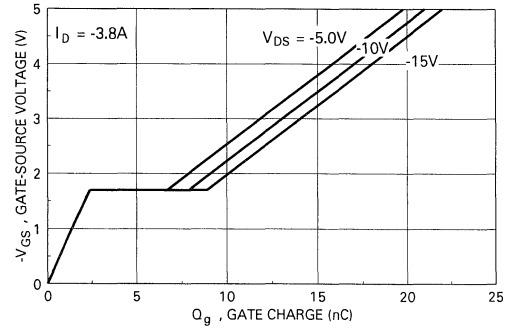


Figure 10. Gate Charge Characteristics.

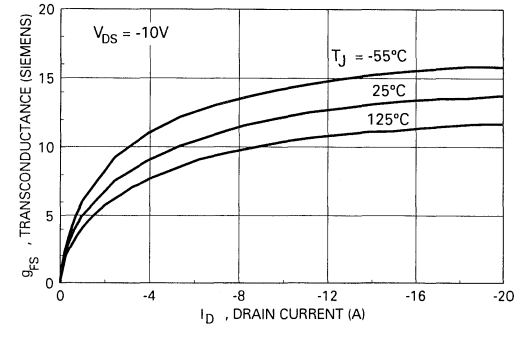


Figure 11. Transconductance Variation with Drain Current and Temperature.

4

Typical Thermal Characteristics

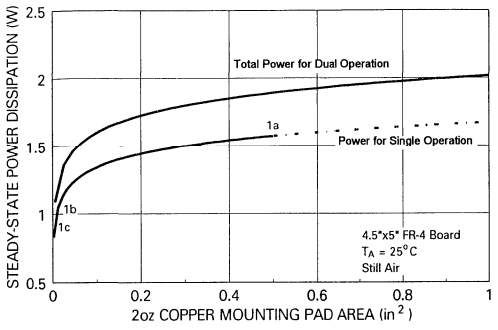


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

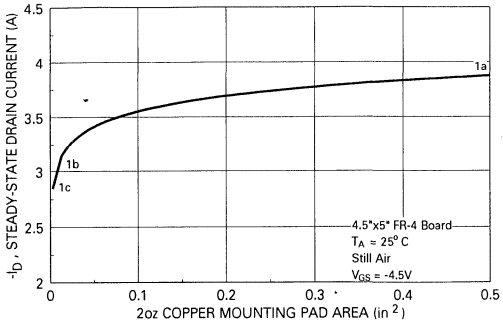


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

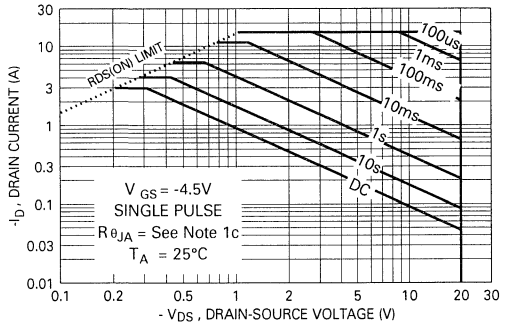


Figure 14. Maximum Safe Operating Area.

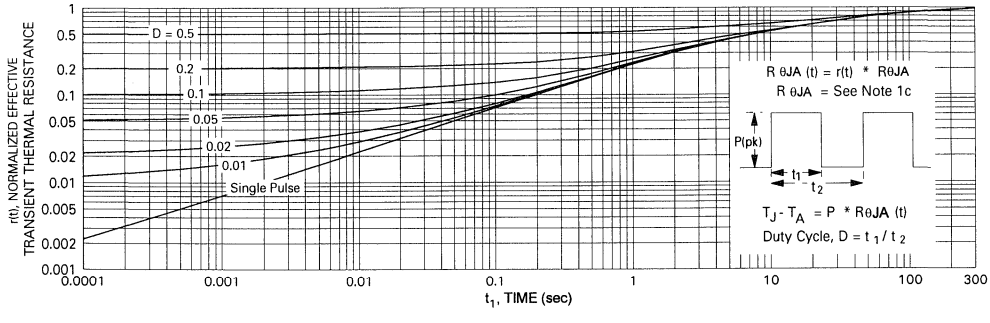


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

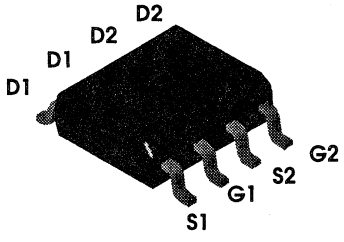
NDS8936
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

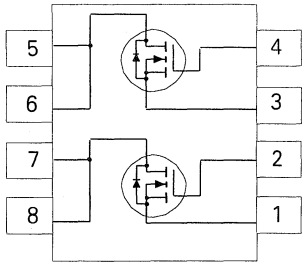
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5.3A, 30V. $R_{DS(ON)}$ = 0.037Ω @ V_{GS} = 10V
  $R_{DS(ON)}$ = 0.055Ω @ V_{GS} = 4.5V
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



8-SOIC



Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		NDS8936	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 5.3	A
	- Pulsed		± 20	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	2.8	V
		T_J = 125°C	0.7	1.2	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5.3 A		0.033	0.035	Ω
		T_J = 125°C		0.046	0.063	
		V_{GS} = 4.5 V, I_D = 4.4 A		0.046	0.05	
		T_J = 125°C		0.064	0.09	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	10			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.3 A		10.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		720		pF
C_{oss}	Output Capacitance			370		pF
C_{rss}	Reverse Transfer Capacitance			250		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		12	20	ns
t_r	Turn - On Rise Time			13	30	ns
$t_{D(off)}$	Turn - Off Delay Time			29	50	ns
t_f	Turn - Off Fall Time			10	20	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 5.3 A, V_{GS} = 10 V		19	30	nC
Q_{gs}	Gate-Source Charge			2.2		nC
Q_{gd}	Gate-Drain Charge			5.5		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 5.3 A (Note 2)		0.9	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

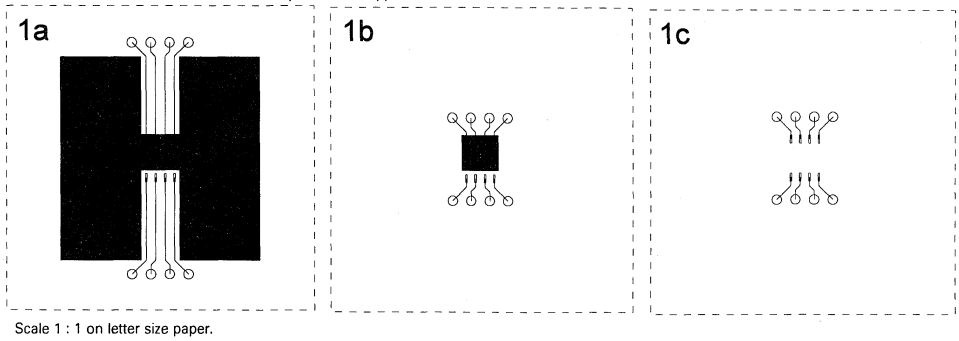
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

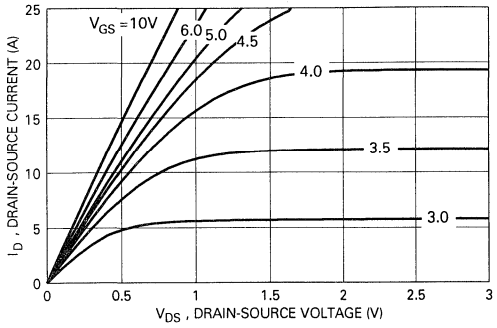


Figure 1. On-Region Characteristics.

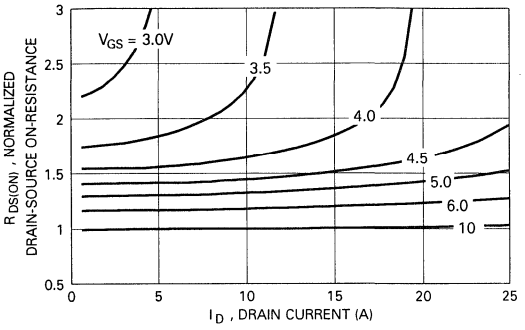


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

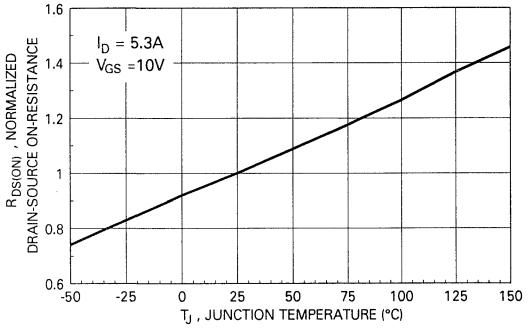


Figure 3. On-Resistance Variation with Temperature.

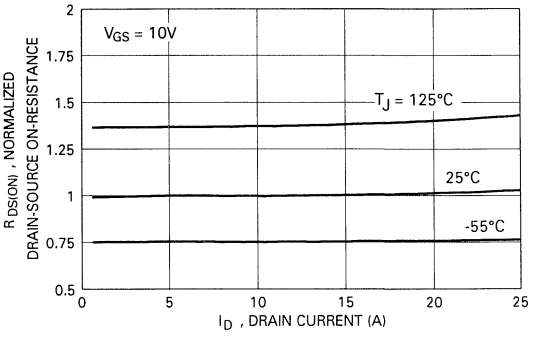


Figure 4. On-Resistance Variation with Drain Current and Temperature.

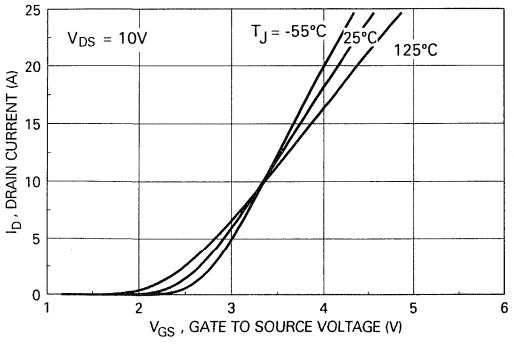


Figure 5. Transfer Characteristics.

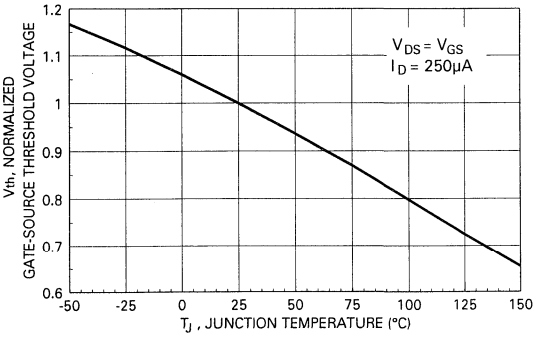


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

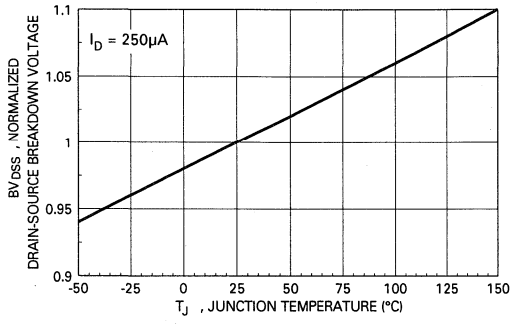


Figure 7. Breakdown Voltage Variation with Temperature.

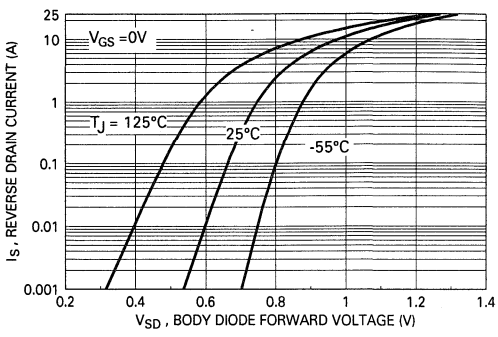


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

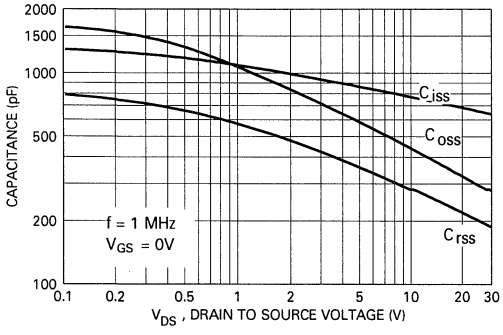


Figure 9. Capacitance Characteristics.

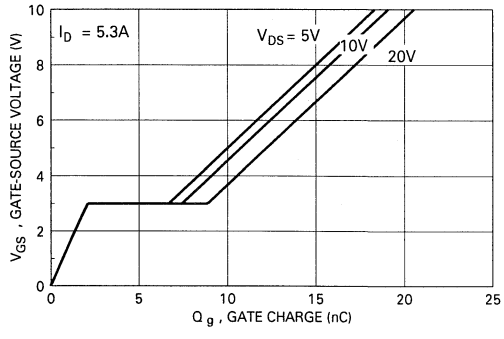


Figure 10. Gate Charge Characteristics.

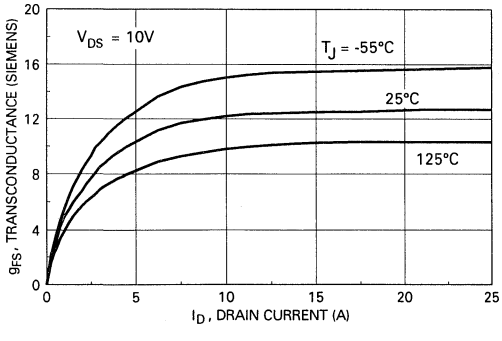


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

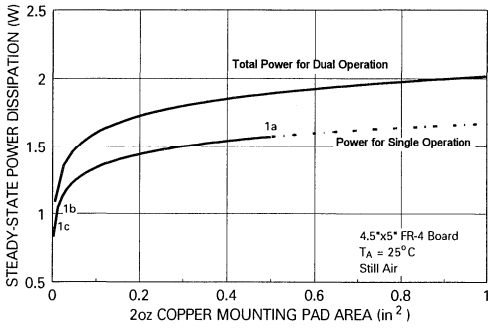


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

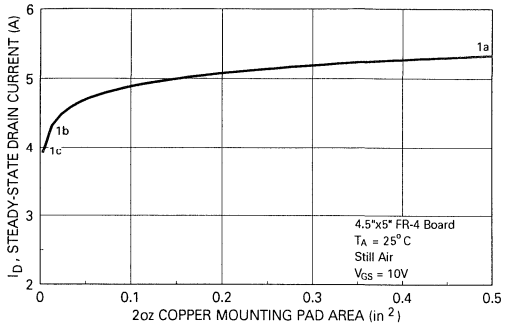


Figure 13. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

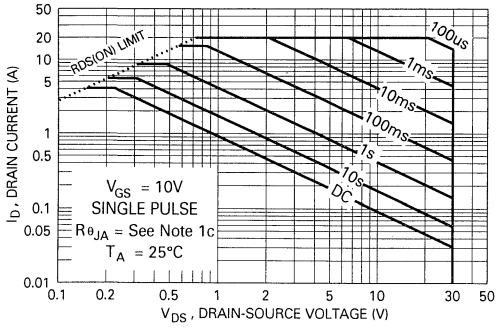


Figure 14. Maximum Safe Operating Area.

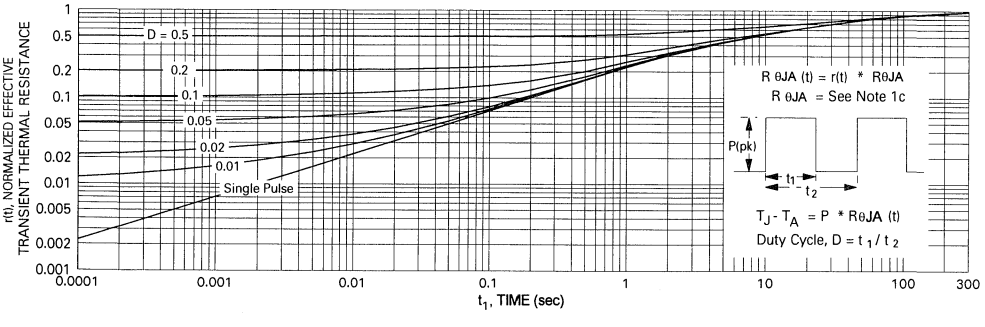


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

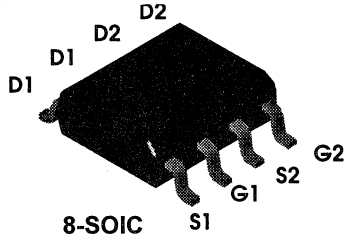
NDS8947
Dual P-Channel Enhancement Mode Field Effect Transistor

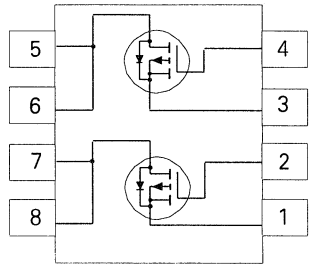
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4A, -30V. $R_{DS(ON)}$ = 0.065Ω @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = -4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





4

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS8947	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		-20	V
I_D	Drain Current - Continuous	(Note 1a)	-4	A
	- Pulsed		-15	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.6	-2.8	V
		T_J = 125°C	-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -4.0 A		0.052	0.065	Ω
		T_J = 125°C		0.075	0.13	
		V_{GS} = -4.5 V, I_D = -3.3 A		0.085	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-5			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -4.0 A		7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		690		pF
C_{oss}	Output Capacitance			430		pF
C_{rss}	Reverse Transfer Capacitance			160		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		9	20	ns
t_r	Turn - On Rise Time			20	30	ns
$t_{D(off)}$	Turn - Off Delay Time			40	50	ns
t_f	Turn - Off Fall Time			19	40	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -4.0 A, V_{GS} = -10 V		21	30	nC
Q_{gs}	Gate-Source Charge			3.1		nC
Q_{gd}	Gate-Drain Charge			5.1		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)		-0.85	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = -1.3 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

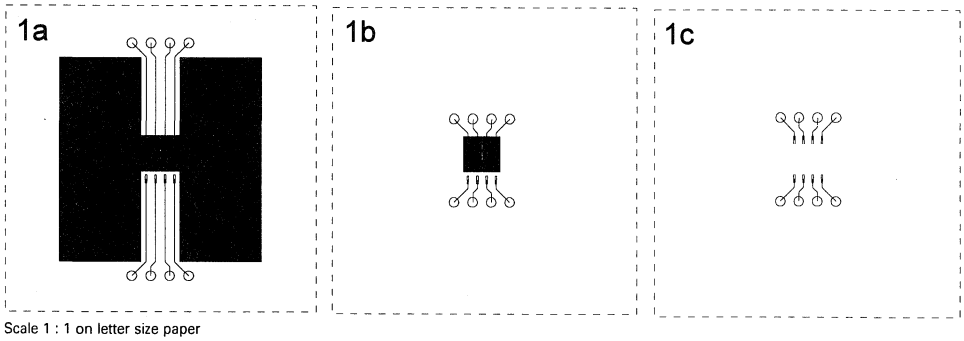
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%..

Typical Electrical Characteristics

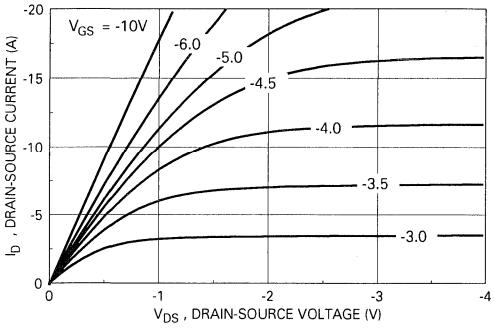


Figure 1. On-Region Characteristics.

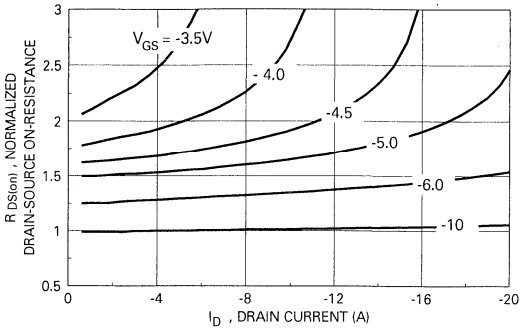


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

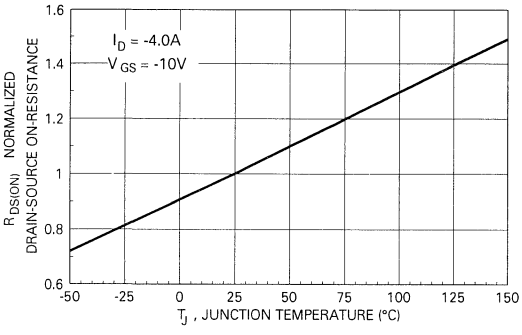


Figure 3. On-Resistance Variation with Temperature.

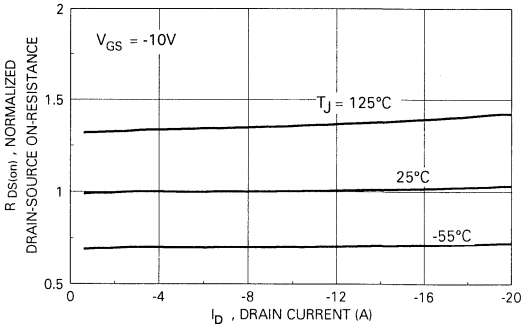


Figure 4. On-Resistance Variation with Drain Current and Temperature.

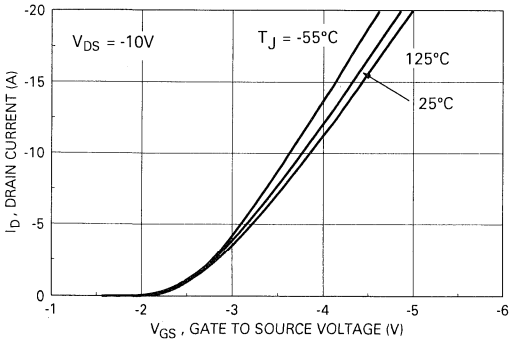


Figure 5. Transfer Characteristics.

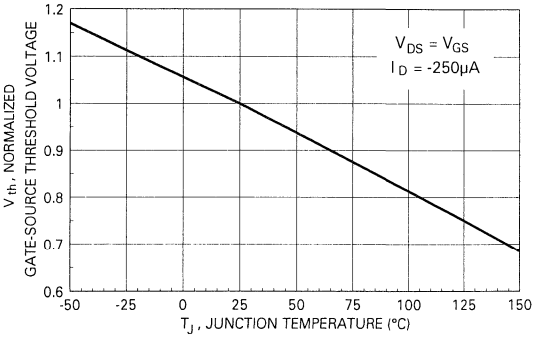


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

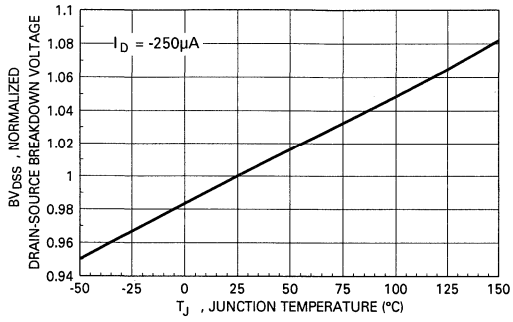


Figure 7. Breakdown Voltage Variation with Temperature.

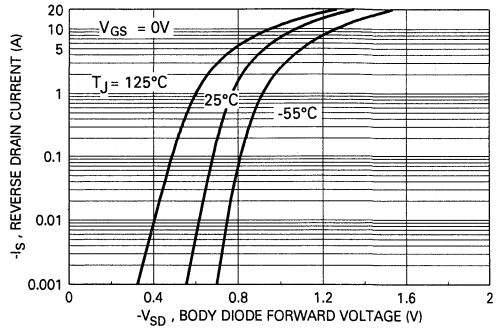


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

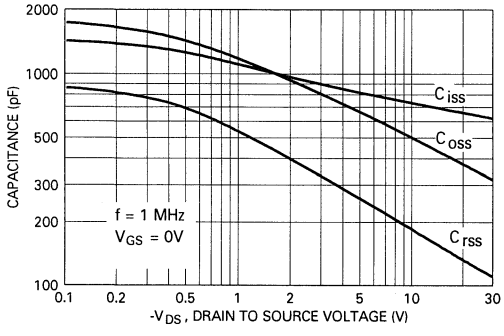


Figure 9. Capacitance Characteristics.

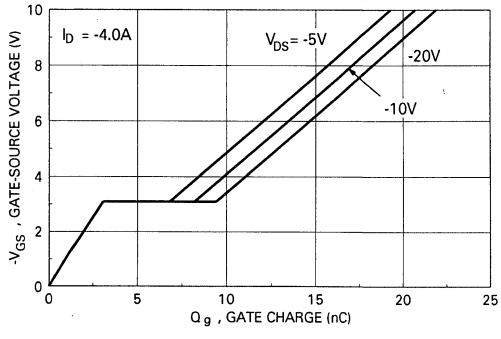


Figure 10. Gate Charge Characteristics.

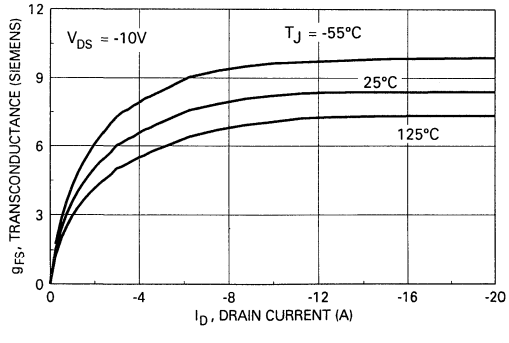


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

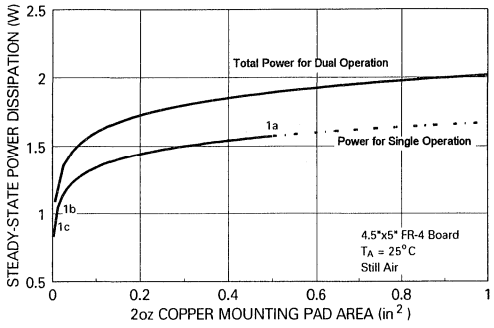


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

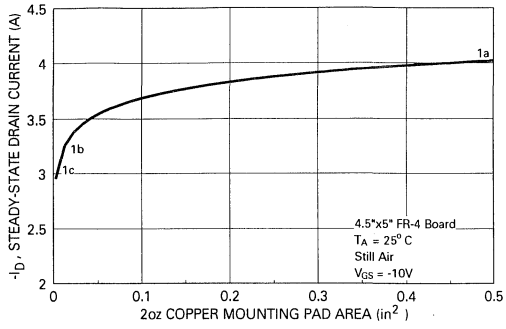


Figure 13. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

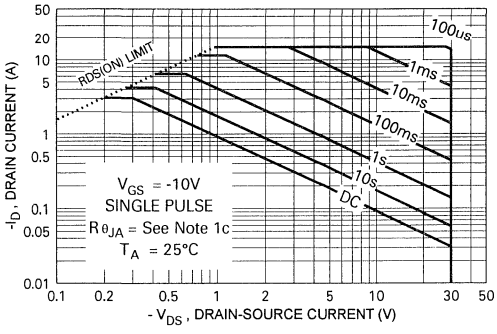


Figure 14. Maximum Safe Operating Area.

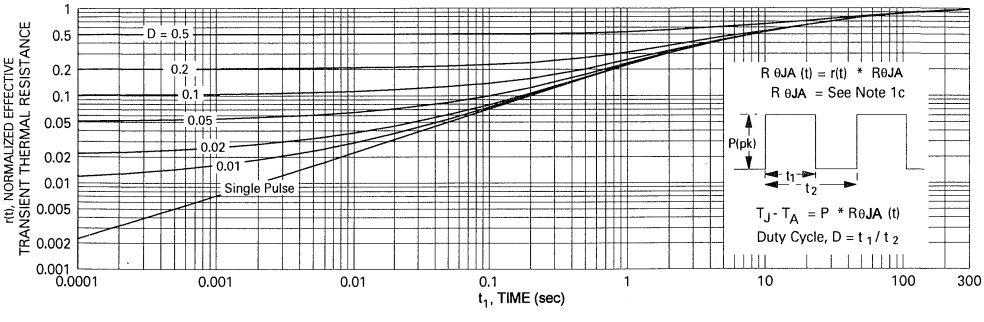


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

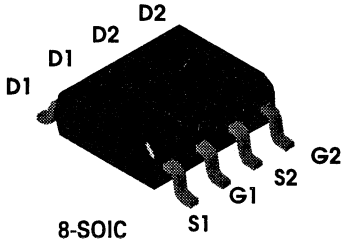
NDS8958
Dual N & P-Channel Enhancement Mode Field Effect Transistor

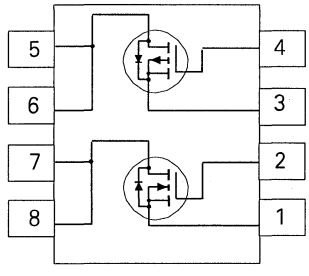
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 5.3A, 30V, $R_{DS(ON)}$=0.035Ω @ V_{GS}=10V.
  P-Channel -4.0A, -30V, $R_{DS(ON)}$=0.065Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





4

Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		20	-20	V
I_D	Drain Current - Continuous	(Note 1a)	5.3	-4	A
	- Pulsed		20	-15	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 55°C				10	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-1	µA
		T_J = 55°C				-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.6	2.8	V
		T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.6	-2.8	
		T_J = 125°C		-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5.3 A	N-Ch		0.033	0.035	Ω
		T_J = 125°C			0.046	0.063	
		V_{GS} = 4.5 V, I_D = 4.4 A			0.046	0.05	
		V_{GS} = -10 V, I_D = -4.0 A	P-Ch		0.052	0.065	
		T_J = 125°C			0.075	0.13	
		V_{GS} = -4.5 V, I_D = -3.3 A			0.085	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	20			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-15			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.3 A	N-Ch		10.5		S
		V_{DS} = -10 V, I_D = -4.0 A	P-Ch		7		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		720		pF
			P-Ch		690		
C_{oss}	Output Capacitance		N-Ch		370		pF
		P-Channel V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		430		
C_{rss}	Reverse Transfer Capacitance		N-Ch		250		pF
			P-Ch		160		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		12	20	ns
			P-Ch		9	20	
t_r	Turn - On Rise Time		N-Ch		13	30	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		20	25	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		29	50	ns
			P-Ch		40	50	
t_f	Turn - Off Fall Time		N-Ch		10	20	ns
			P-Ch		19	40	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 5.3 A, V_{GS} = 10 V	N-Ch		19	30	nC
			P-Ch		21	30	
Q_{gs}	Gate-Source Charge		N-Ch		2.2		
		P-Channel V_{DS} = -10 V, I_D = -4.0 A, V_{GS} = -10 V	P-Ch		3.1		
Q_{gd}	Gate-Drain Charge		N-Ch		5.5		
			P-Ch		5.1		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.3	A
			P-Ch			-1.3	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	N-Ch		0.9	1.2	V
		V_{GS} = 0 V, I_S = -1.3 A (Note 2)	P-Ch		-0.85	-1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.3 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
		V_{GS} = 0 V, I_F = -1.3 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

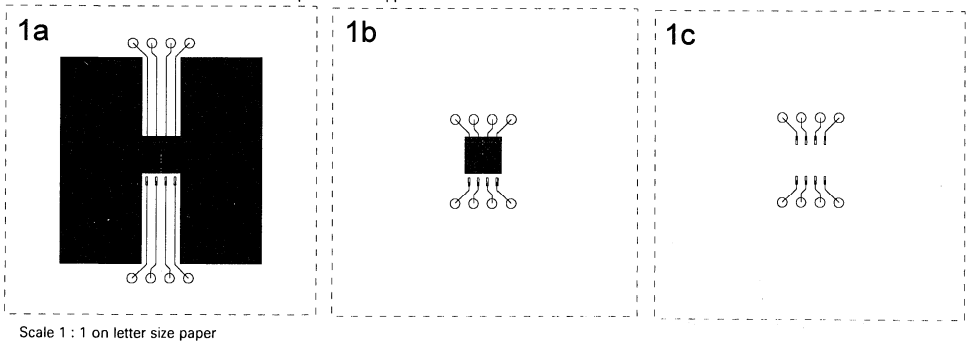
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

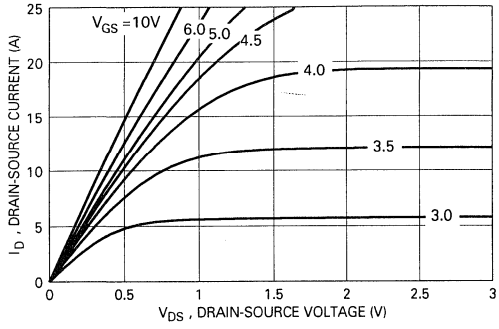


Figure 1. N-Channel On-Region Characteristic.

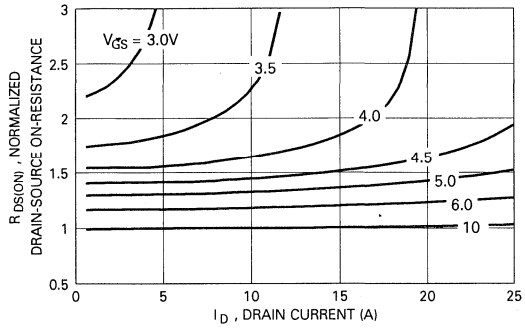


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

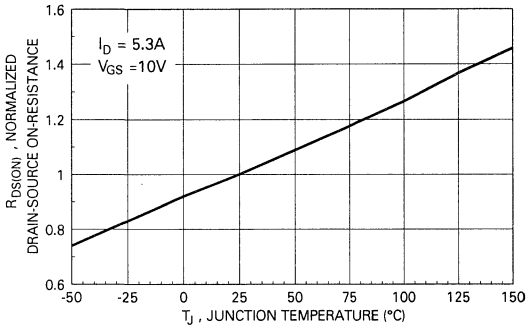


Figure 3. N-Channel On-Resistance Variation with Temperature.

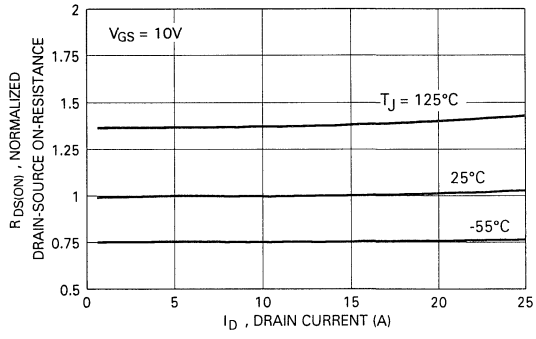


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

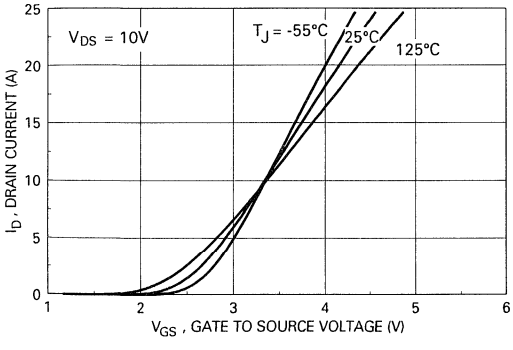


Figure 5. N-Channel Transfer Characteristic.

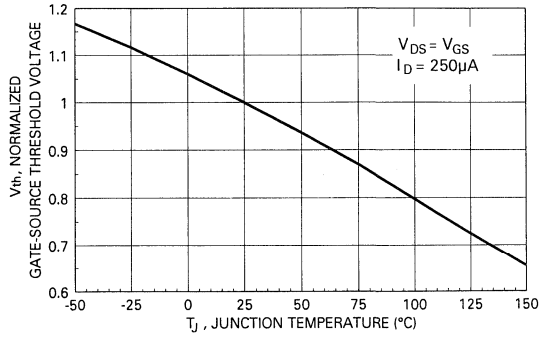


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

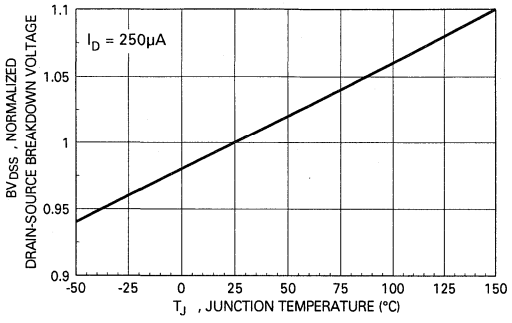


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

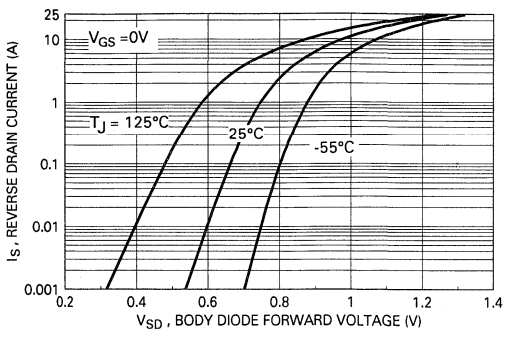


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

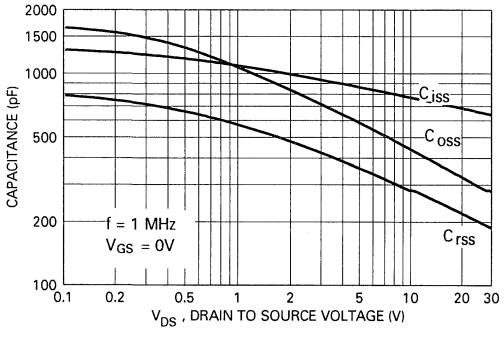


Figure 9. N-Channel Capacitance Characteristics.

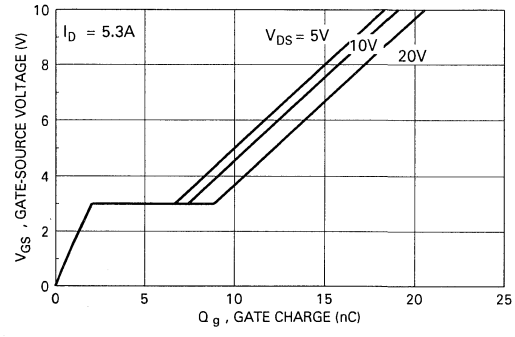


Figure 10. N-Channel Gate Charge Characteristics.

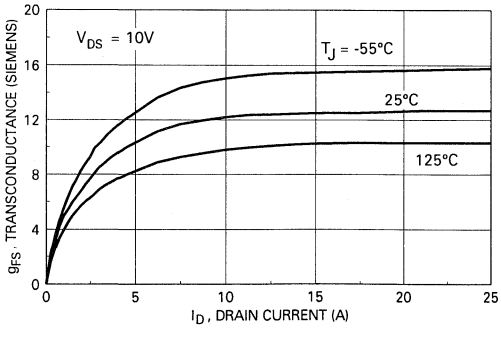


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

4

Typical Electrical Characteristics: P-Channel (continued)

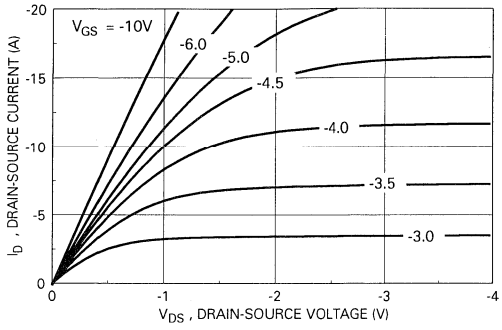


Figure 12. P-Channel On-Region Characteristics.

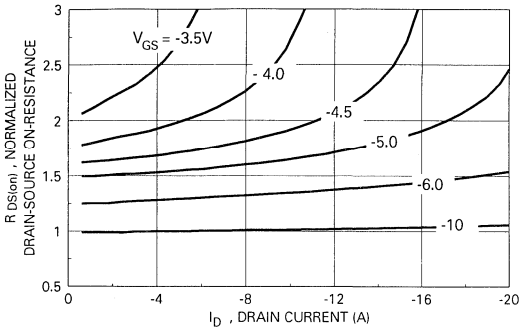


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

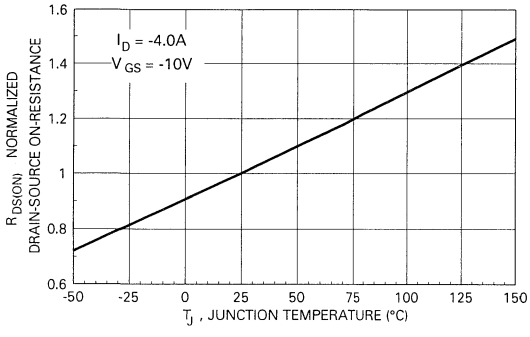


Figure 14. P-Channel On-Resistance Variation with Temperature.

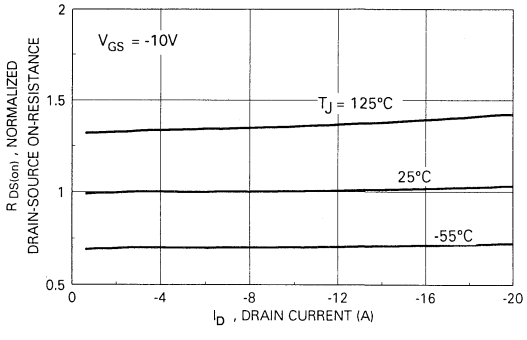


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

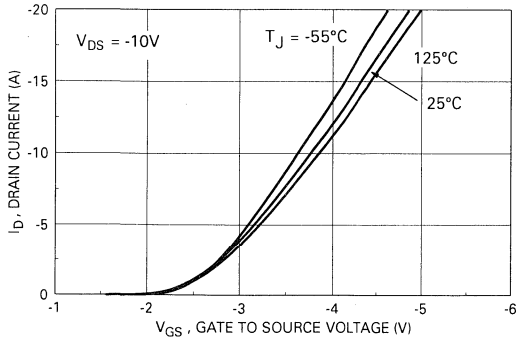


Figure 16. P-Channel Transfer Characteristics.

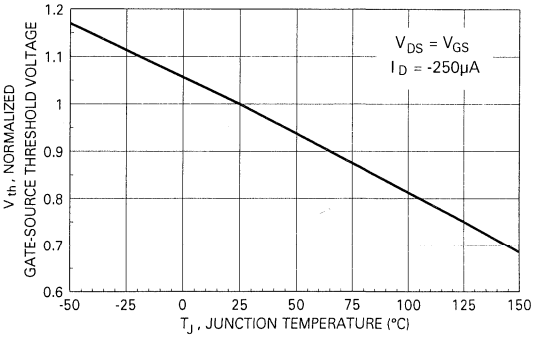


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

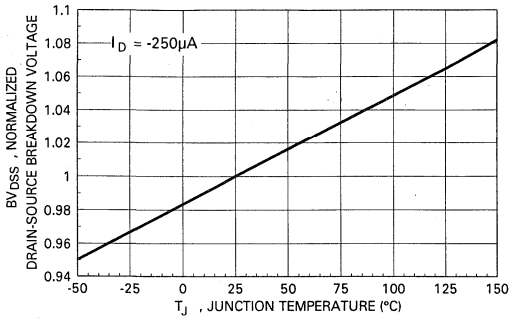


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

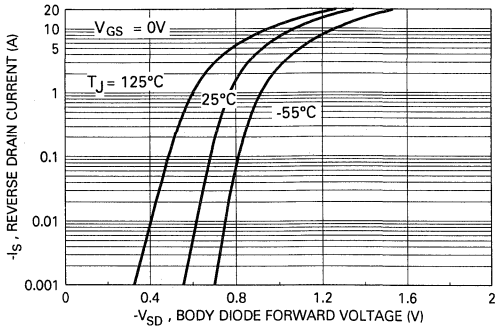


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

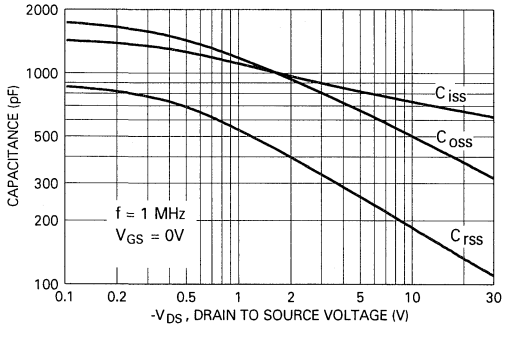


Figure 20. P-Channel Capacitance Characteristics.

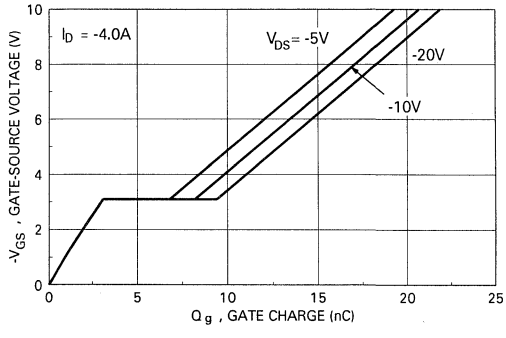


Figure 21. P-Channel Gate Charge Characteristic.

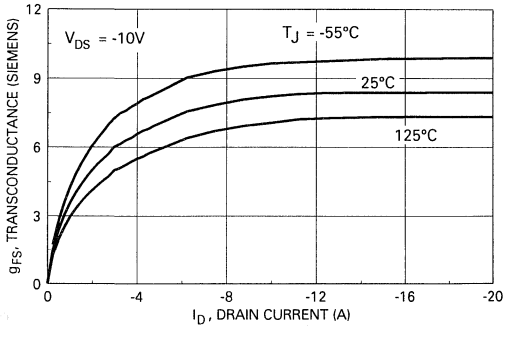


Figure 22. P-Channel Transconductance Variation with Drain Current and

Typical Thermal Characteristics: N & P-Channel

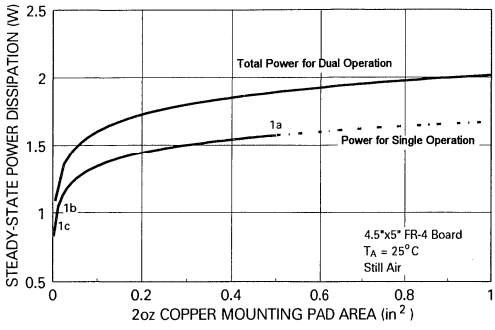


Figure 23. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

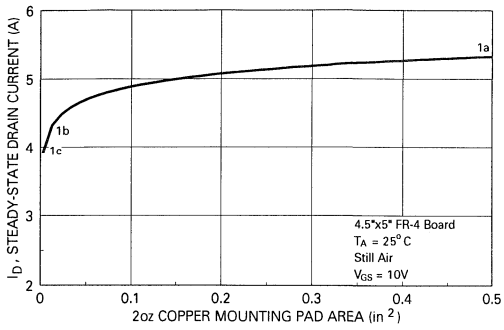


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

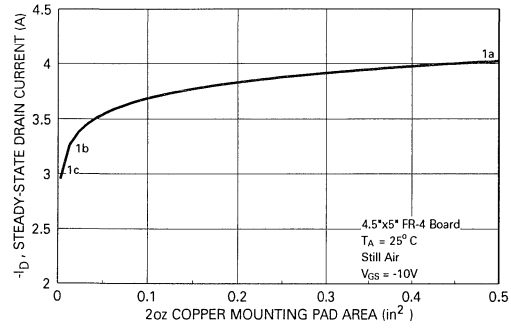


Figure 25. P-Ch Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

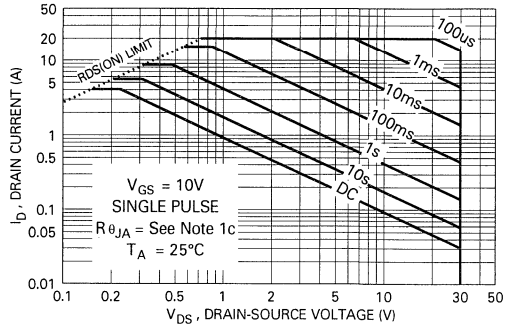


Figure 26. N-Channel Maximum Safe Operating Area.

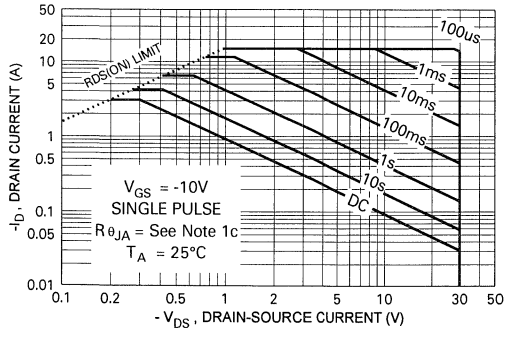


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

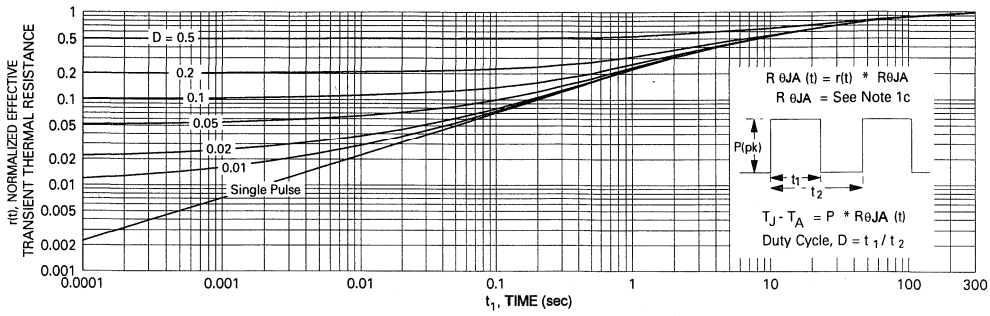


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

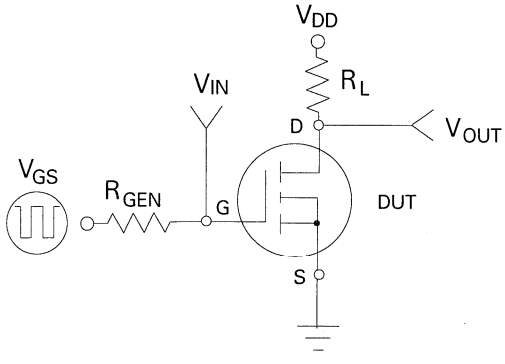


Figure 29. N or P-Channel Switching Test Circuit.

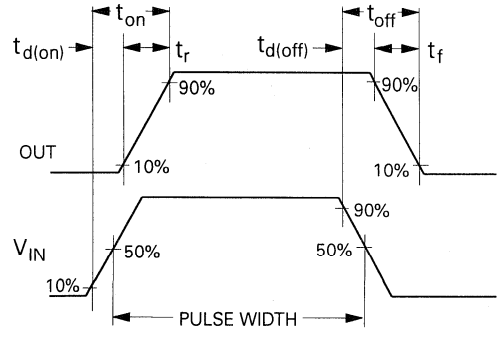


Figure 30. N or P-Channel Switching Waveforms.

National Semiconductor™

May 1996

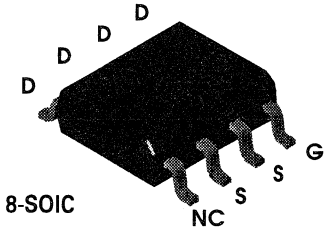
NDS9400A
Single P-Channel Enhancement Mode Field Effect Transistor

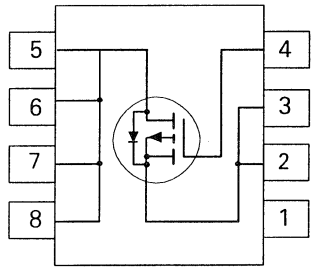
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.4A, -30V. $R_{DS(ON)}$ = 0.13Ω @ V_{GS} = -10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Rugged and reliable.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9400A	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 3.4	A
	- Pulsed		± 10	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-2	µA
		T_J = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.6	-2.8	V
		T_J = 125°C	-0.85	-1.25	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1.0 A		0.11	0.13	Ω
		T_J = 125°C		0.15	0.21	
		V_{GS} = -4.5 V, I_D = -0.5 A		0.17	0.2	
		T_J = 125°C		0.24	0.32	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-10			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -3.4 A		4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		350		pF
C_{oss}	Output Capacitance			260		pF
C_{rss}	Reverse Transfer Capacitance			100		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		9	40	ns
t_r	Turn - On Rise Time			21	40	ns
$t_{D(off)}$	Turn - Off Delay Time			21	90	ns
t_f	Turn - Off Fall Time			8	50	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -3.4 A, V_{GS} = -10 V		10	25	nC
Q_{gs}	Gate-Source Charge			1.6		nC
Q_{gd}	Gate-Drain Charge			3.4		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.9	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.25 A (Note 2)		-0.8	-1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = -2.0 A, dI_F/dt = 100 A/µs			100	ns
I_{rr}	Reverse Recovery Current			1.9		A

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

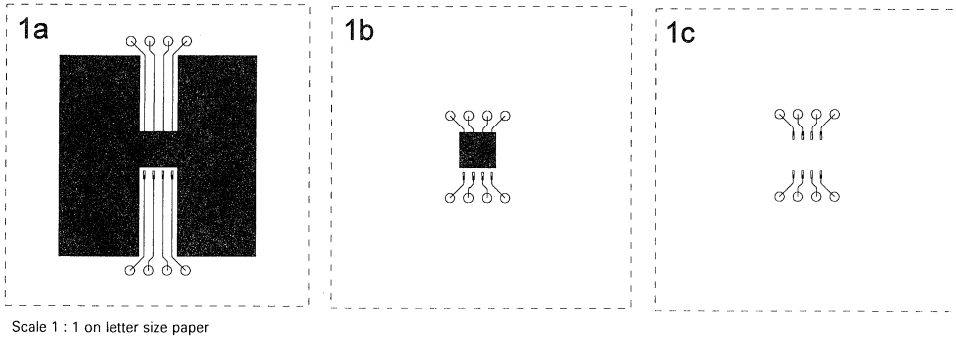
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

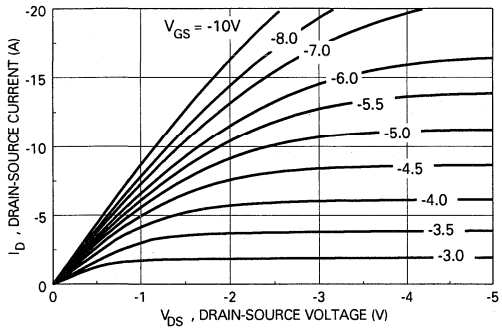


Figure 1. On-Region Characteristics.

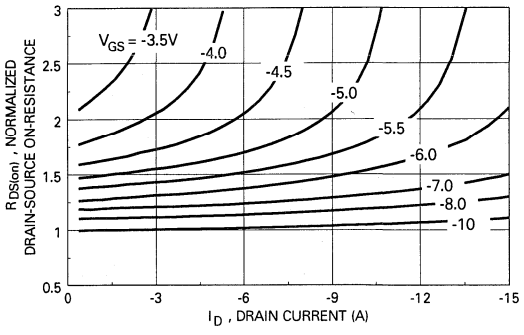


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

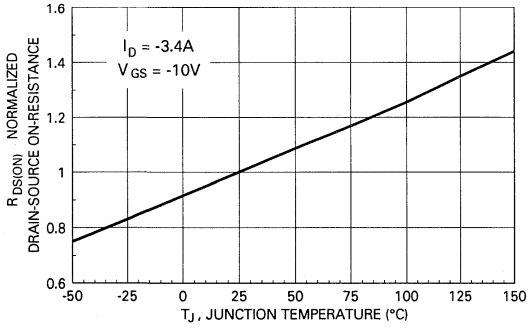


Figure 3. On-Resistance Variation with Temperature.

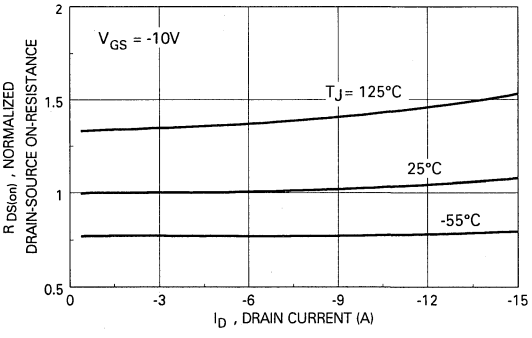


Figure 4. On-Resistance Variation with Drain Current and Temperature.

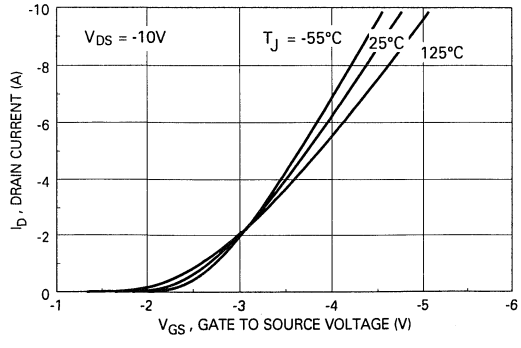


Figure 5. Transfer Characteristics.

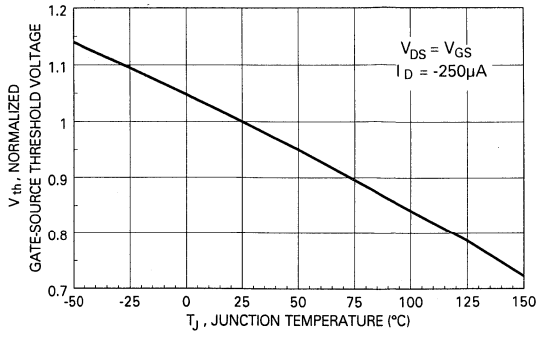


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

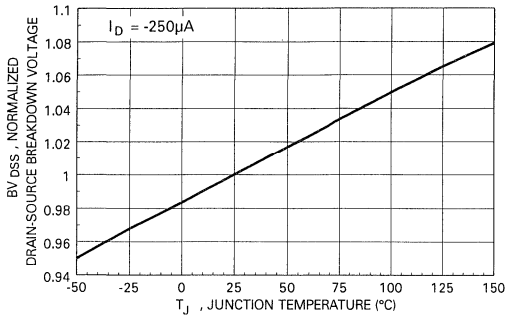


Figure 7. Breakdown Voltage Variation with Temperature.

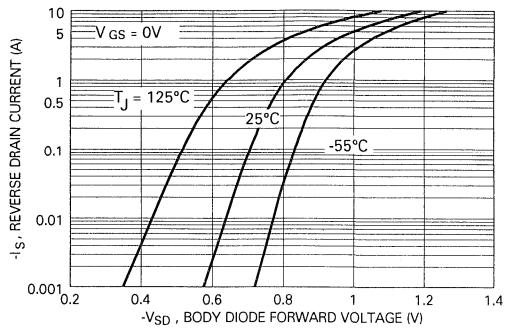


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

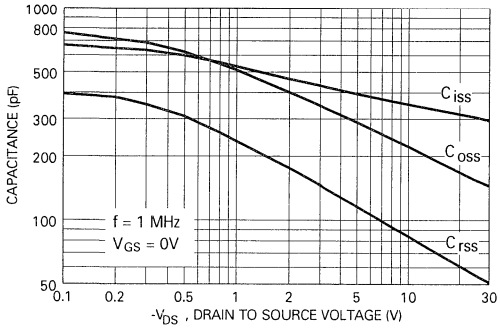


Figure 9. Capacitance Characteristics.

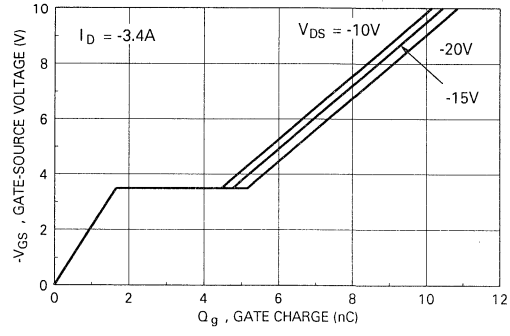


Figure 10. Gate Charge Characteristics.

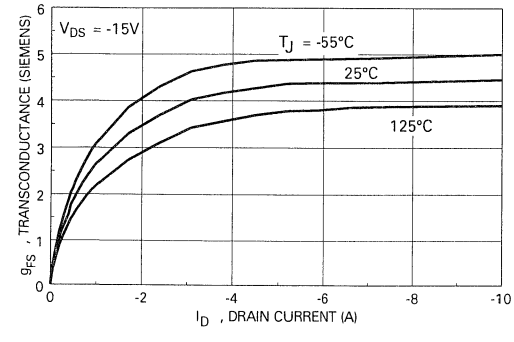


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

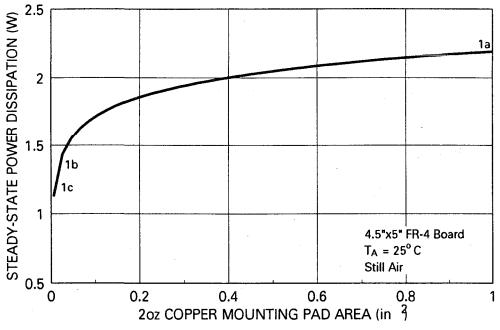


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

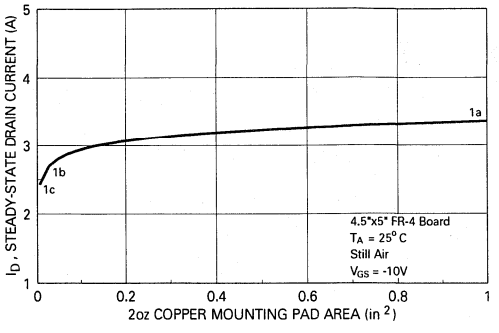


Figure 13. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

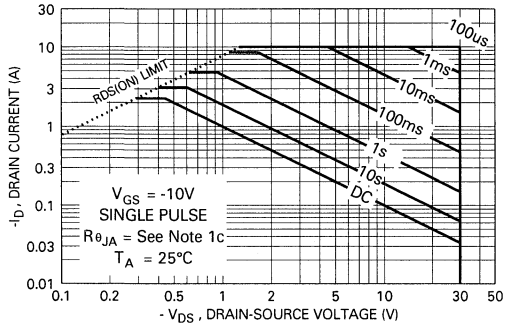


Figure 14. Maximum Safe Operating Area.

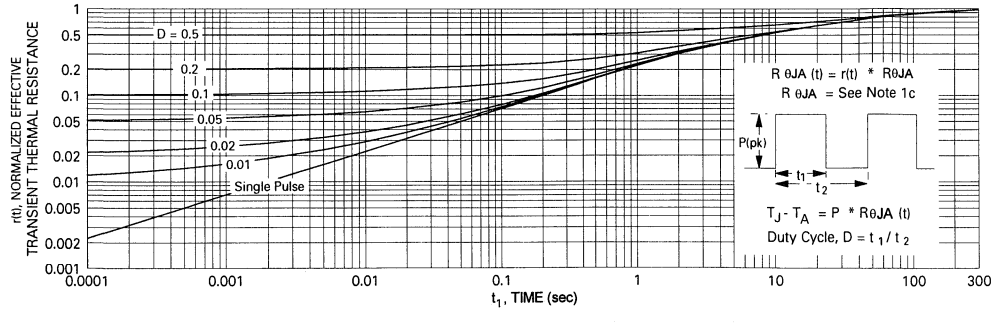


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

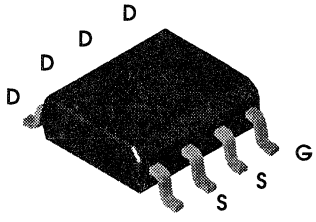
NDS9405
Single P-Channel Enhancement Mode Field Effect Transistor

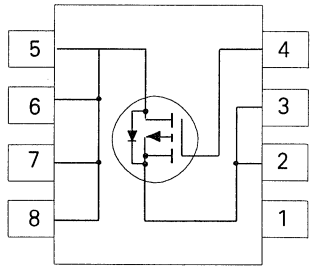
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is been especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -4.3A, -20V. $R_{DS(ON)}$ = 0.10Ω @ V_{GS} = -10V
- High density cell design for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9405	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 4.3	A
	- Continuous T_A = 70°C	(Note 1a)	± 3.3	
	- Pulsed T_A = 25°C		± 20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-2	µA
		T_J = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.5	-1.65	-3	V
		T_J = 125°C	-0.85		-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2 A		0.053	0.1	Ω
		T_J = 125°C		0.075	0.15	
		V_{GS} = -4.5 V, I_D = -2 A		0.08	0.16	
		T_J = 125°C		0.12	0.24	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-20			A
		V_{GS} = -4.5, V_{DS} = -5V	-5			
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -4.3 A		9		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1425		pF
C_{oss}	Output Capacitance			850		pF
C_{rss}	Reverse Transfer Capacitance			430		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		17	30	ns
t_r	Turn - On Rise Time			24	80	ns
$t_{D(off)}$	Turn - Off Delay Time			56	200	ns
t_f	Turn - Off Fall Time			30	200	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -4.3 A, V_{GS} = -10 V			40	nC
Q_{gs}	Gate-Source Charge				5	nC
Q_{gd}	Gate-Drain Charge				25	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.25 A (Note 2)		-0.78	-1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = -1.25 A, dI_F/dt = 100 A/µs		80		ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

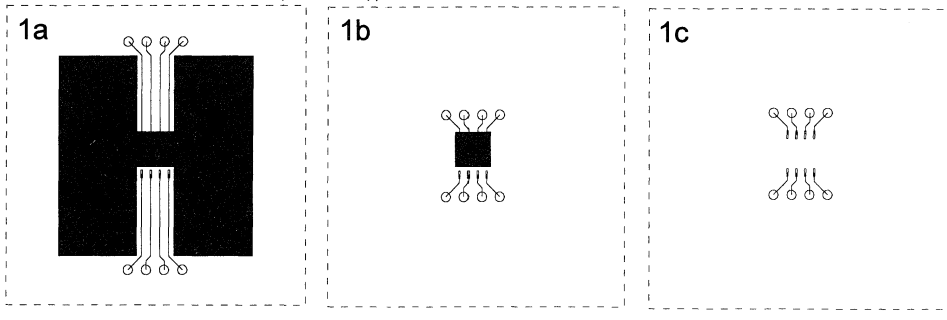
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

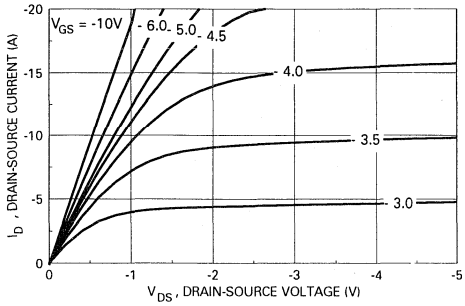


Figure 1. On-Region Characteristics

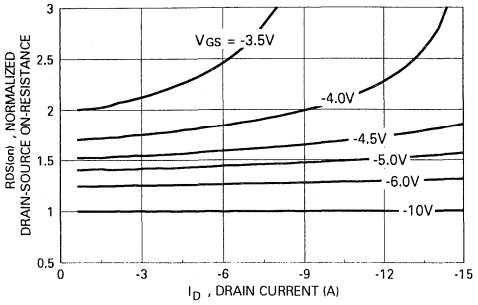


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

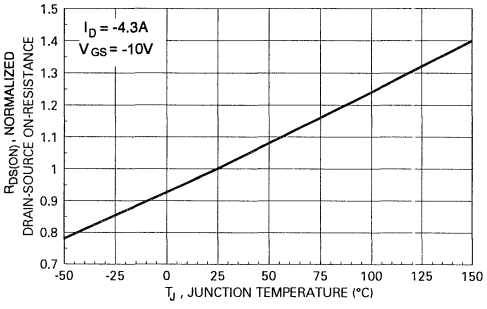


Figure 3. On-Resistance Variation with Temperature

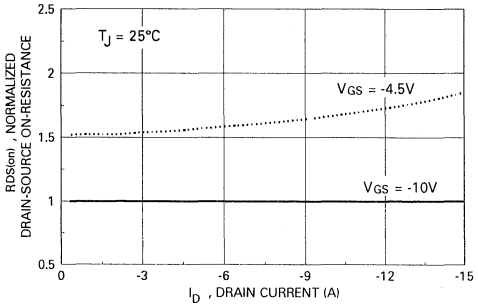


Figure 4. On-Resistance Variation with Drain Current

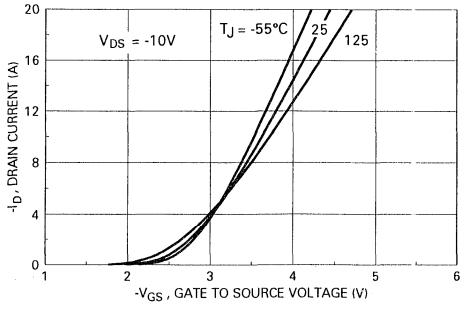


Figure 5. Transfer Characteristics

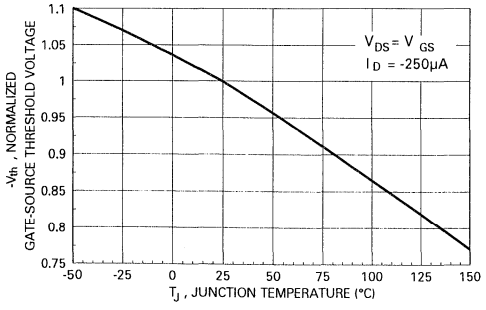


Figure 6. Gate Threshold Variation with Temperature

4

Typical Electrical Characteristics (continued)

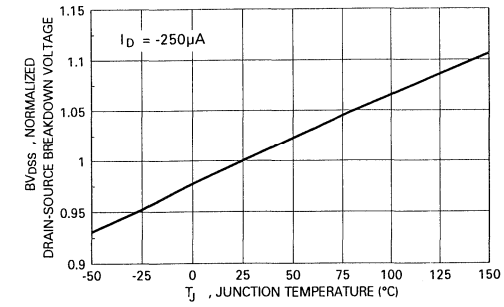


Figure 7. Breakdown Voltage Variation with Temperature

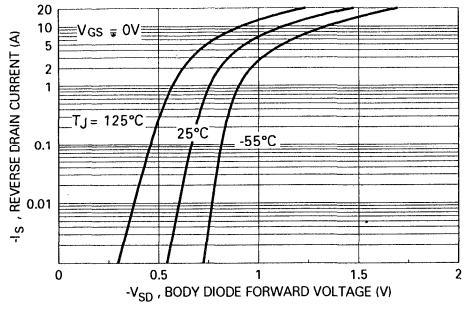


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

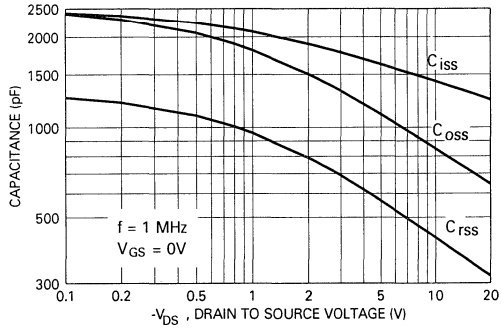


Figure 9. Capacitance Characteristics

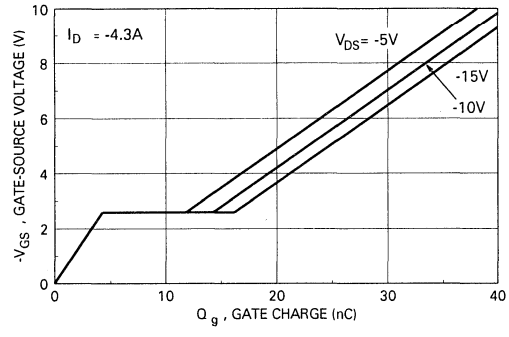


Figure 10. Gate Charge Characteristics

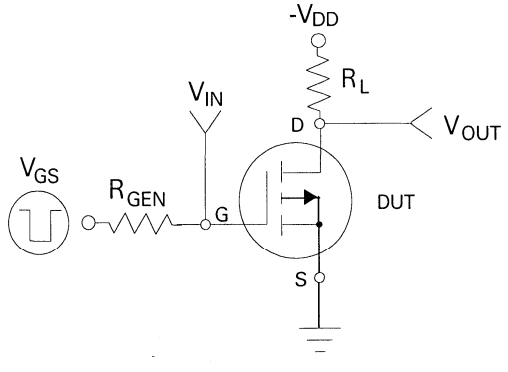


Figure 11. Switching Test Circuit

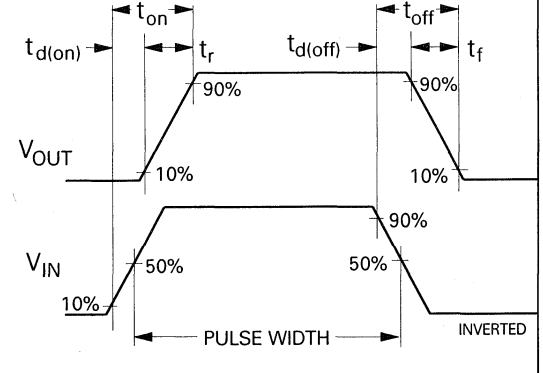


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

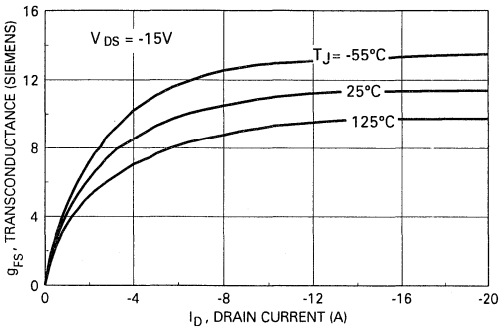


Figure 13. Transconductance Variation with Drain Current and Temperature

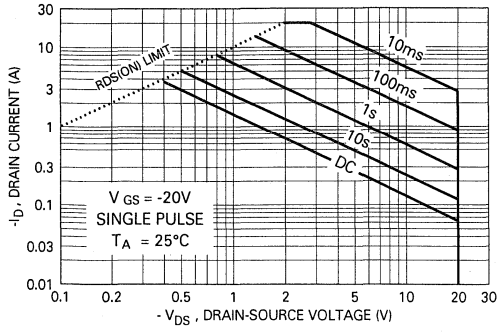


Figure 14. Maximum Safe Operating Area

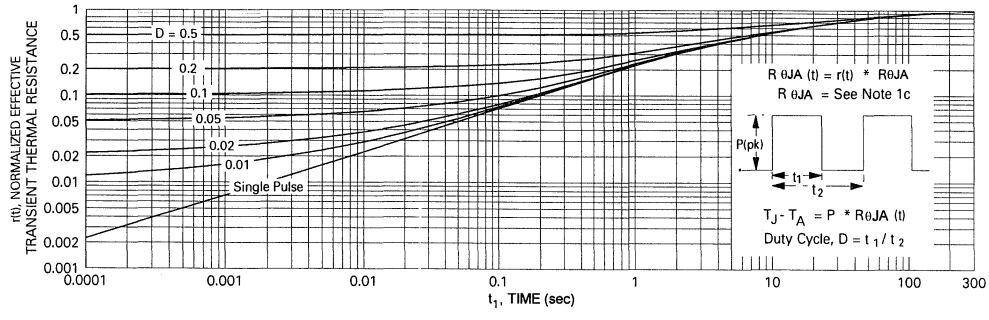


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

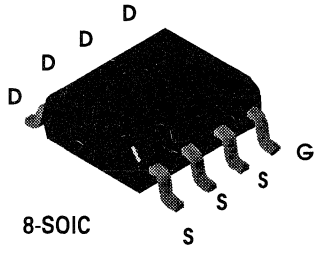
NDS9407
Single P-Channel Enhancement Mode Field Effect Transistor

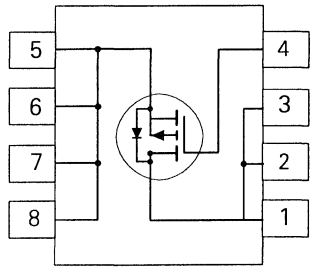
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.0A, -60V. $R_{DS(ON)}$ = 0.15Ω @ V_{GS}=-10V
  $R_{DS(ON)}$ = 0.24Ω @ V_{GS}=-4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9407	Units
V_{DSS}	Drain-Source Voltage		-60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 3.0	A
	- Continuous T_A = 70°C		± 2.4	
	- Pulsed T_A = 25°C		± 12	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_A = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2.3		V
		T_A = 125°C	-0.8	-1.8		
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -3.0 A		0.08	0.15	Ω
		T_A = 125°C		0.13	0.3	
		V_{GS} = -4.5 V, I_D = -1.6 A		0.135	0.24	
		T_A = 125°C		0.2	0.48	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-12			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -3.0 A		6.8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -30 V, V_{GS} = 0 V, f = 1.0 MHz		1400		pF
C_{oss}	Output Capacitance			290		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -25 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		12	30	ns
t_r	Turn - On Rise Time			12	40	ns
$t_{D(off)}$	Turn - Off Delay Time			55	100	ns
t_f	Turn - Off Fall Time			22	45	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -3.0 A, V_{GS} = -10 V		37	50	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			10		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.5 A (Note 2)		-0.9	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

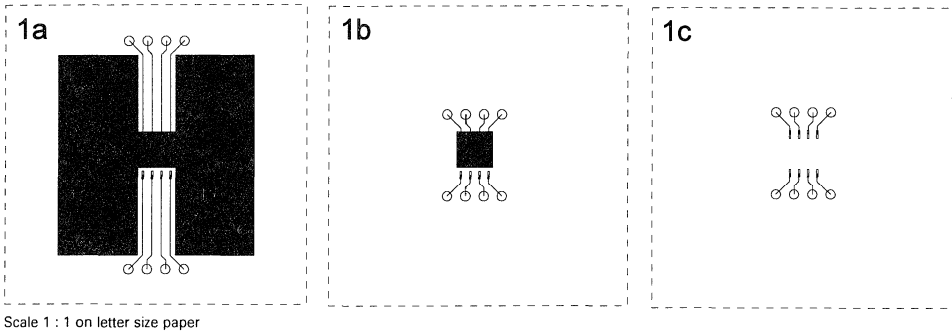
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

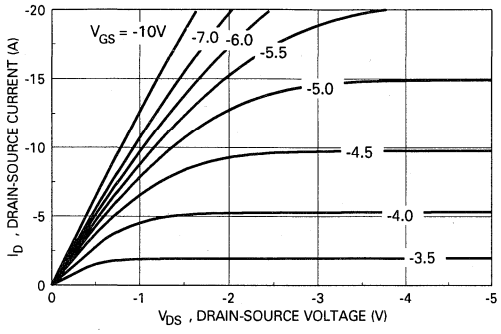


Figure 1. On-Region Characteristics.

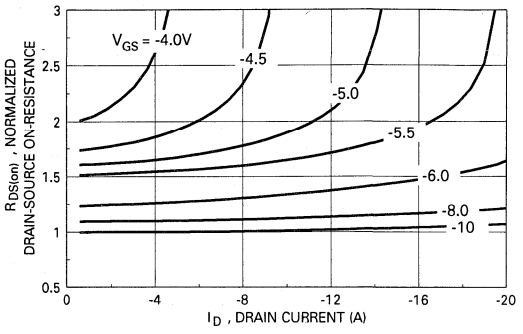


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

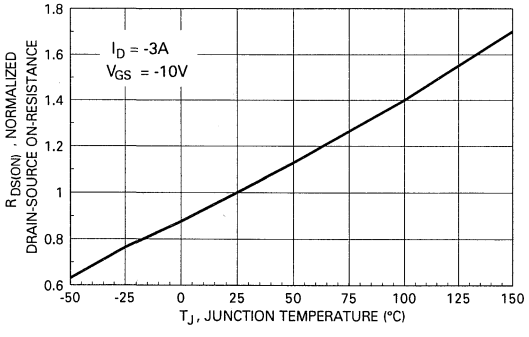


Figure 3. On-Resistance Variation with Temperature.

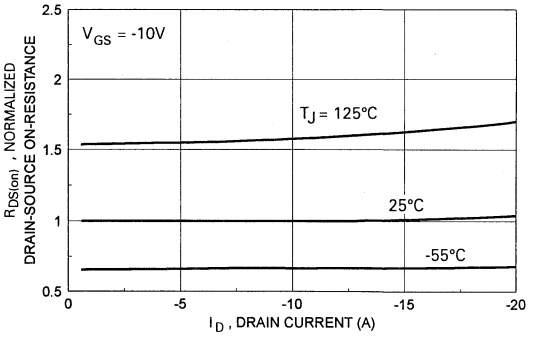


Figure 4. On-Resistance Variation with Drain Current and Temperature.

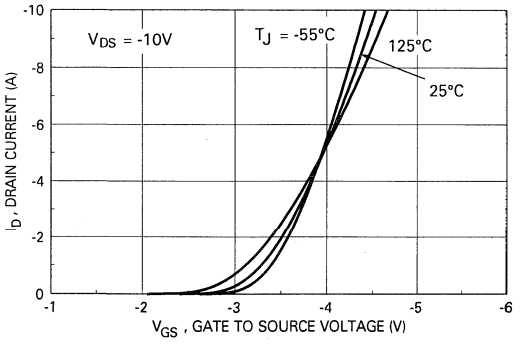


Figure 5. Transfer Characteristics.

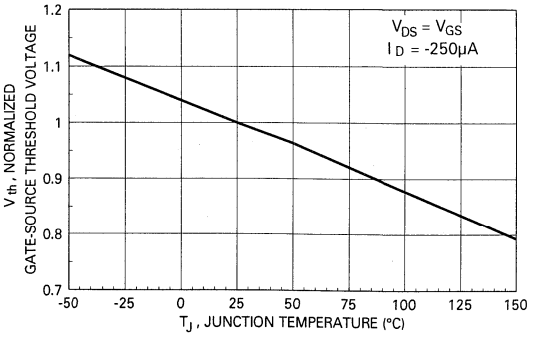


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

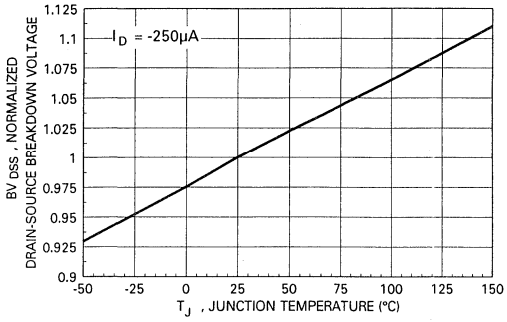


Figure 7. Breakdown Voltage Variation with Temperature.

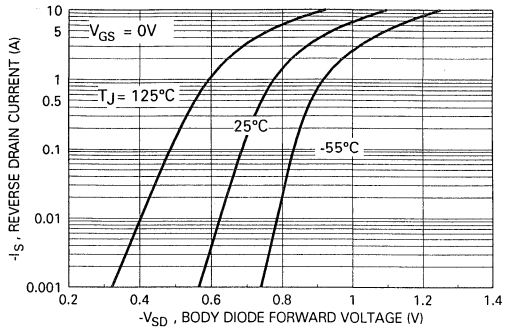


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

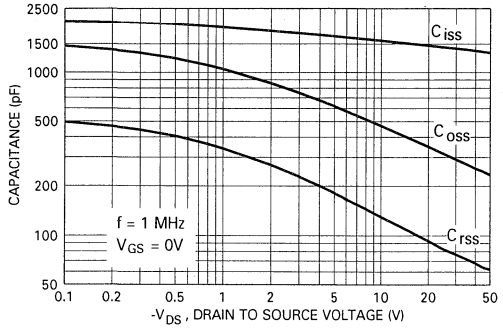


Figure 9. Capacitance Characteristics.

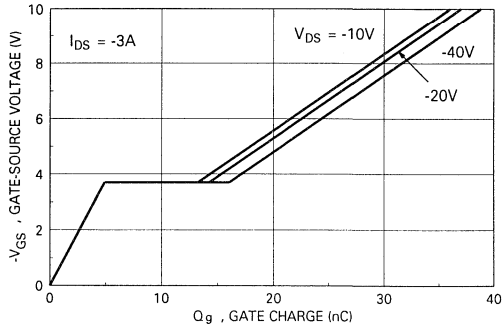


Figure 10. Gate Charge Characteristics.

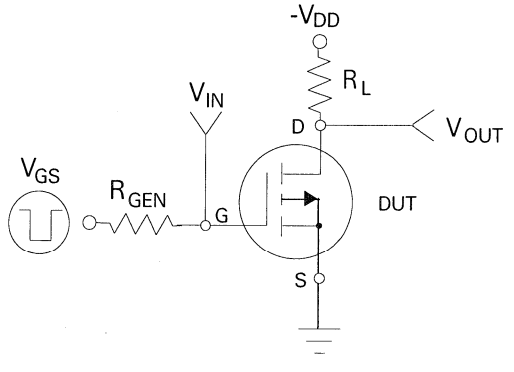


Figure 11. Switching Test Circuit

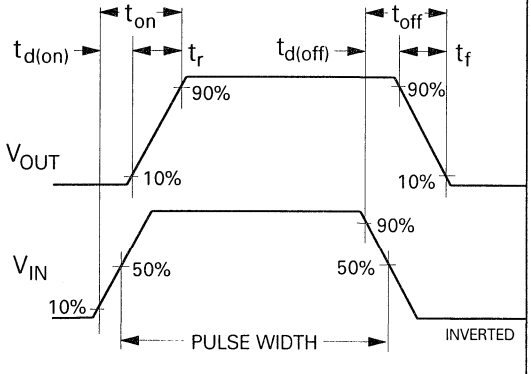


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

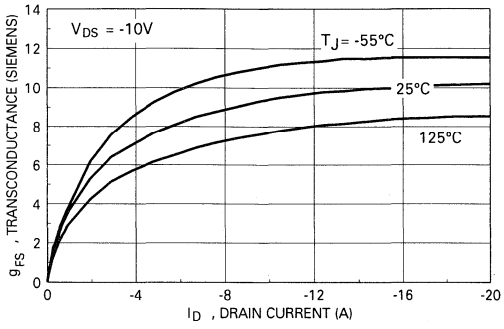


Figure 13. Transconductance Variation with Drain Current and Temperature

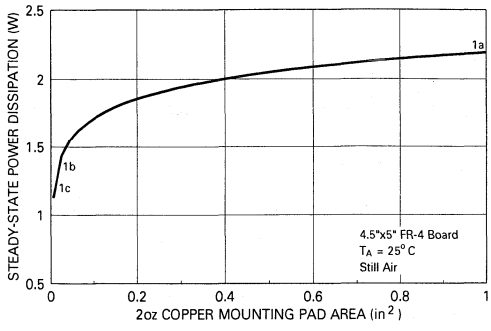


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

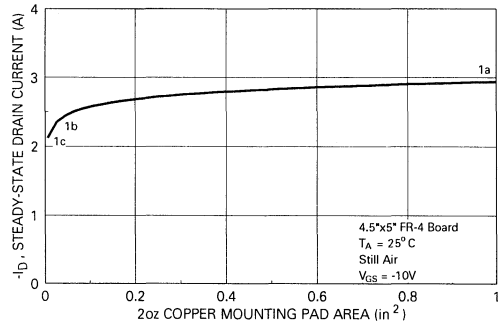


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

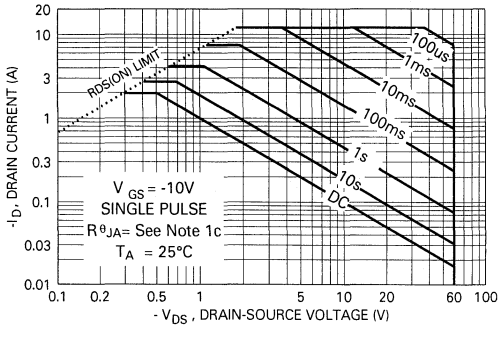


Figure 16. Maximum Safe Operating Area

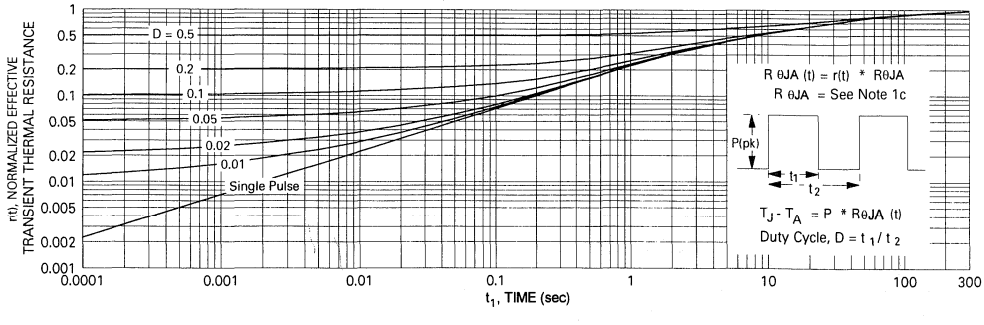


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

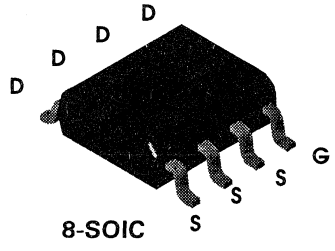
NDS9410A
Single N-Channel Enhancement Mode Field Effect Transistor

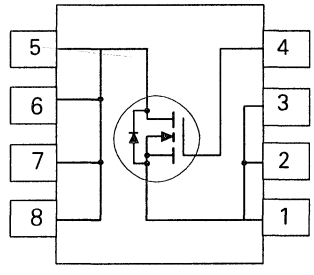
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 7.3A, 30V. $R_{DS(ON)}$ = 0.028Ω @ V_{GS} = 10V.
  $R_{DS(ON)}$ = 0.042Ω @ V_{GS} = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9410A	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 7.3	A
	- Pulsed		± 20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		T_J = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	2	3	V
		T_J = 125°C	0.7	1.5	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.3 A		0.022	0.028	Ω
		T_J = 125°C		0.03	0.045	
		V_{GS} = 4.5 V, I_D = 6.3 A		0.035	0.042	
		T_J = 125°C		0.047	0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 7.3 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		890		pF
C_{oss}	Output Capacitance			560		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		10	30	ns
t_r	Turn - On Rise Time			20	60	ns
$t_{D(off)}$	Turn - Off Delay Time			40	150	ns
t_f	Turn - Off Fall Time			35	140	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 2 A, V_{GS} = 10 V		28	50	nC
Q_{gs}	Gate-Source Charge			3.9		nC
Q_{gd}	Gate-Drain Charge			12.6		nC

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.3 A (Note 2)		0.78	1.1	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2 A, dI_F/dt = 100A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

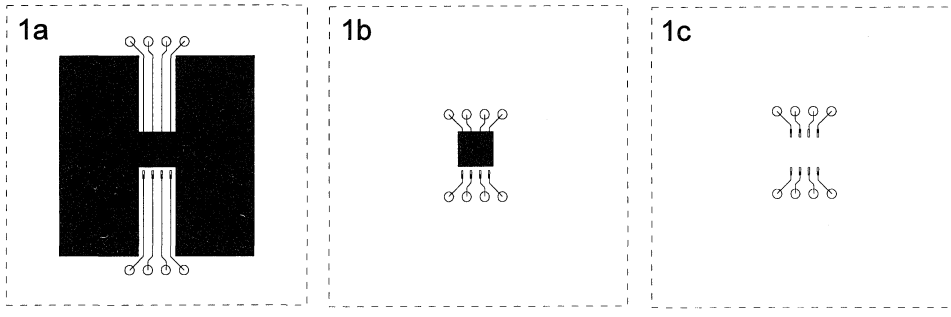
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

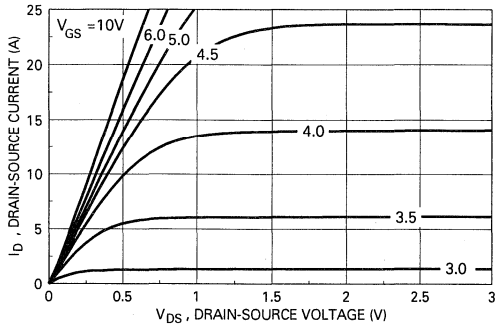


Figure 1. On-Region Characteristics.

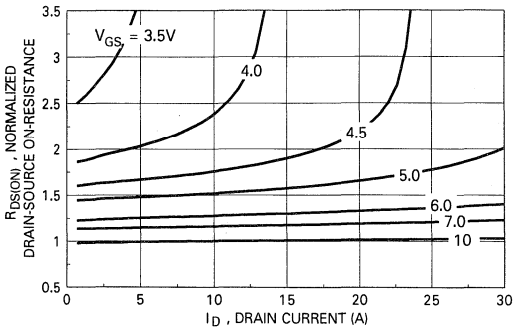


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

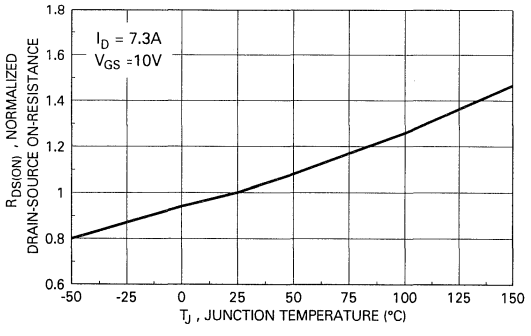


Figure 3. On-Resistance Variation with Temperature.

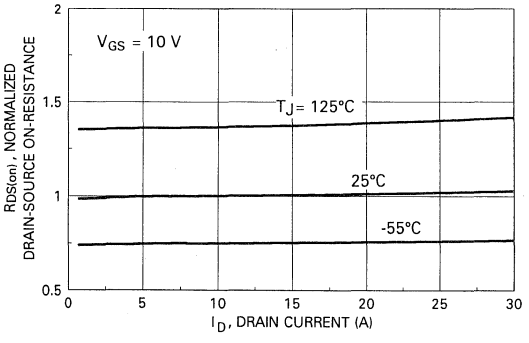


Figure 4. On-Resistance Variation with Drain Current and Temperature.

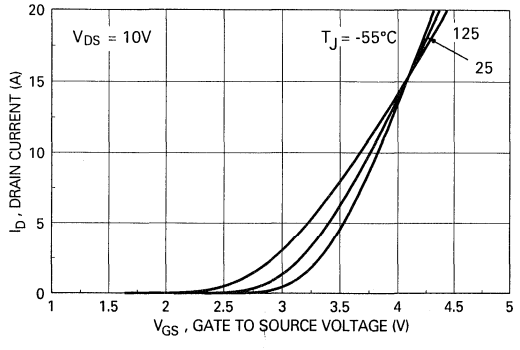


Figure 5. Transfer Characteristics.

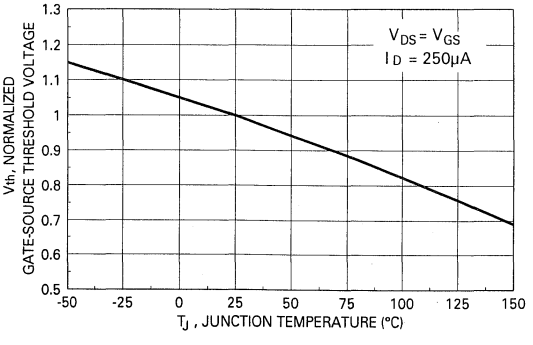


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

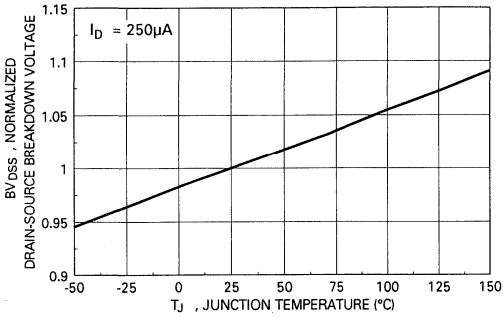


Figure 7. Breakdown Voltage Variation with Temperature.

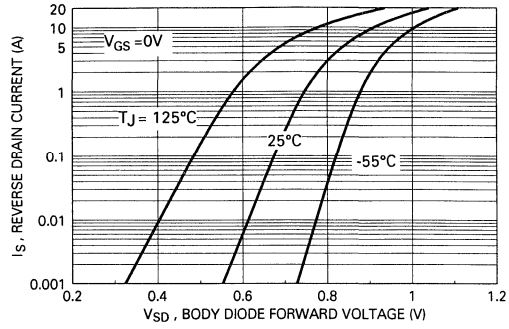


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

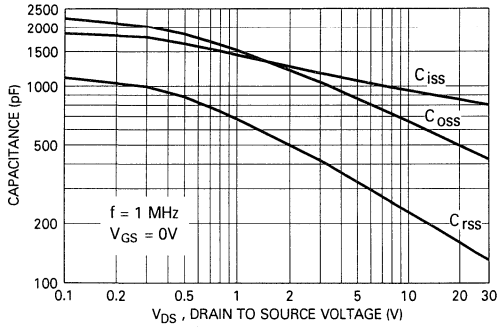


Figure 9. Capacitance Characteristics.

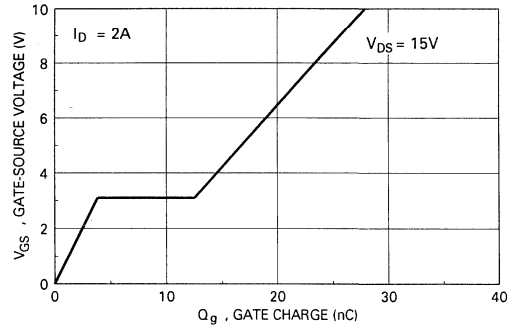


Figure 10. Gate Charge Characteristics.

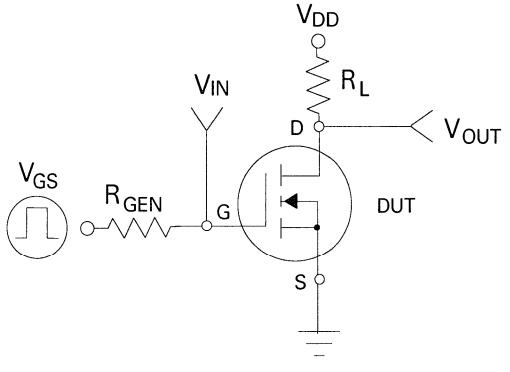


Figure 11. Switching Test Circuit

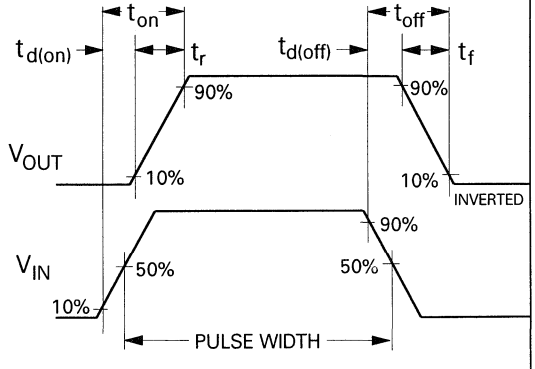


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics

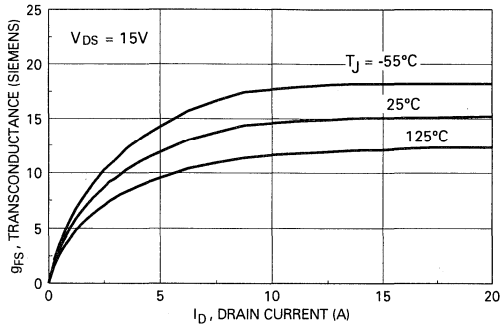


Figure 13. Transconductance Variation with Drain Current and Temperature.

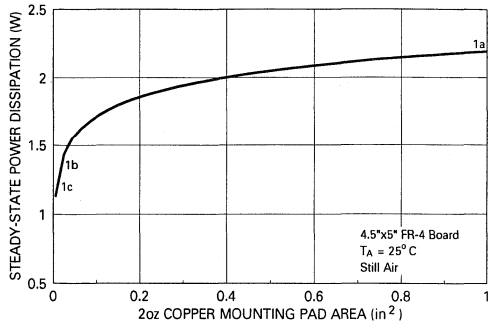


Figure 14. SO-8 Single Device Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

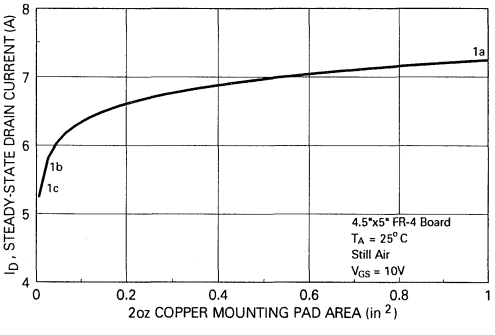


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

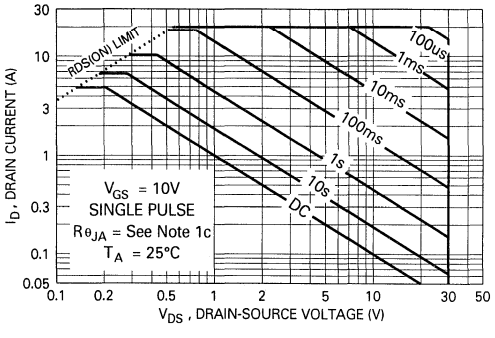


Figure 16. Maximum Safe Operating Area.

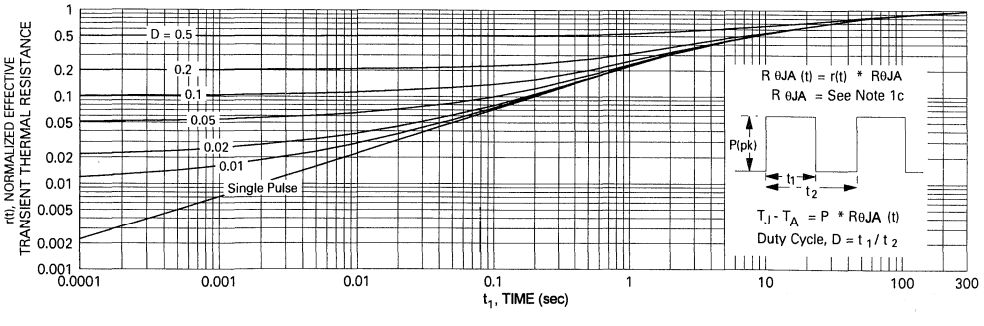


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

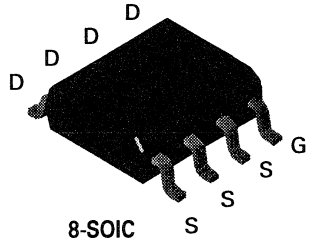
NDS9430
Single P-Channel Enhancement Mode Field Effect Transistor

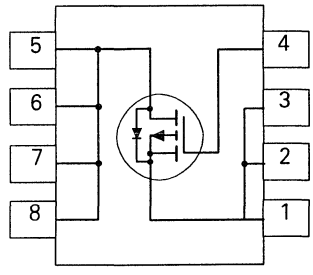
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -5.3A, -20V. $R_{DS(ON)}$ = 0.06Ω @ V_{GS} = -10V.
- High density cell design for extremely low $R_{DS(ON)}$
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9430	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 5.3	A
	- Continuous T_A = 70°C	(Note 1a)	± 4.2	
	- Pulsed T_A = 25°C		± 15	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2	-3	V
		T_J=125°C	-0.85	-1.7	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.3 A		0.055	0.06	Ω
		T_J=125°C		0.077	0.09	
		V_{GS} = -6 V, I_D = -3.6 A		0.067	0.08	
		V_{GS} = -4.5 V, I_D = -2 A		0.082	0.115	
		T_J=125°C		0.12	0.19	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5, V_{DS} = -5V	-3.6			
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -5.3 A		8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		1430		pF
C_{oss}	Output Capacitance			810		pF
C_{rss}	Reverse Transfer Capacitance			375		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		13	30	ns
t_r	Turn - On Rise Time			22	60	ns
$t_{D(off)}$	Turn - Off Delay Time			66	120	ns
t_f	Turn - Off Fall Time			28	100	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -5.3 A, V_{GS} = -10 V		38		nC
Q_{gs}	Gate-Source Charge			3		nC
Q_{gd}	Gate-Drain Charge			12		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -5.3 A (Note 2)		-1.04	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = -5.3 A, dI_F/dt = 100 A/µs		80	100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

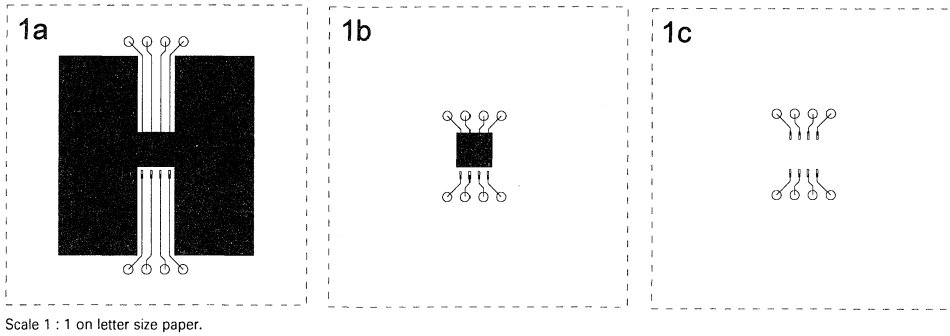
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

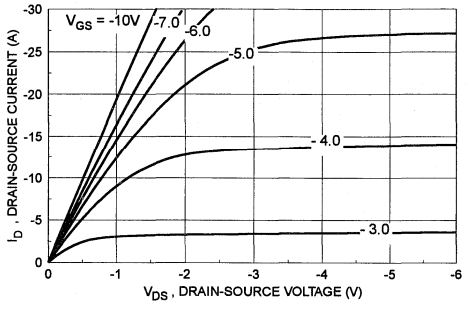


Figure 1. On-Region Characteristics

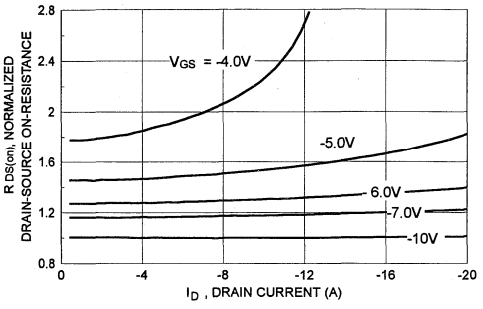


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

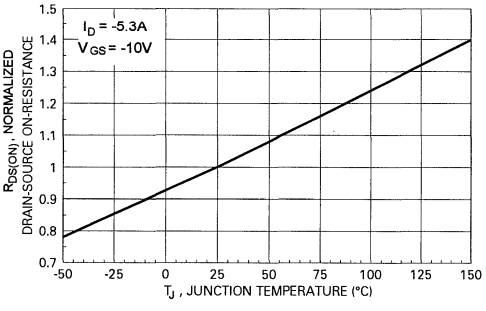


Figure 3. On-Resistance Variation with Temperature

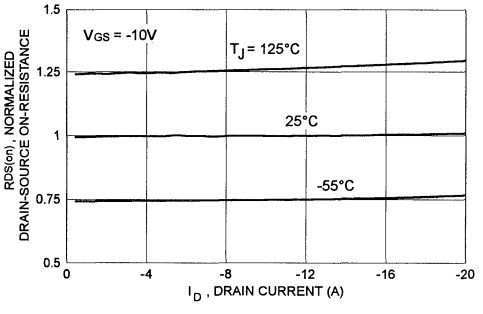


Figure 4. On-Resistance Variation with Drain Current and Temperature

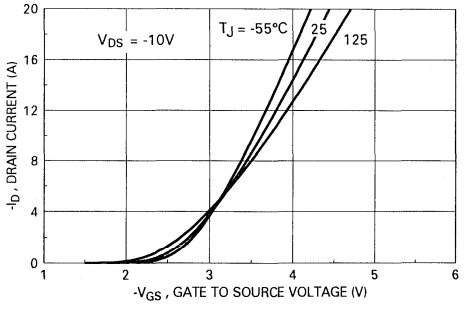


Figure 5. Transfer Characteristics

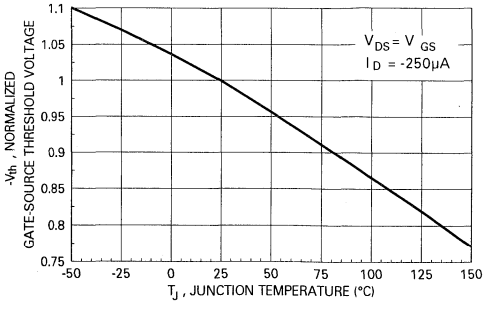


Figure 6. Gate Threshold Variation with Temperature

4

Typical Electrical Characteristics (continued)

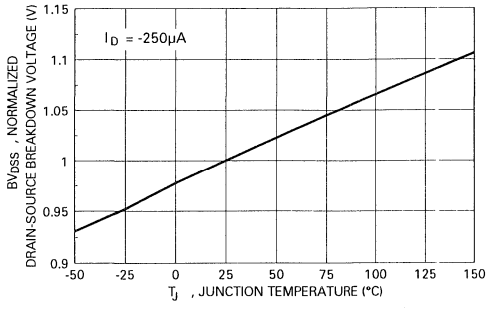


Figure 7. Breakdown Voltage Variation with Temperature

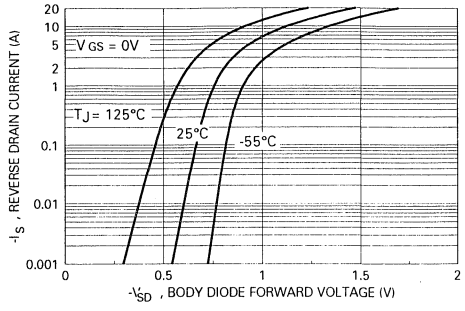


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

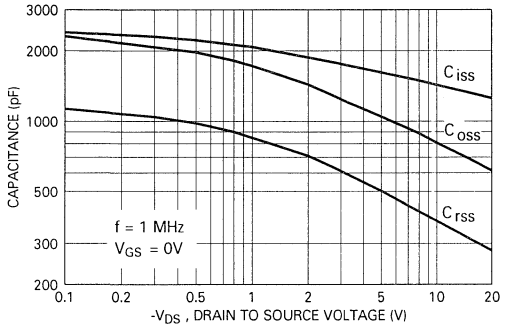


Figure 9. Capacitance Characteristics

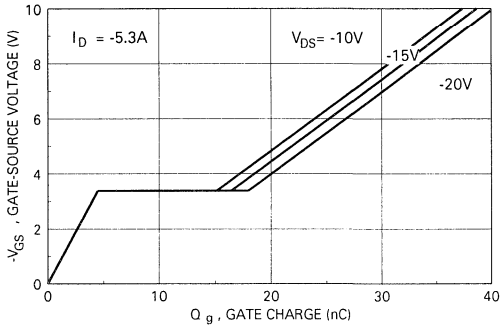


Figure 10. Gate Charge Characteristics

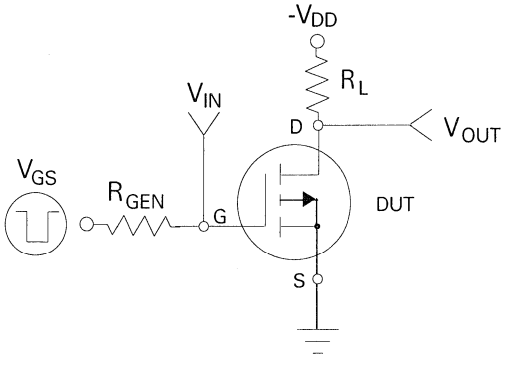


Figure 11. Switching Test Circuit

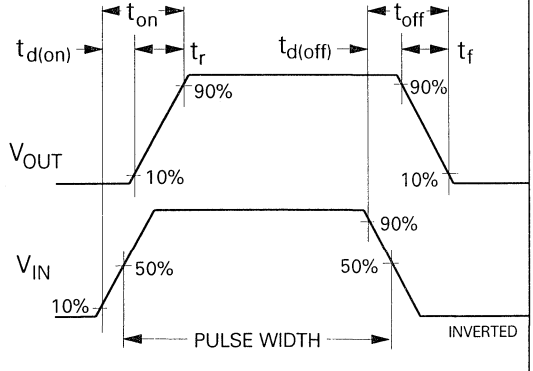


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

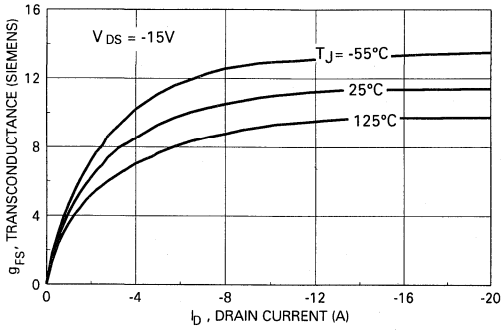


Figure 13. Transconductance Variation with Drain Current and Temperature

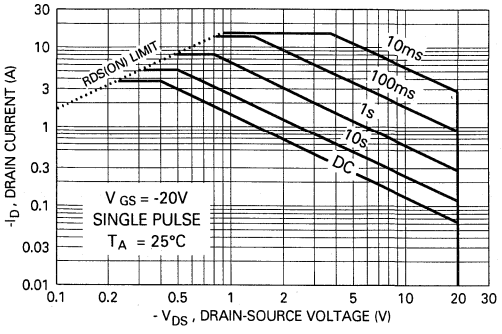


Figure 14. Maximum Safe Operating Area

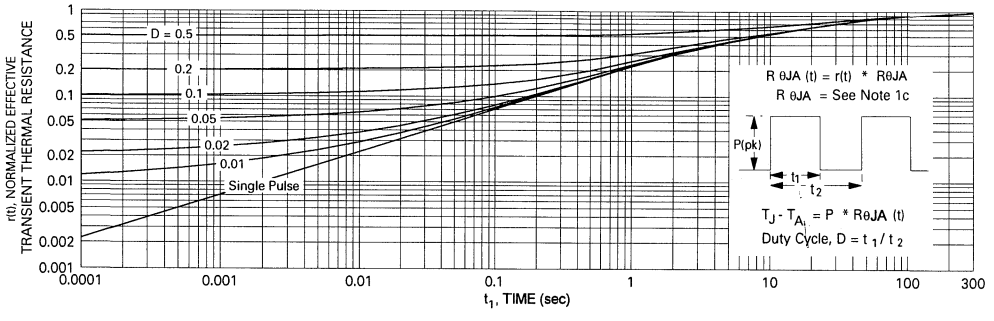


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

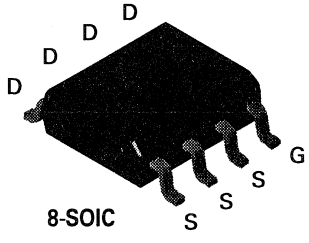
NDS9435A
Single P-Channel Enhancement Mode Field Effect Transistor

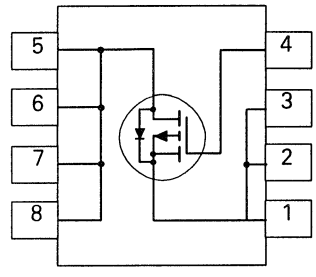
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -5.3A, -30V. $R_{DS(ON)}$ = 0.05Ω @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.07Ω @ V_{GS} = -6V
  $R_{DS(ON)}$ = 0.09Ω @ V_{GS} = -4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9435A	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 5.3	A
	- Pulsed		± 20	
P_D	Maximum Power Dissipation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -15 V, V_{GS} = 0 V, T_J = 70°C			-5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.4		V
		T_J = 125°C	-0.7	-1		
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.3 A		0.038	0.05	Ω
		T_J = 125°C		0.054	0.1	
		V_{GS} = -6 V, I_D = -4.7 A		0.046	0.07	
		V_{GS} = -4.5 V, I_D = -4.2 A		0.064	0.09	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-20			A
		V_{GS} = -4.5, V_{DS} = -5V	-5			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 5.3 A		10		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		950		pF
C_{oss}	Output Capacitance			610		pF
C_{rss}	Reverse Transfer Capacitance			220		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		10	30	ns
t_r	Turn - On Rise Time			18	60	ns
$t_{D(off)}$	Turn - Off Delay Time			80	120	ns
t_f	Turn - Off Fall Time			45	100	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -5.3 A, V_{GS} = -10 V		29	40	nC
Q_{gs}	Gate-Source Charge			3		nC
Q_{gd}	Gate-Drain Charge			9		nC

4

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.9	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -5.3 A (Note 2)		0.85	-1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = -5.3 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

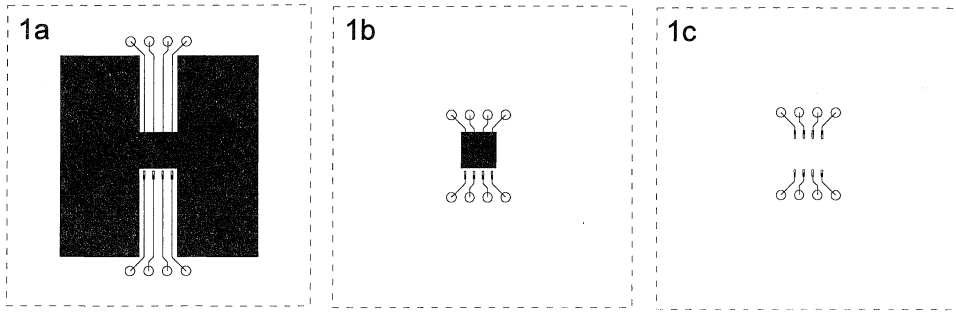
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in² pad of 2oz copper.

b. 105°C/W when mounted on a 0.04 in² pad of 2oz copper.

c. 125°C/W when mounted on a 0.006 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

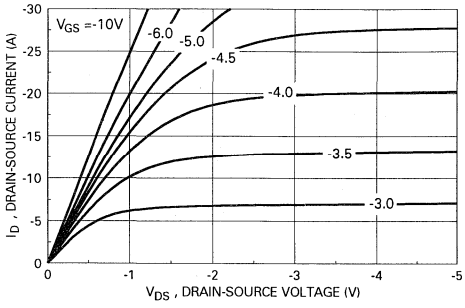


Figure 1. On-Region Characteristics

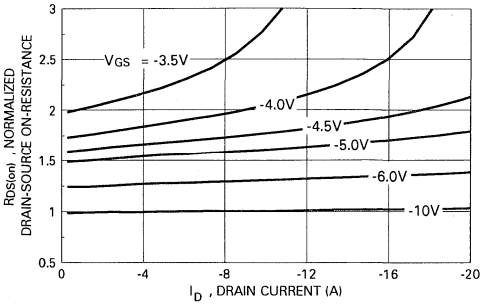


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

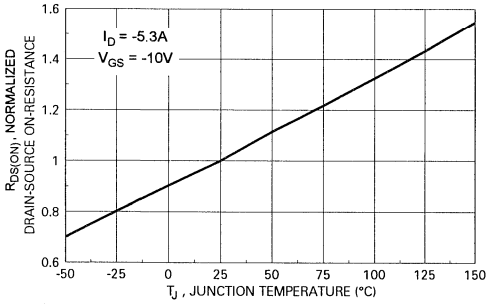


Figure 3. On-Resistance Variation with Temperature

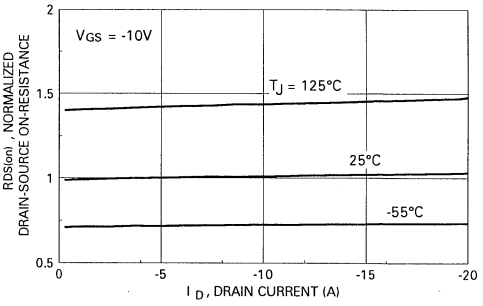


Figure 4. On-Resistance Variation with Drain Current and Temperature

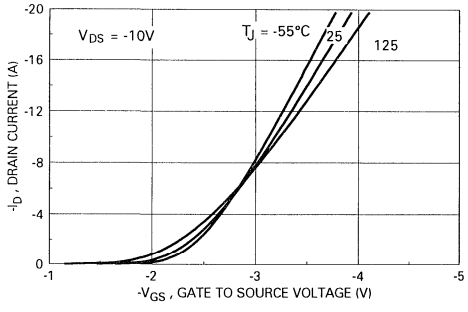


Figure 5. Transfer Characteristics

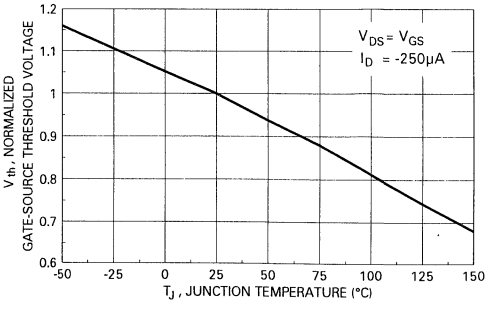


Figure 6. Gate Threshold Variation with Temperature

4

Typical Electrical Characteristics (continued)

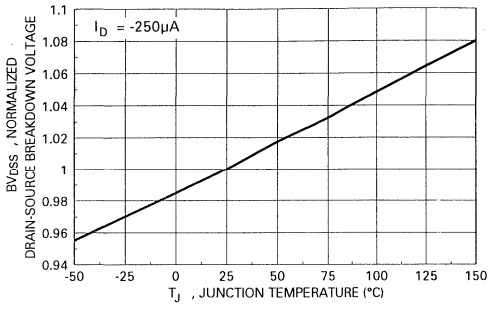


Figure 7. Breakdown Voltage Variation with Temperature

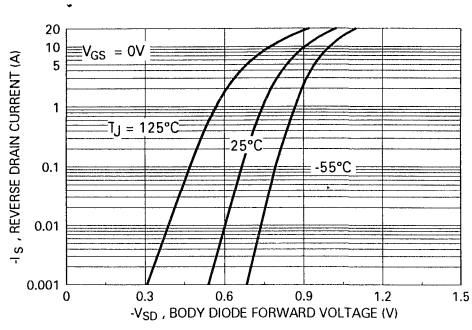


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

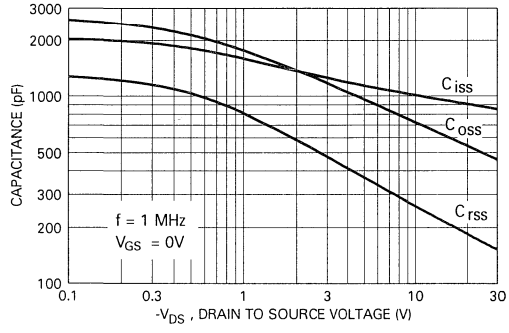


Figure 9. Capacitance Characteristics

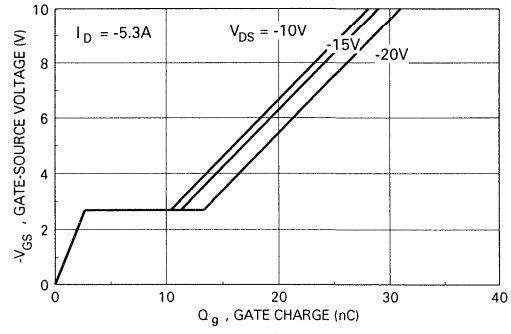


Figure 10. Gate Charge Characteristics

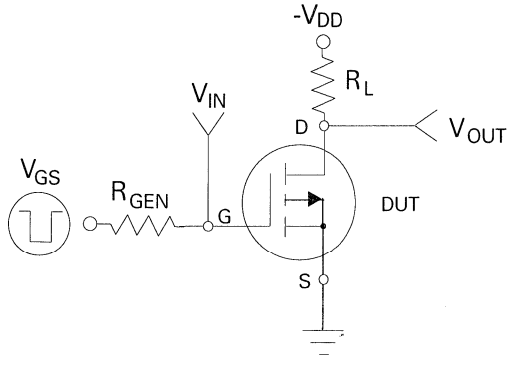


Figure 11. Switching Test Circuit

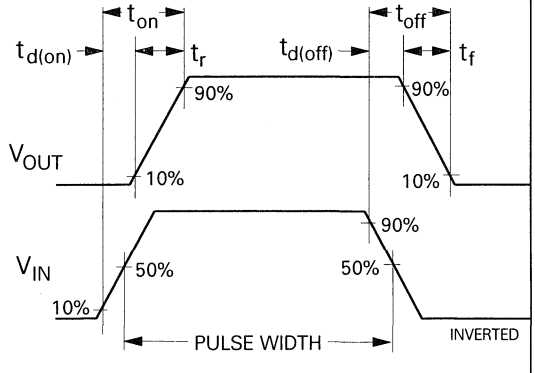


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics (continued)

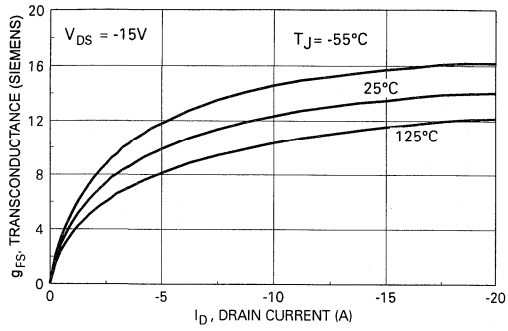


Figure 13. Transconductance Variation with Drain Current and Temperature

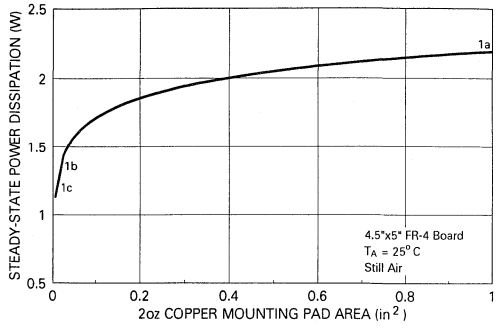


Figure 14. SO-8 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

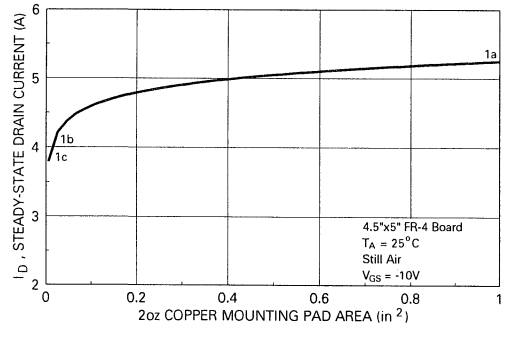


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

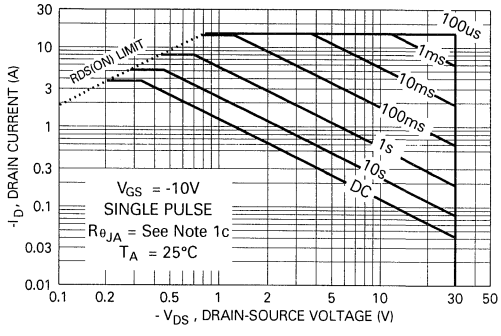


Figure 16. Maximum Safe Operating Area

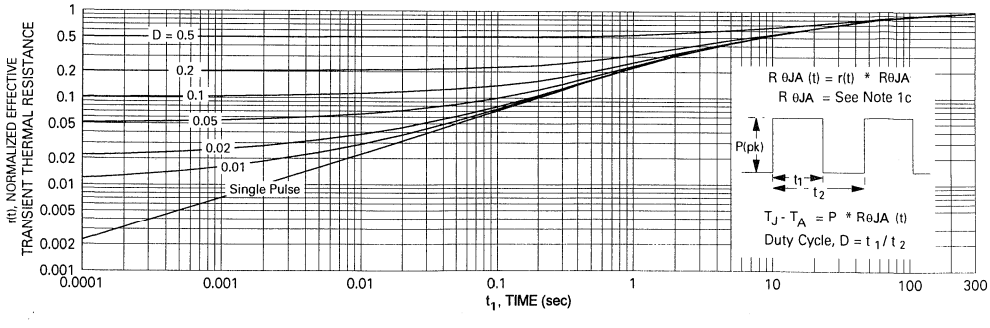


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996
ADVANCE INFORMATION

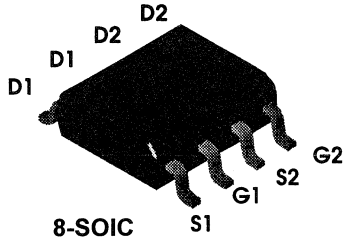
NDS9925A
Dual N-Channel Enhancement Mode Field Effect Transistor

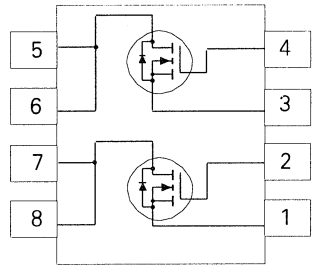
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 4.5A, 20V. $R_{DS(ON)}$ = 0.06Ω @ V_{GS} = 4.5V
  $R_{DS(ON)}$ = 0.075Ω @ V_{GS} = 2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise not

Symbol	Parameter	NDS9925A	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	8	V
I_D	Drain Current - Continuous (Note 1a)	4.5	A
	- Pulsed	15	
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a)	1.6	
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.4		1	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 4.5 A			0.06	Ω
		V_{GS} = 2.7 V, I_D = 1 A			0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	15			A
		V_{GS} = 2.7 V, V_{DS} = 5 V	5			
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)			1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

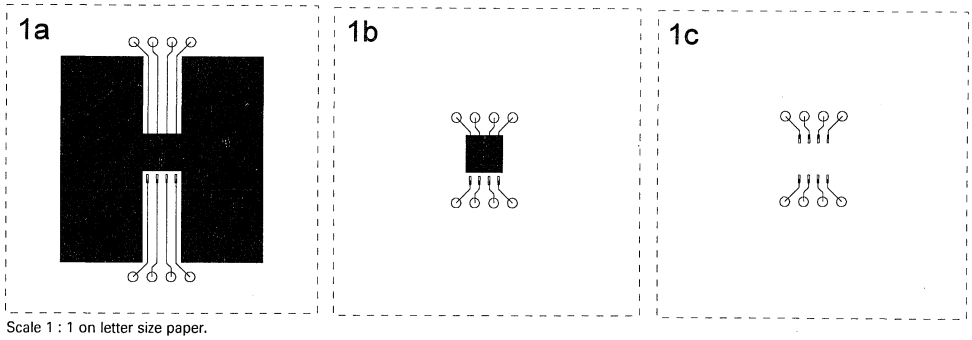
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

May 1996

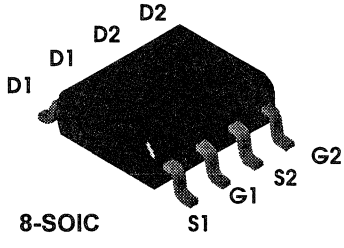
NDS9933
Dual P-Channel Enhancement Mode Field Effect Transistor

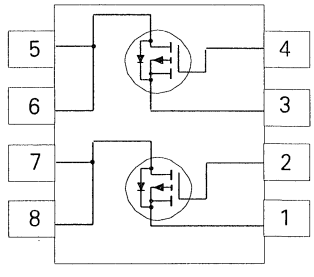
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.2A, -20V. $R_{DS(ON)}$ = 0.11Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.15Ω @ V_{GS} = -3.0V
  $R_{DS(ON)}$ = 0.19Ω @ V_{GS} = -2.7V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9933	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-12	V
I_D	Drain Current - Continuous	(Note 1a)	-3.2	A
	- Pulsed		-10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -10 V, V_{GS} = 0 V, T_J = 70°C			-5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -12 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.8	-1		V
		T_J = 125°C	-0.5	-0.8		
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -3.2 A		0.07	0.11	Ω
		T_J = 125°C		0.1	0.22	
		V_{GS} = -3.0 V, I_D = -2 A		0.105	0.15	
		V_{GS} = -2.7 V, I_D = -1 A		0.12	0.19	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-10			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-2			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -3.2 A		7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		870		pF
C_{oss}	Output Capacitance			630		pF
C_{rss}	Reverse Transfer Capacitance			240		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -6 V, I_D = -1 A, V_{GEN} = -6 V, R_{GEN} = 6 Ω		13	40	ns
t_r	Turn - On Rise Time			36	80	ns
$t_{D(off)}$	Turn - Off Delay Time			35	70	ns
t_f	Turn - Off Fall Time			24	40	ns
Q_g	Total Gate Charge	V_{DS} = -6 V, I_D = -3.2 A, V_{GS} = -4.5 V		12	20	nC
Q_{gs}	Gate-Source Charge			2.6		nC
Q_{gd}	Gate-Drain Charge			5		nC

4

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)		-0.8	-1.2	V
t_{rr}	Source-Drain Reverse Recovery Time	I_F = -1.3 A, di/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

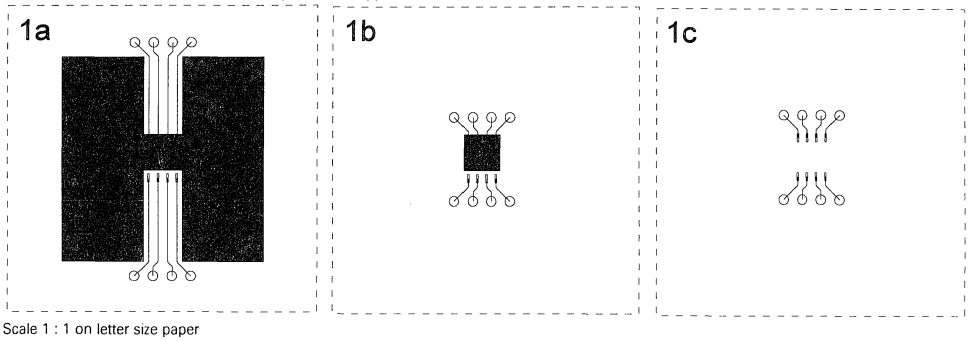
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%..

Typical Electrical Characteristics

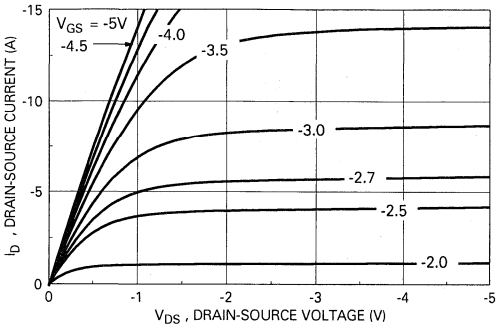


Figure 1. On-Region Characteristics.

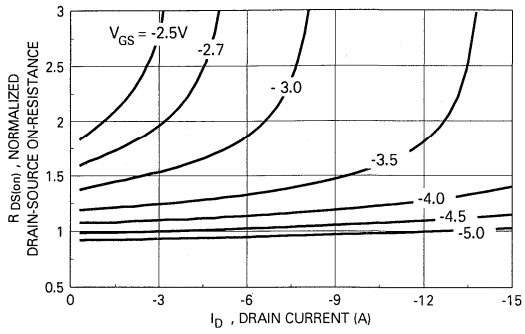


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

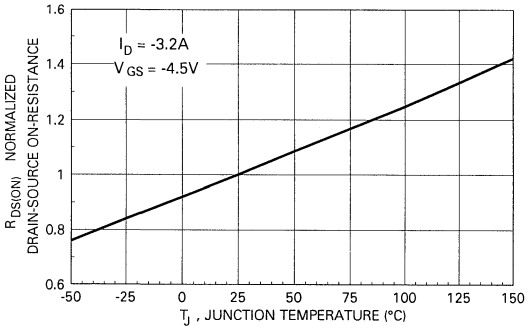


Figure 3. On-Resistance Variation with Temperature.

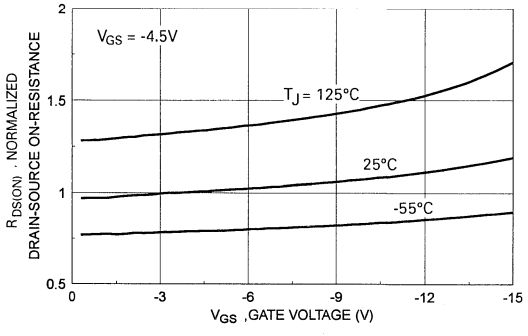


Figure 4. On-Resistance Variation with Drain Current and Temperature.

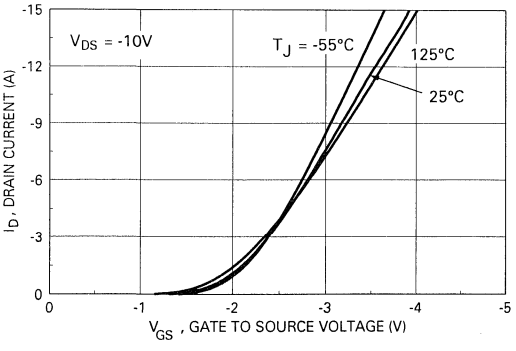


Figure 5. Transfer Characteristics.

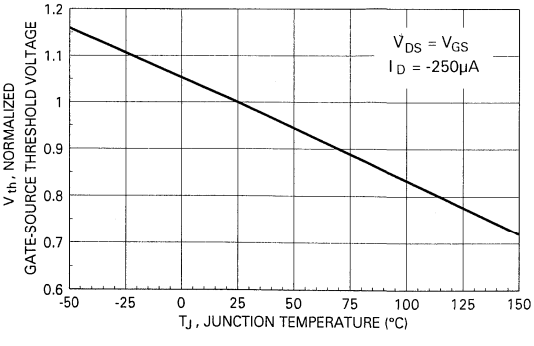


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

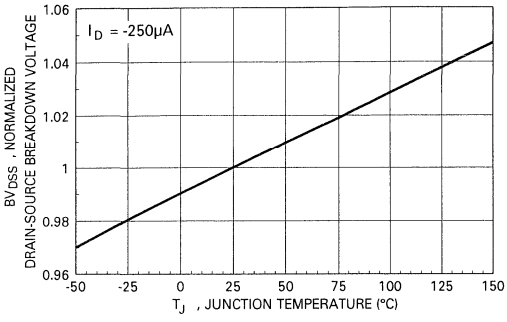


Figure 7. Breakdown Voltage Variation with Temperature.

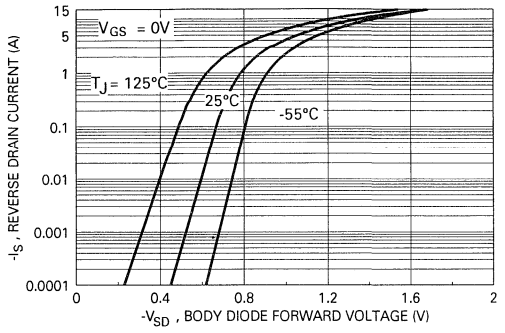


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

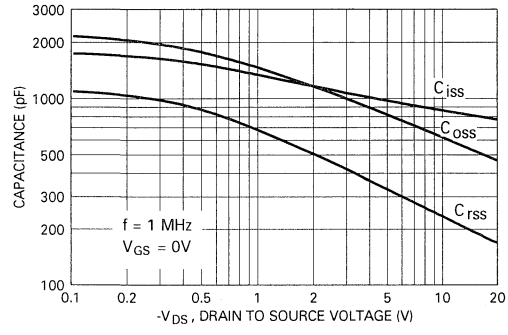


Figure 9. Capacitance Characteristics.

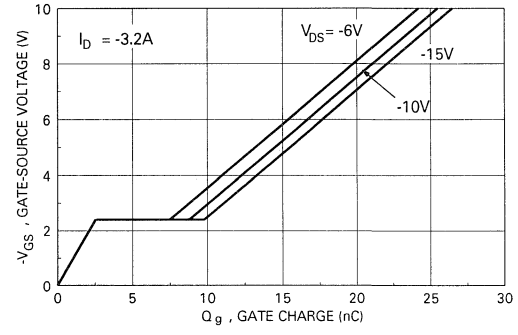


Figure 10. Gate Charge Characteristics.

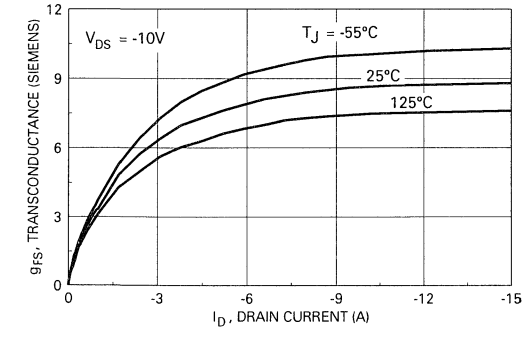


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

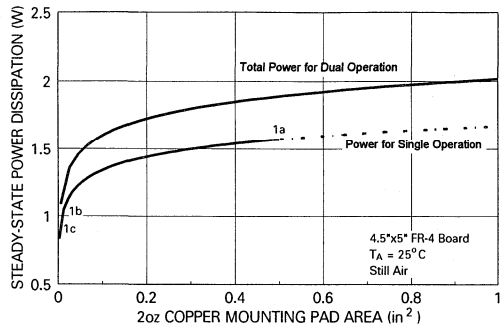


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

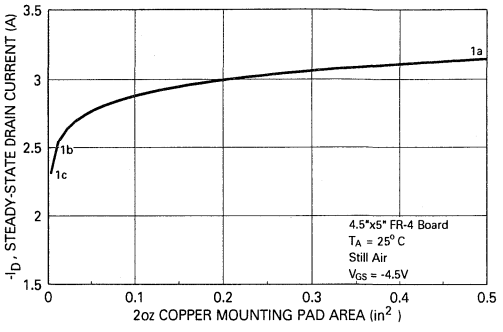


Figure 13. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

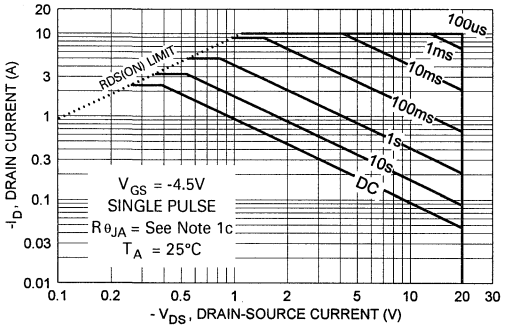


Figure 14. Maximum Safe Operating Area.

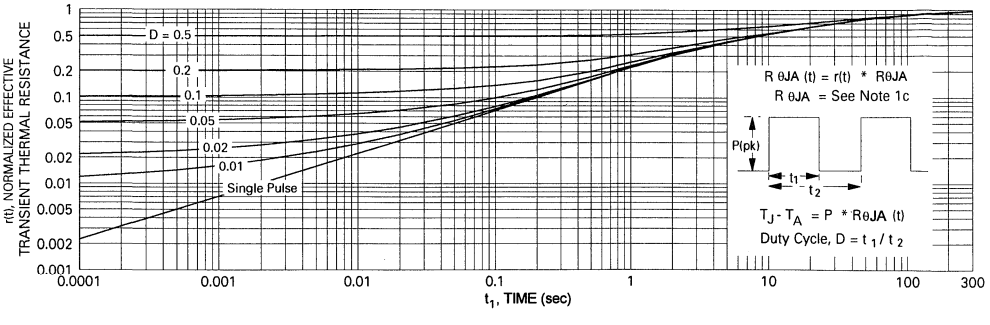


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

ADVANCE INFORMATION

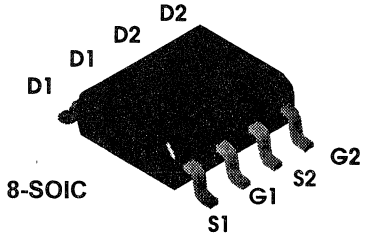
NDS9933A
Dual P-Channel Enhancement Mode Field Effect Transistor

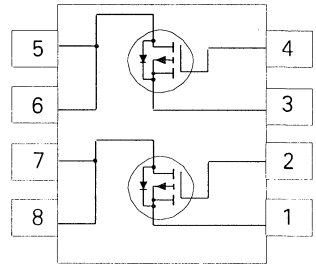
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -2.7A, -20V. $R_{DS(ON)}$ = 0.14Ω @ V_{GS} = -4.5V
  $R_{DS(ON)}$ = 0.19Ω @ V_{GS} = -2.7V
  $R_{DS(ON)}$ = 0.20Ω @ V_{GS} = -2.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9933A	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		-8	V
I_D	Drain Current - Continuous	(Note 1a)	-2.7	A
	- Pulsed		-10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -10 V, V_{GS} = 0 V, T_J = 70°C			-5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4			V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -2.7 A			0.14	Ω
		T_J = 125°C			0.26	
		V_{GS} = -3.0 V, I_D = -2 A			0.19	
		V_{GS} = -2.7 V, I_D = -1 A			0.2	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-10			A
		V_{GS} = -2.7 V, V_{DS} = -5 V	-2			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2.7A		6		S
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.3 A (Note 2)			-1.2	V
t_{rr}	Source-Drain Reverse Recovery Time	I_F = -1.3 A, di/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

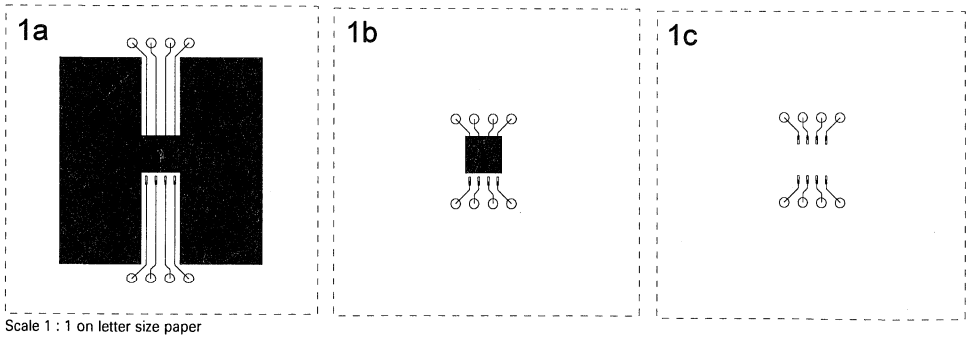
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%..

National Semiconductor™

May 1996

NDS9936

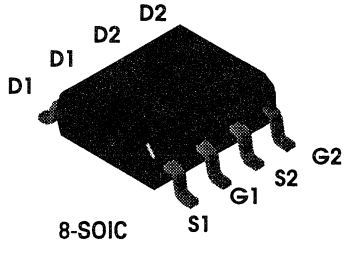
Dual N-Channel Enhancement Mode Field Effect Transistor

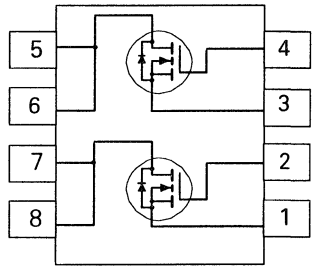
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5A, 30V. $R_{DS(ON)}$ = 0.05Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9936	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	(Note 1a)	± 5.0	A
	- Continuous @ T_A = 70°C	(Note 1a)	± 4.0	
	- Pulsed @ T_A = 25°C		± 40	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		T_J= 55°C			20	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.4	3	V
		T_J=125°C	0.7	1.1	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5 A		0.044	0.05	Ω
		T_J=125°C		0.066	0.1	
		V_{GS} = 4.5 V, I_D = 3.9 A		0.066	0.08	
		T_J=125°C		0.099	0.16	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	40			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	20			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A	3	8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		525		pF
C_{oss}	Output Capacitance			315		pF
C_{rss}	Reverse Transfer Capacitance			185		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(ON)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		12	30	ns
t_r	Turn - On Rise Time			10	25	ns
$t_{D(OFF)}$	Turn - Off Delay Time			25	50	ns
t_f	Turn - Off Fall Time			10	50	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 5 A, V_{GS} = 10 V		17	35	nC
Q_{gs}	Gate-Source Charge			1.5		nC
Q_{gd}	Gate-Drain Charge			3.7		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.7 A (Note 2)		0.78	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 5 A, dI_F/dt = 100 A/µs		70	160	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

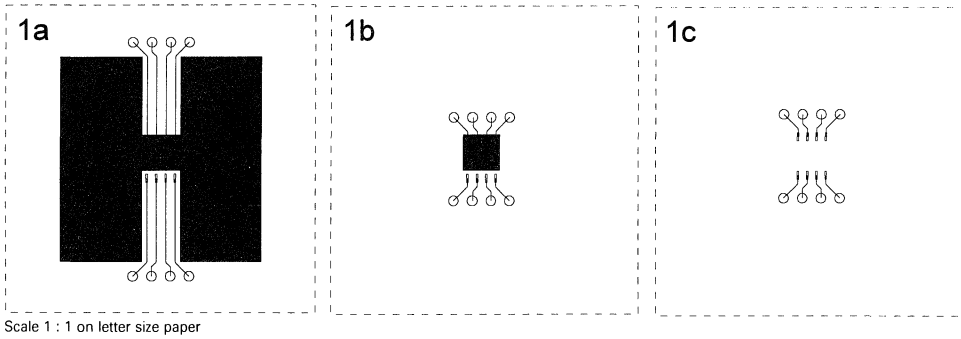
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

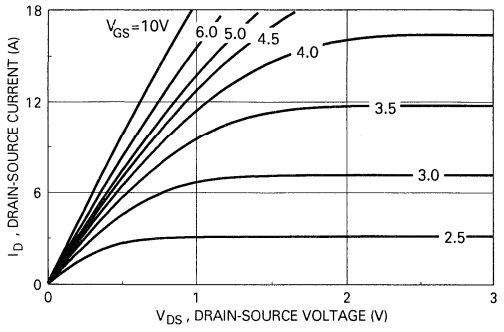


Figure 1. On-Region Characteristics.

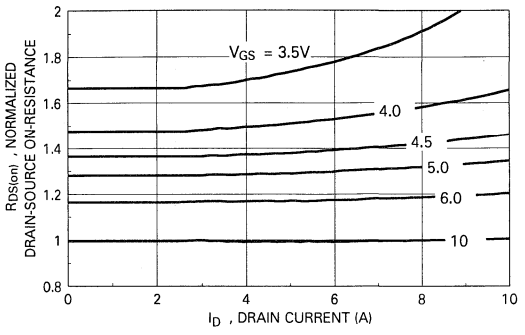


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

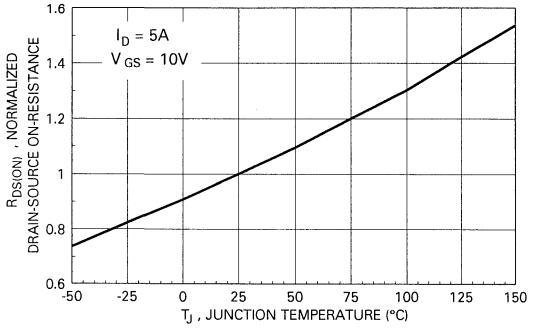


Figure 3. On-Resistance Variation with Temperature.

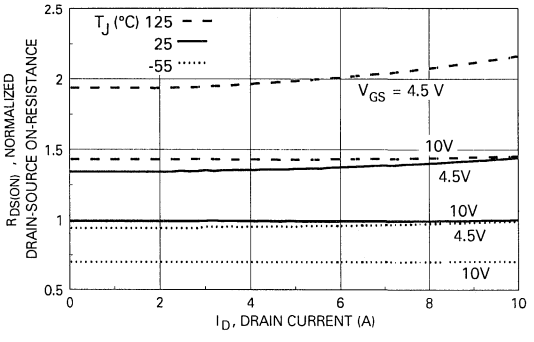


Figure 4. On-Resistance Variation with Drain Current and Temperature.

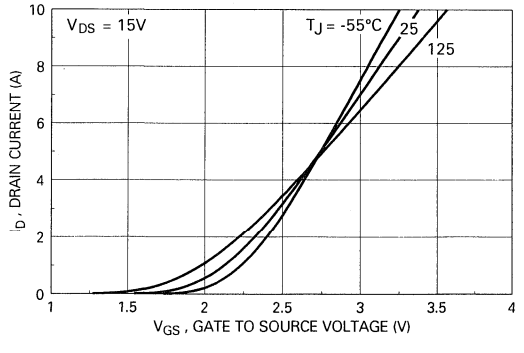


Figure 5. Transfer Characteristics.

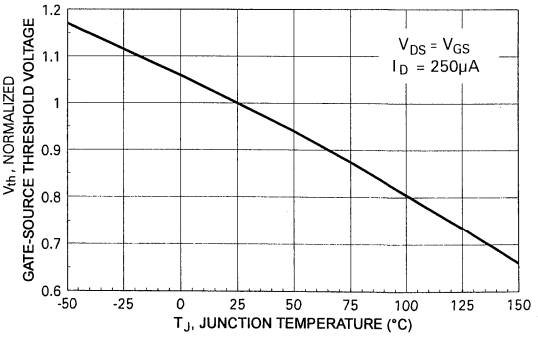


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

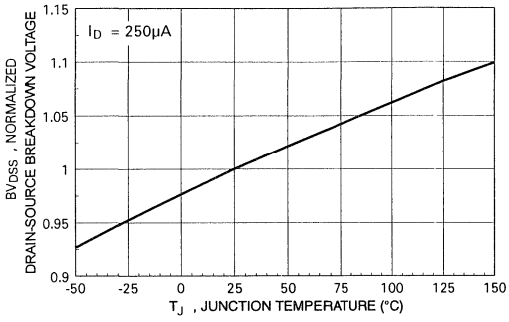


Figure 7. Breakdown Voltage Variation with Temperature.

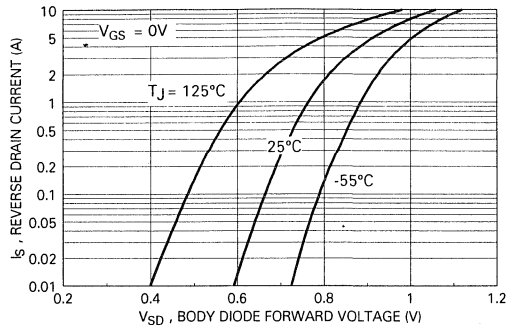


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

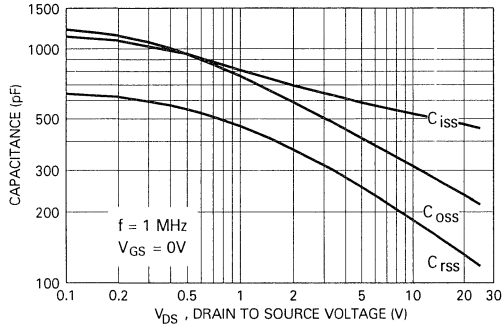


Figure 9. Capacitance Characteristics.

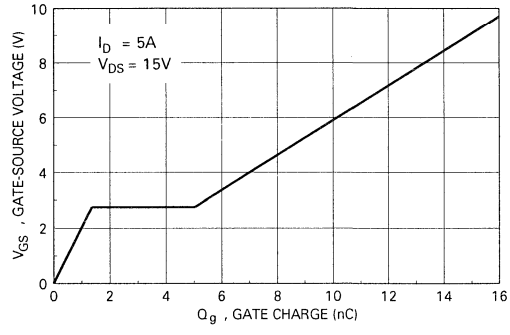


Figure 10. Gate Charge Characteristics.

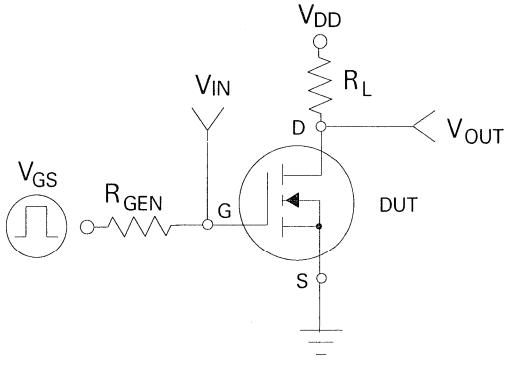


Figure 11. Switching Test Circuit

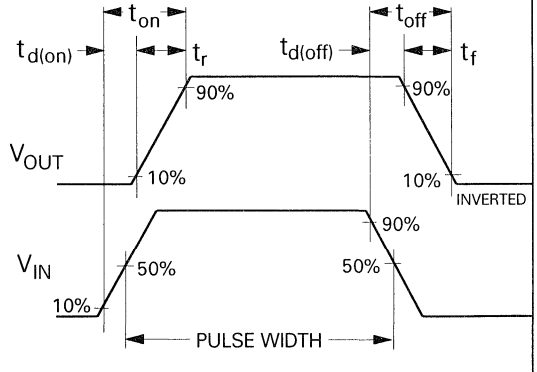


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

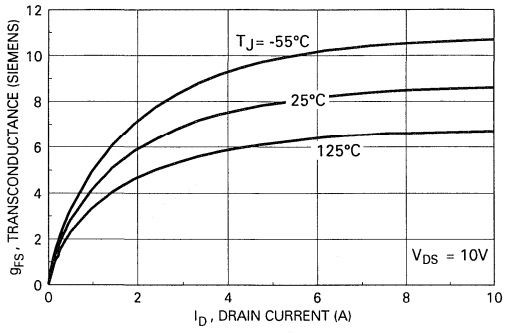


Figure 13. Transconductance Variation with Drain Current and Temperature.

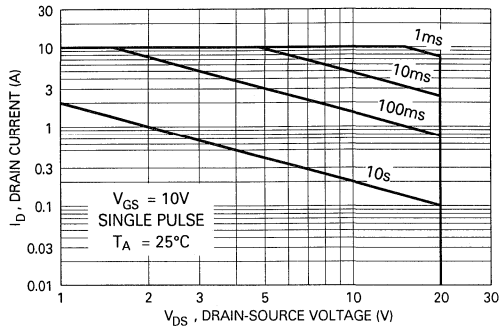


Figure 14. Maximum Safe Operating Area.

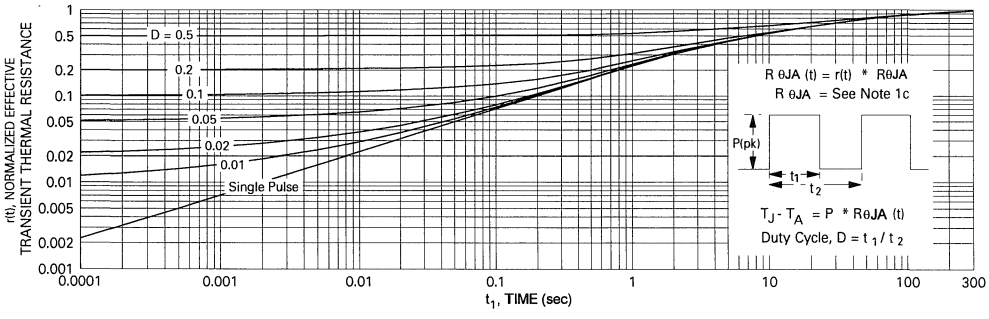


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

4

National Semiconductor™

May 1996

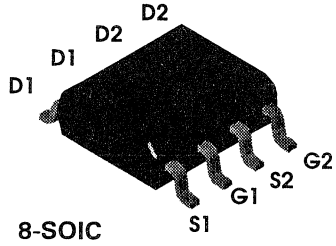
NDS9942
Dual N & P-Channel Enhancement Mode Field Effect Transistor

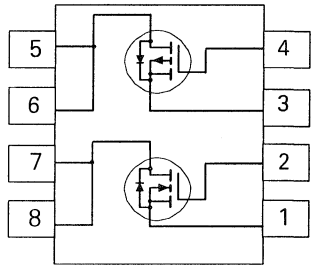
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.0A, 20V, $R_{DS(ON)}$=0.125Ω @ V_{GS}=10V
  P-Channel -2.5A, -20V, $R_{DS(ON)}$=0.2Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		20	-20	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 3.0	± 2.5	A
	- Continuous T_A = 70°C	(Note 1a)	± 2.5	± 2.0	
	- Pulsed T_A = 25°C		± 10	± 10	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		T_J = 55°C				25	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_J = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		T_J = 125°C		0.7	1.1	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2	-3	
		T_J = 125°C		-0.85	-1.7	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.0 A	N-Ch		0.062	0.125	Ω
		T_J = 125°C			0.085	0.175	
		V_{GS} = 4.5 V, I_D = 0.5 A			0.08	0.25	
		T_J = 125°C			0.11	0.35	
		V_{GS} = -10 V, I_D = -1.0 A	P-Ch		0.18	0.2	
		T_J = 125°C			0.24	0.35	
		V_{GS} = -4.5 V, I_D = -0.5 A			0.26	0.4	
		T_J = 125°C			0.35	0.56	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = 4.5 V, V_{DS} = 5 V		2			
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			
		V_{GS} = -4.5 V, V_{DS} = 5 V		-2			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		525		
C_{oss}	Output Capacitance		N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		300		
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		130		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		6	15	ns
			P-Ch		8	40	
t_r	Turn - On Rise Time		N-Ch		12	20	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		15	40	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		22	50	ns
			P-Ch		25	90	
t_f	Turn - Off Fall Time		N-Ch		8	50	ns
			P-Ch		8	50	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 2.3 A, V_{GS} = 10 V	N-Ch		17	27	nC
			P-Ch		15	25	
Q_{gs}	Gate-Source Charge		N-Ch		1.2		nC
		P-Channel V_{DS} = -10 V, I_D = -2.3 A, V_{GS} = -10 V	P-Ch		1.2		
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		4.8		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.6	A
			P-Ch			-1.6	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.78	1.2	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch		-0.94	-1.6	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs	N-Ch		28	100	ns
			P-Ch		29	100	
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0 V, I_F = -1.25 A, dI_F/dt = 100 A/µs	N-Ch		2.1		A
			P-Ch		1.9		

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

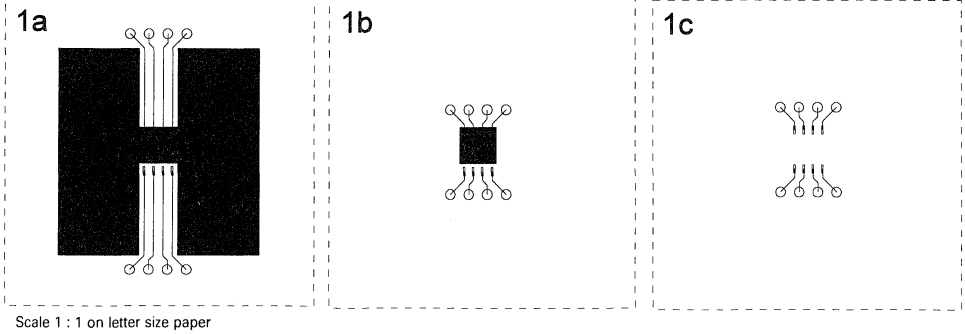
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

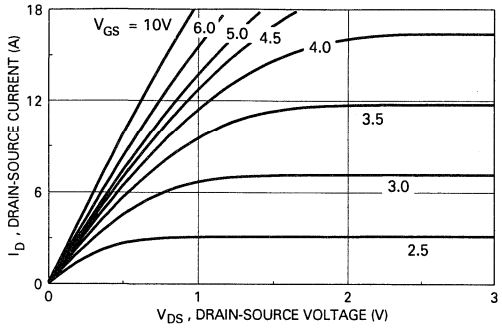


Figure 1. N-Channel On-Region Characteristic.

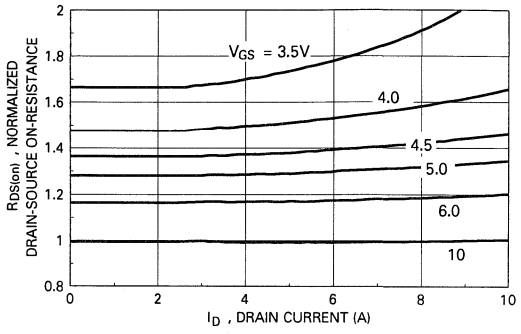


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

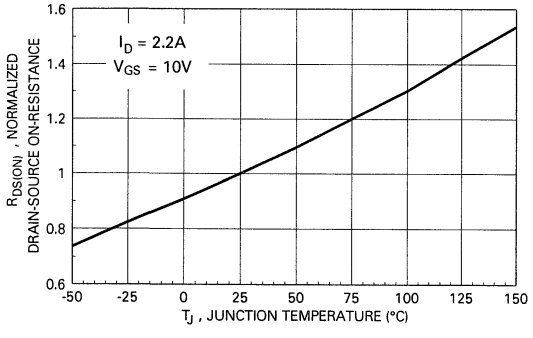


Figure 3. N-Channel On-Resistance Variation with Temperature.

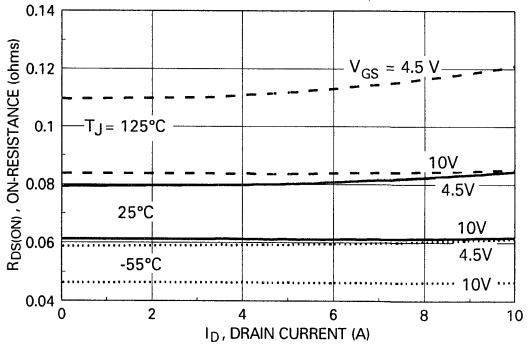


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

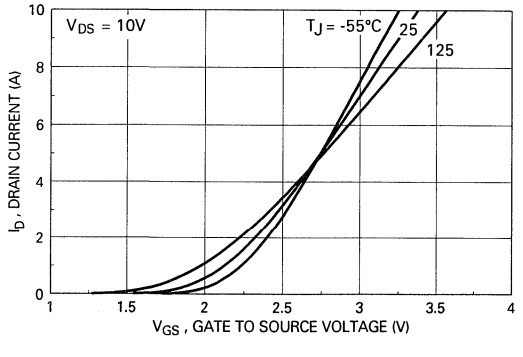


Figure 5. N-Channel Transfer Characteristic.

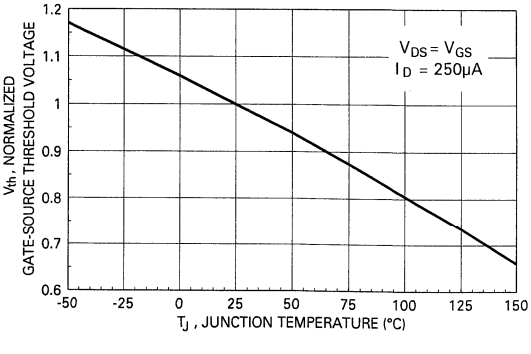


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

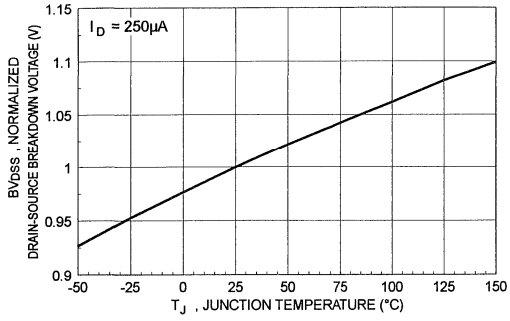


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

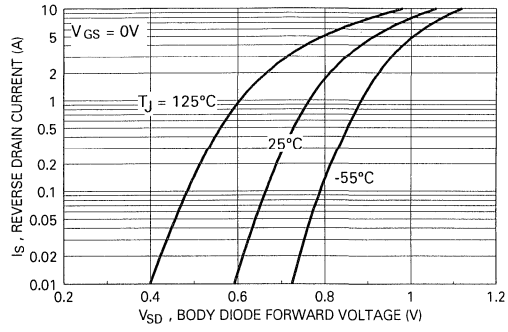


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

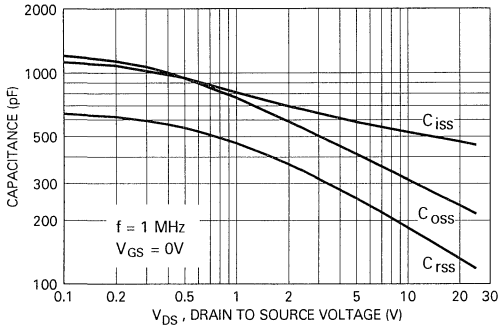


Figure 9. N-Channel Capacitance Characteristics.

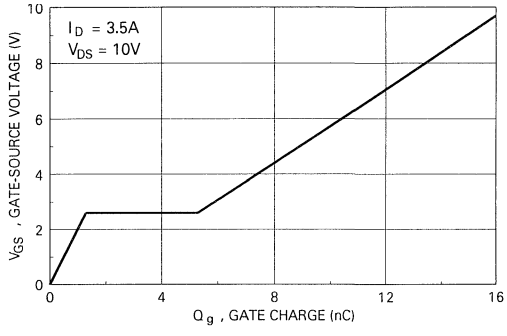


Figure 10. N-Channel Gate Charge Characteristic.

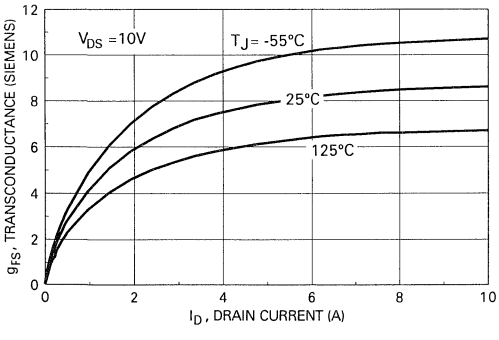


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

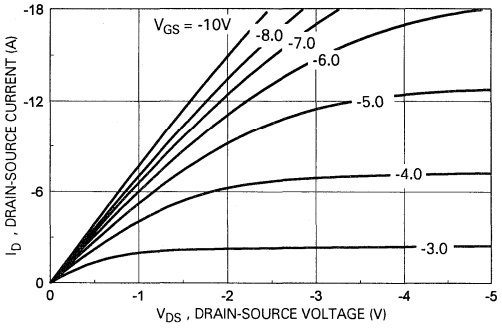


Figure 12. P-Channel On-Region Characteristics.

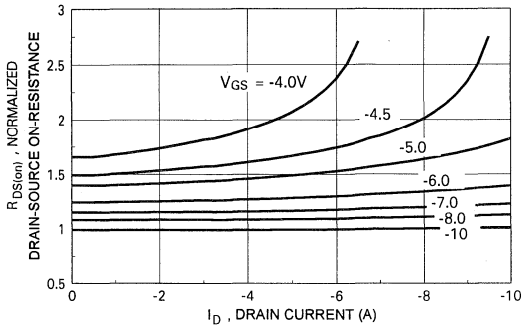


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

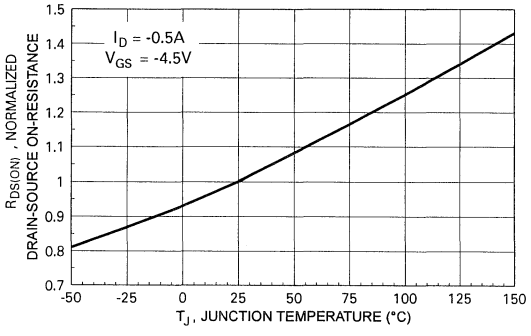


Figure 14. P-Channel On-Resistance Variation with Temperature.

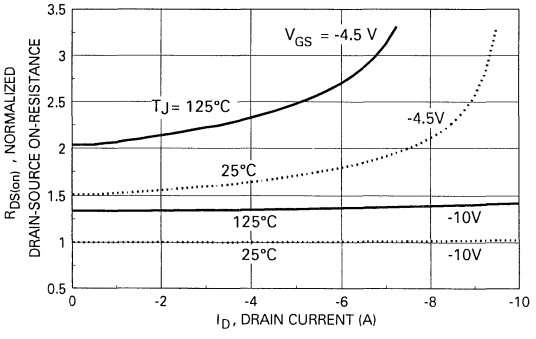


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

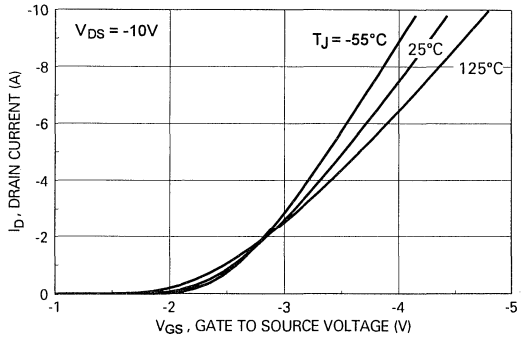


Figure 16. P-Channel Transfer Characteristics.

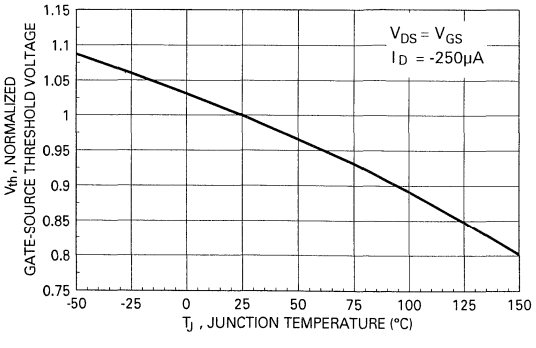


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

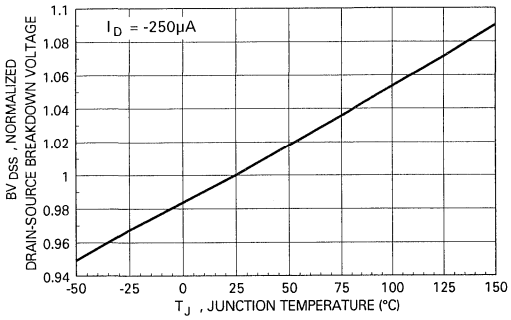


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

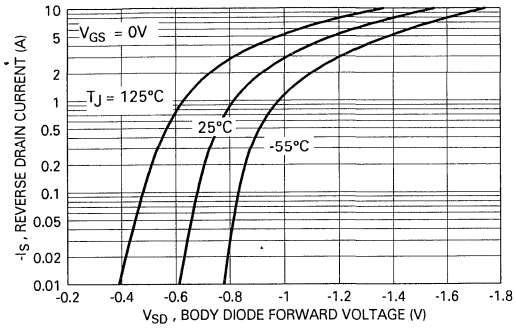


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

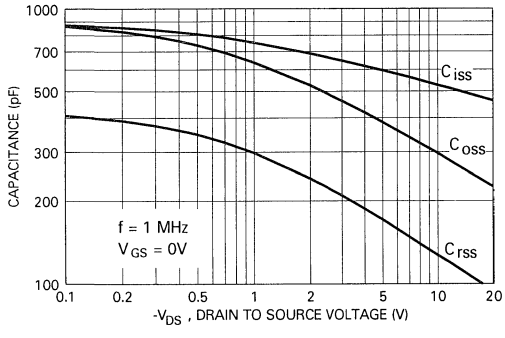


Figure 20. P-Channel Capacitance Characteristics.

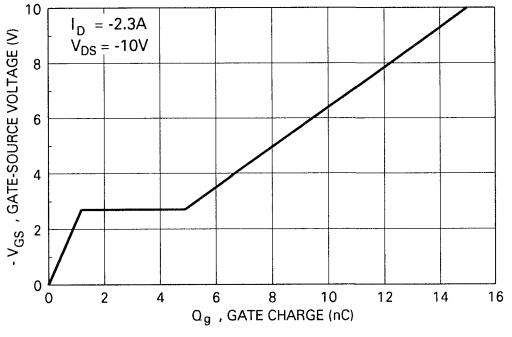


Figure 21. P-Channel Gate Charge Characteristic.

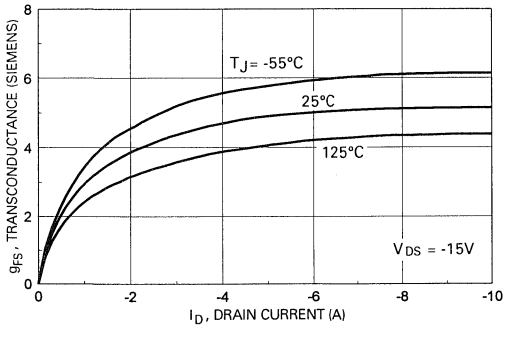


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

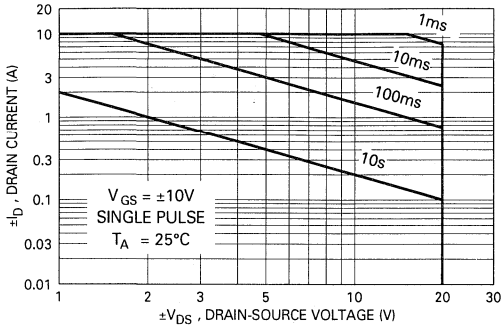


Figure 23. Maximum Safe Operating Area for both N & P-Channel.

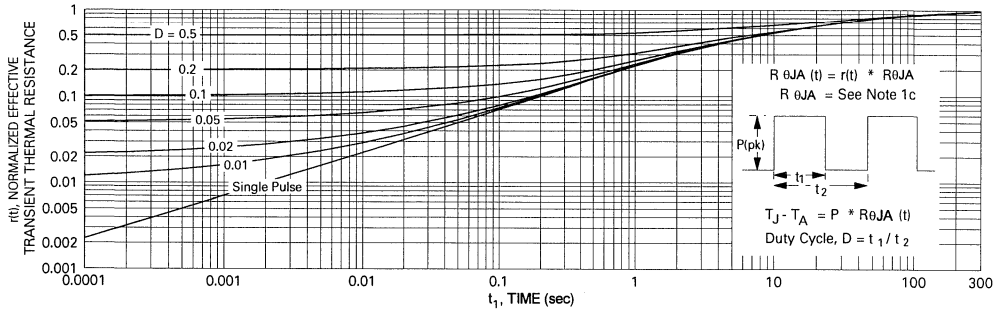


Figure 24. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

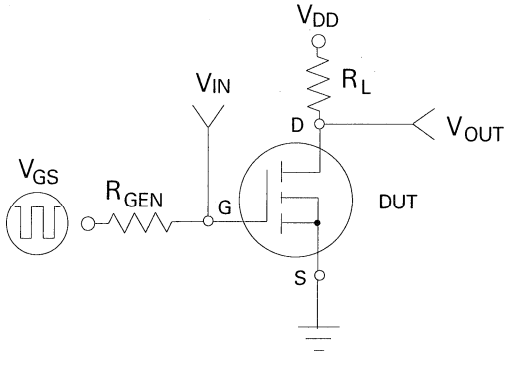


Figure 25. N or P-Channel Switching Test Circuit.

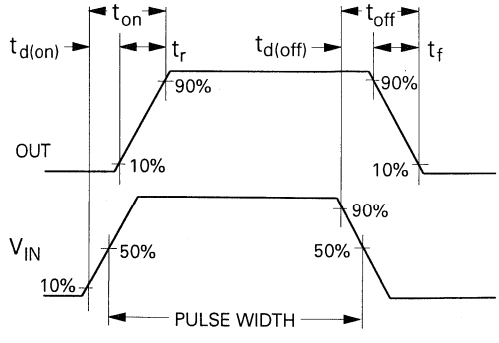


Figure 26. N or P-Channel Switching Waveforms.

National Semiconductor™

May 1996

NDS9943

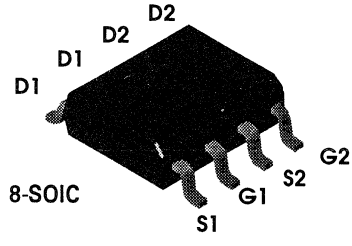
Dual N & P-Channel Enhancement Mode Field Effect Transistor

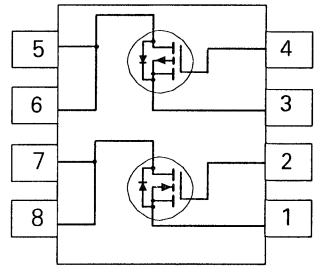
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.0A, 20V, $R_{DS(ON)}$=0.125Ω @ V_{GS}=10V
  P-Channel -2.8A, -25V, $R_{DS(ON)}$=0.16Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		20	-20	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 3.0	± 2.8	A
	- Continuous T_A = 70°C	(Note 1a)	± 2.5	± 2.3	
	- Pulsed T_A = 25°C		± 10	± 10	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			2	µA
		T_J = 55°C				25	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_J = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		T_J = 125°C		0.7	1.1	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2	-3	
		T_J = 125°C		-0.85	-1.7	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.0 A	N-Ch		0.062	0.125	Ω
		T_J = 125°C			0.085	0.175	
		V_{GS} = 6 V, I_D = 2.0 A			0.073	0.16	
		V_{GS} = 4.5 V, I_D = 1.5 A			0.08	0.25	
		T_J = 125°C			0.11	0.35	
		V_{GS} = -10 V, I_D = -3.0 A	P-Ch			0.16	
		T_J = 125°C				0.35	
		V_{GS} = -6 V, I_D = -2.0 A				0.2	
		V_{GS} = -4.5 V, I_D = -1.5 A				0.3	
		T_J = 125°C				0.56	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	10			A
		V_{GS} = 4.5 V, V_{DS} = 5 V		2			
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			
		V_{GS} = -4.5 V, V_{DS} = 5 V		-2			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.0 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3.0 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		525		
C_{oss}	Output Capacitance	P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		315		pF
			P-Ch		300		
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		130		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 20 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		6	15	ns
			P-Ch		8	40	
t_r	Turn - On Rise Time		N-Ch		12	20	ns
		P-Channel V_{DD} = -20 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		15	40	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		22	50	ns
			P-Ch		25	90	
t_f	Turn - Off Fall Time		N-Ch		8	50	ns
			P-Ch		8	50	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 2.3 A, V_{GS} = 10 V	N-Ch		17	27	nC
			P-Ch		15	25	
Q_{gs}	Gate-Source Charge		N-Ch		1.2		nC
		P-Channel V_{DS} = -10 V, I_D = -2.3 A, V_{GS} = -10 V	P-Ch		1.2		
Q_{gd}	Gate-Drain Charge		N-Ch		5		nC
			P-Ch		4.8		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.6	A
			P-Ch			-1.6	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.78	1.2	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch		-0.94	-1.6	
t_{rr}	Reverse Recovery Time	N-Channel V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs	N-Ch		28	100	ns
			P-Ch		29	100	
I_{rr}	Reverse Recovery Current	P-Channel V_{GS} = 0 V, I_F = -1.25 A, dI_F/dt = 100 A/µs	N-Ch		2.1		A
			P-Ch		1.9		

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

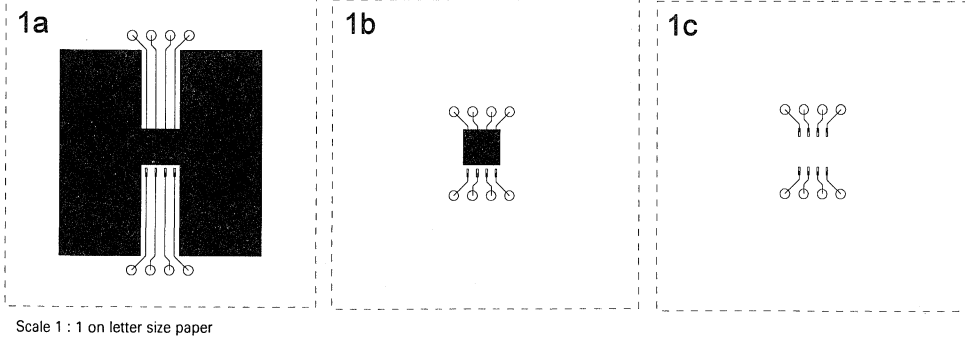
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

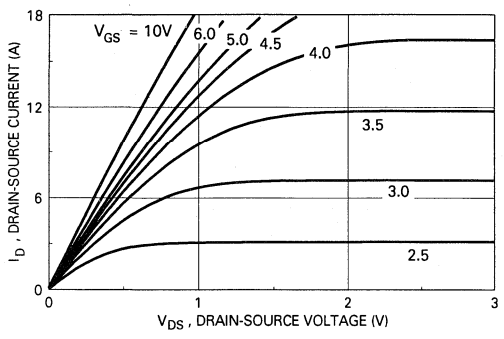


Figure 1. N-Channel On-Region Characteristic.

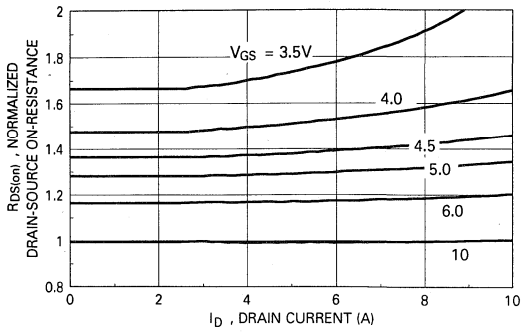


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

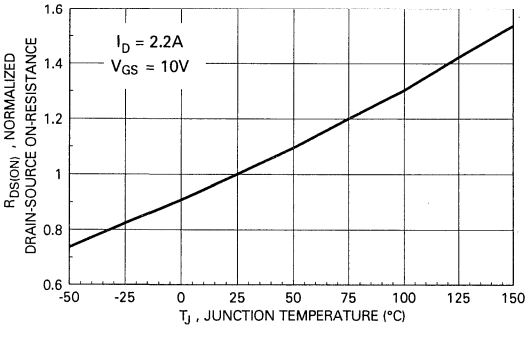


Figure 3. N-Channel On-Resistance Variation with Temperature.

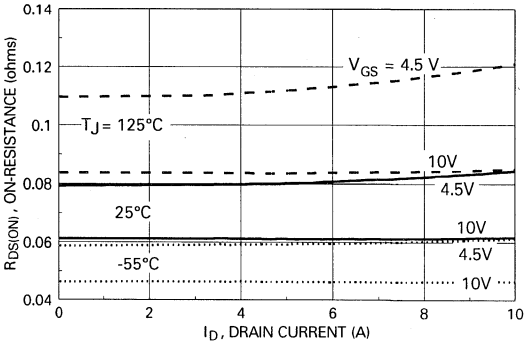


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

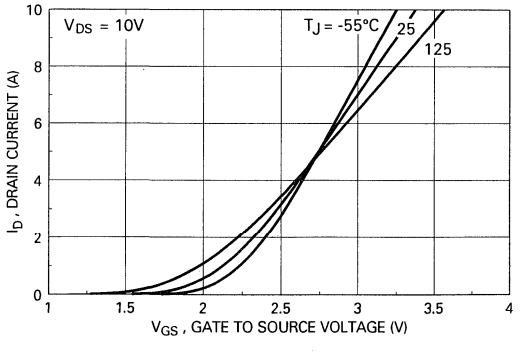


Figure 5. N-Channel Transfer Characteristic.

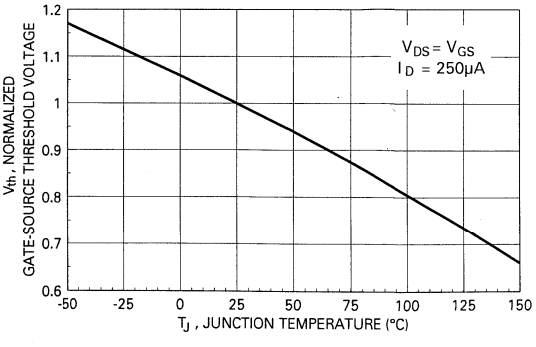


Figure 6. N-Channel Gate Threshold Variation with Temperature.

4

Typical Electrical Characteristics: N-Channel (continued)

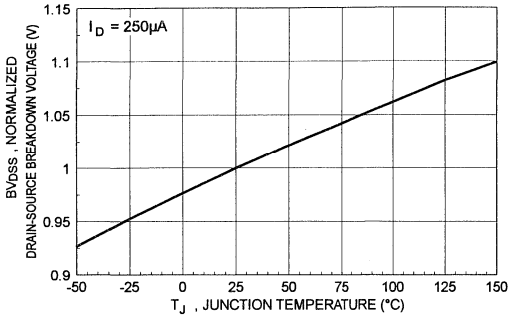


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

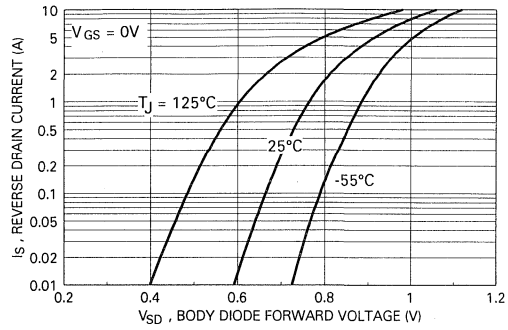


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

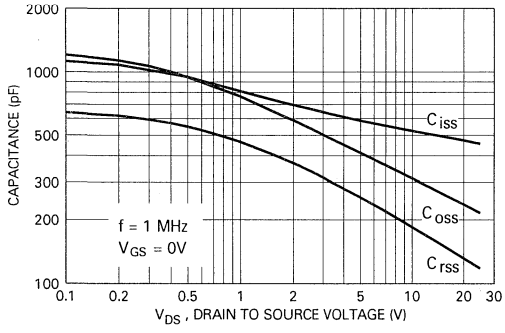


Figure 9. N-Channel Capacitance Characteristics.

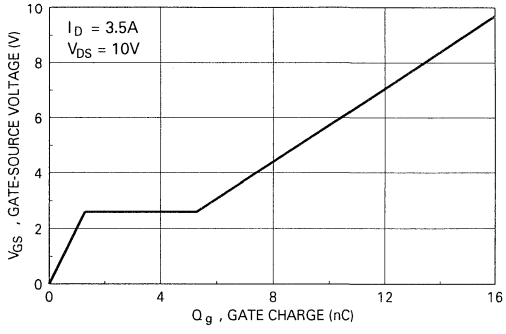


Figure 10. N-Channel Gate Charge Characteristic.

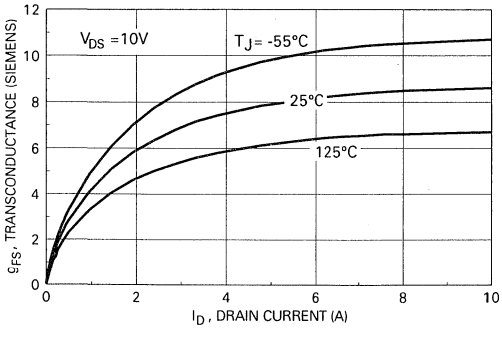


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

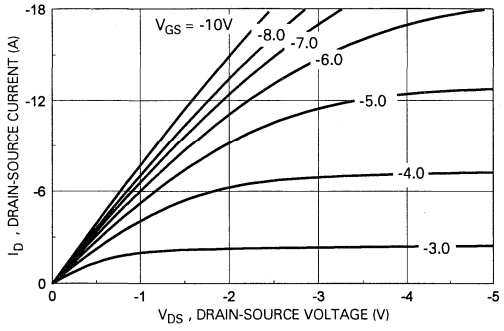


Figure 12. P-Channel On-Region Characteristics.

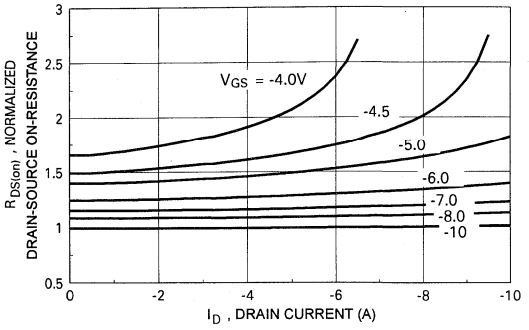


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

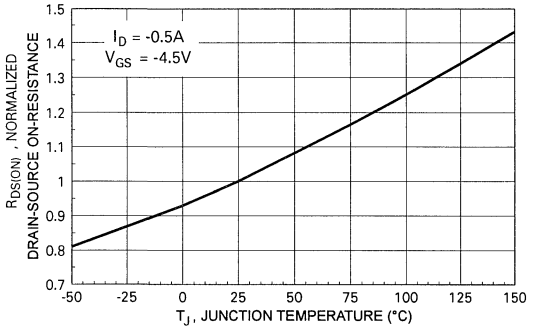


Figure 14. P-Channel On-Resistance Variation with Temperature.

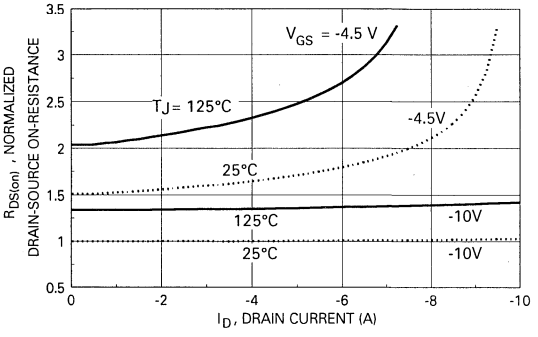


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

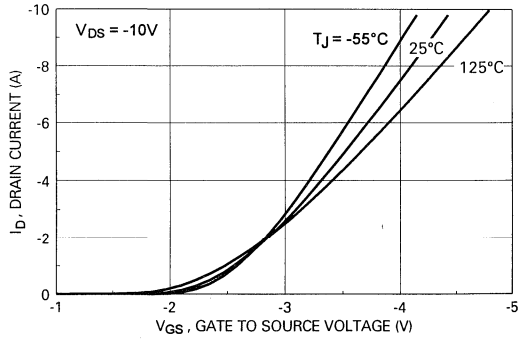


Figure 16. P-Channel Transfer Characteristics.

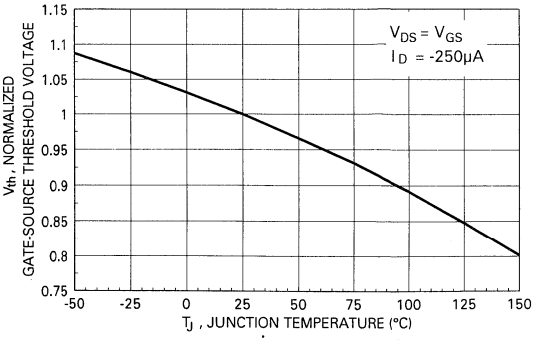


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

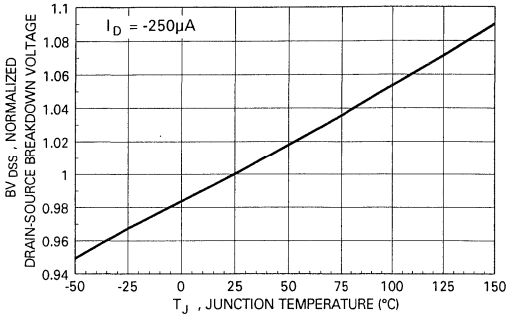


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

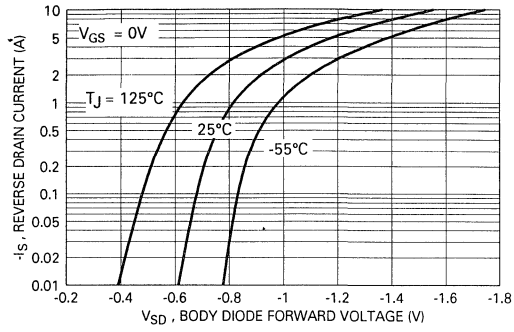


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

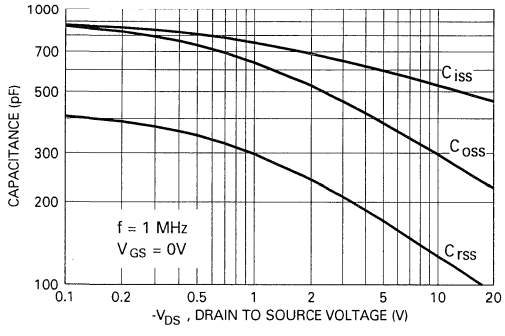


Figure 20. P-Channel Capacitance Characteristics.

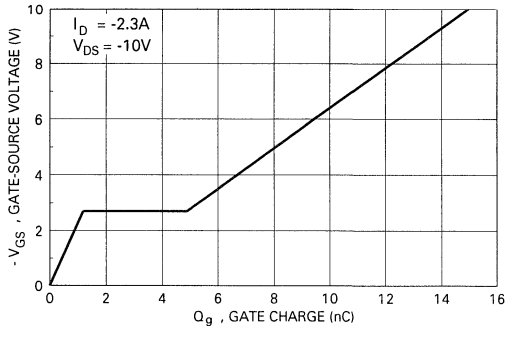


Figure 21. P-Channel Gate Charge Characteristic.

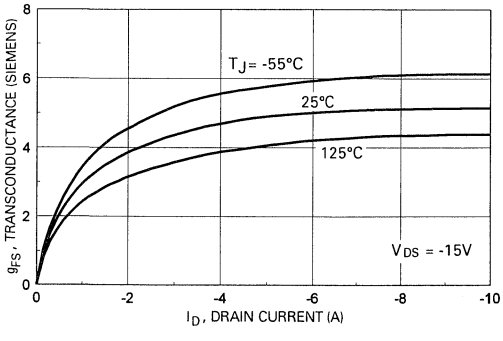


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

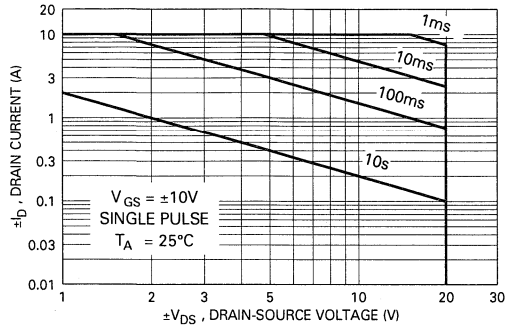


Figure 23. Maximum Safe Operating Area for both N & P-Channel.

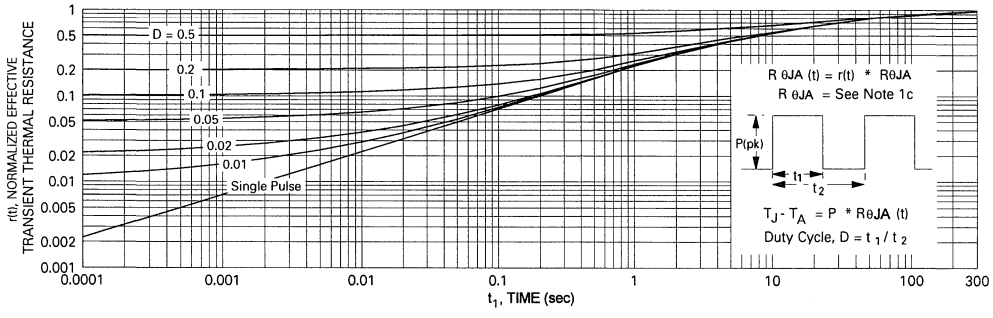


Figure 24. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

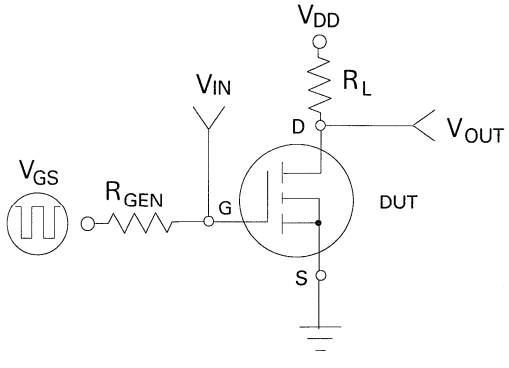


Figure 25. N or P-Channel Switching Test Circuit.

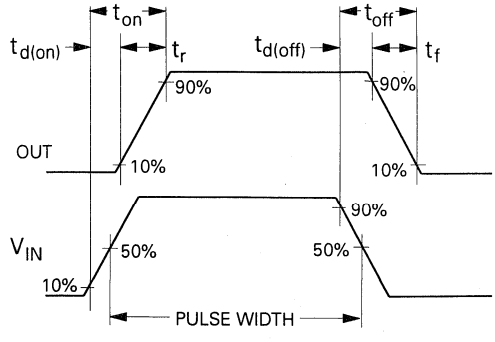


Figure 26. N or P-Channel Switching Waveforms.

National Semiconductor™

May 1996

NDS9945

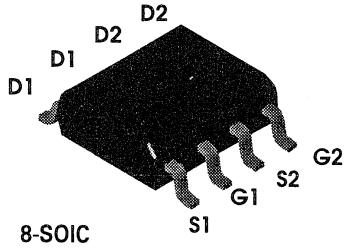
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.5A, 60V. $R_{DS(ON)}$ = 0.10Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



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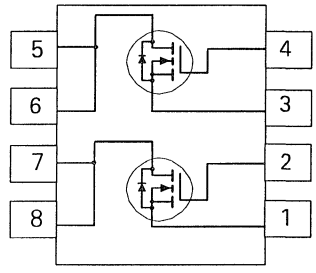


Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9945	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	(Note 1a)	± 3.5	A
	- Continuous @ T_A = 70°C	(Note 1a)	± 2.8	
	- Pulsed @ T_A = 25°C		± 10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		T_J = 125°C	0.7		2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A		0.084	0.1	Ω
		T_J = 125°C		0.13	0.2	
		V_{GS} = 4.5 V, I_D = 2.5 A		0.11	0.2	
		T_J = 125°C		0.17	0.3	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	10			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	3.5			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.5 A		6.3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		435		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	25	ns
t_r	Turn - On Rise Time			4	30	ns
$t_{D(off)}$	Turn - Off Delay Time			24	50	ns
t_f	Turn - Off Fall Time			7	40	ns
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D = 3.5 A, V_{GS} = 10 V		13	30	nC
Q_{gs}	Gate-Source Charge			1.2		nC
Q_{gd}	Gate-Drain Charge			4.7		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.7 A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 1.7 A, dI_F/dt = 100 A/µs		52		ns
I_{rr}	Reverse Recovery Current			2.3		A

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

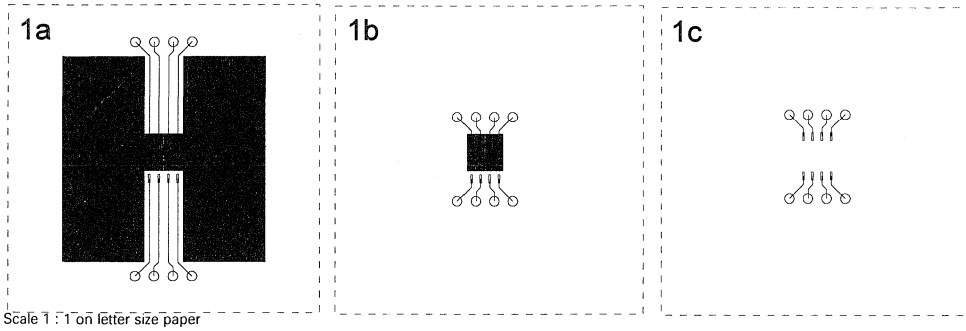
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

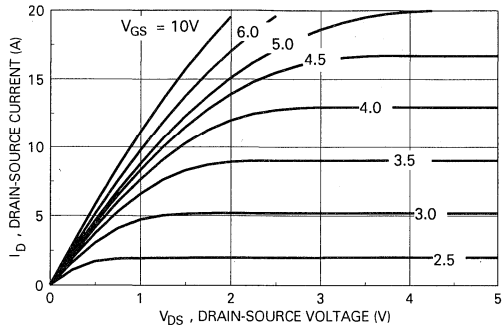


Figure 1. On-Region Characteristics.

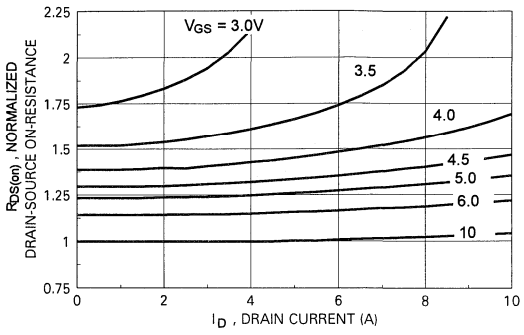


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

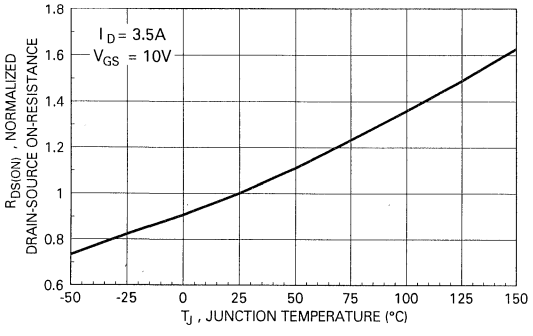


Figure 3. On-Resistance Variation with Temperature.

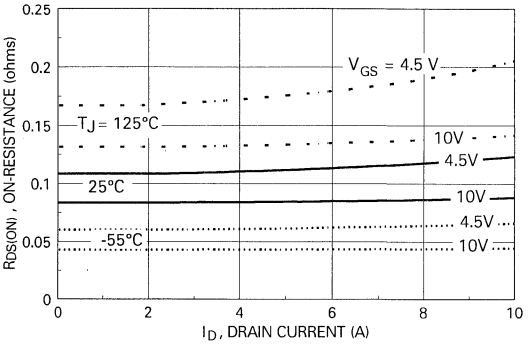


Figure 4. On-Resistance Variation with Drain Current and Temperature.

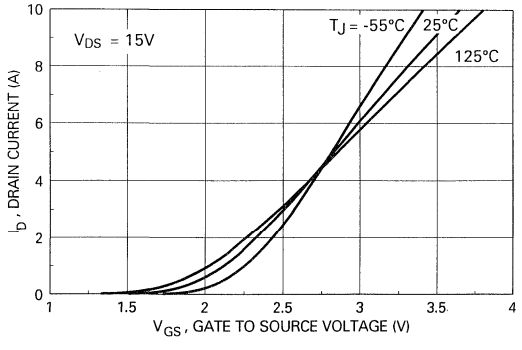


Figure 5. Transfer Characteristics.

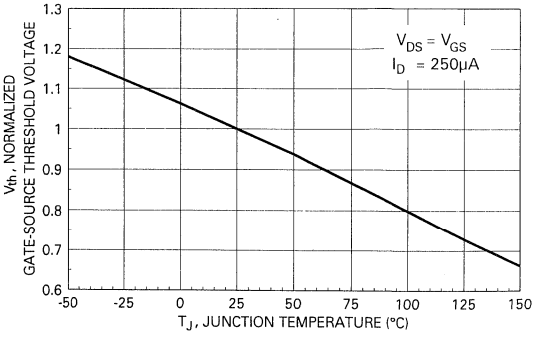


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

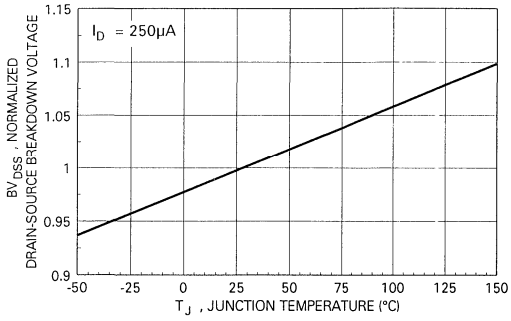


Figure 7. Breakdown Voltage Variation with Temperature.

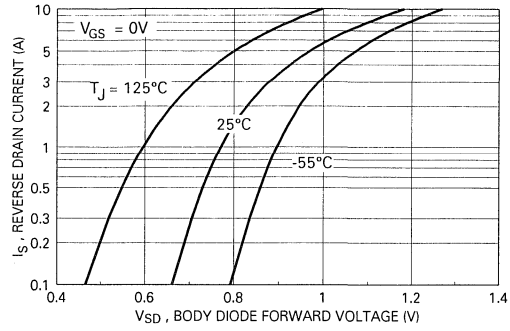


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

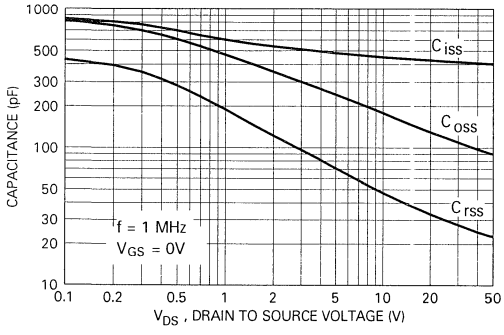


Figure 9. Capacitance Characteristics.

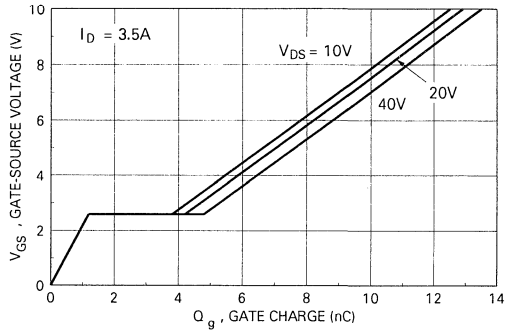


Figure 10. Gate Charge Characteristics.

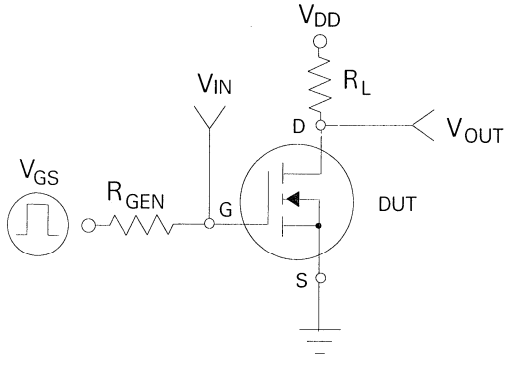


Figure 11. Switching Test Circuit.

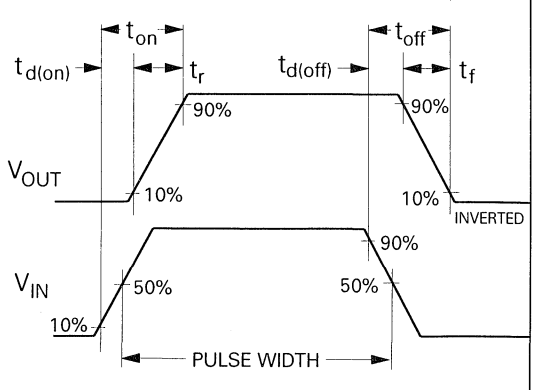


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

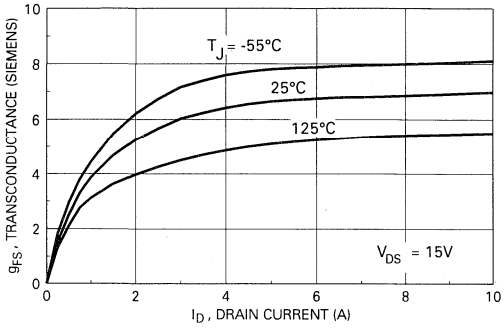


Figure 13. Transconductance Variation with Drain Current and Temperature.

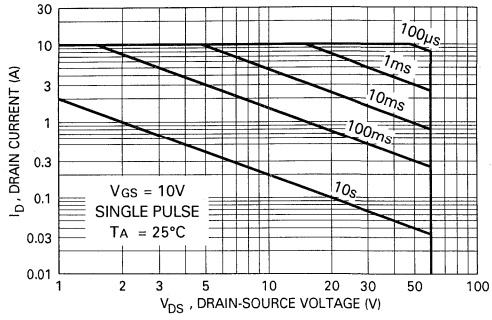


Figure 14. Maximum Safe Operating Area.

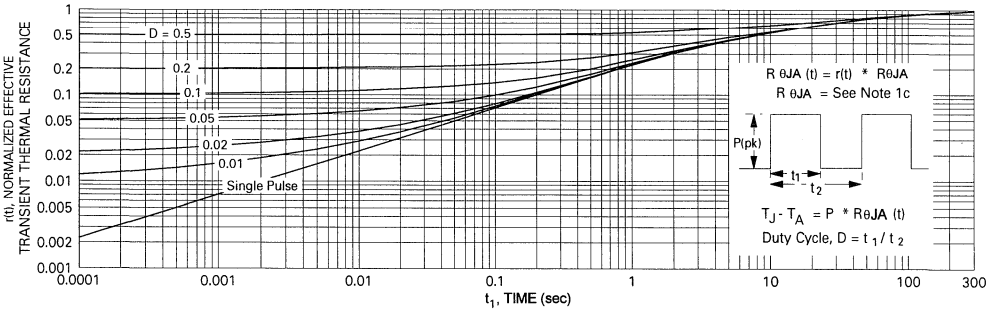


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

4

National Semiconductor™

May 1996

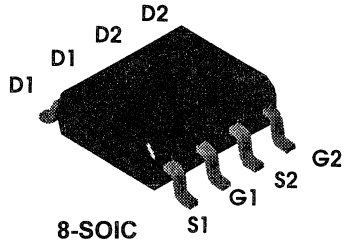
NDS9947
Dual P-Channel Enhancement Mode Field Effect Transistor

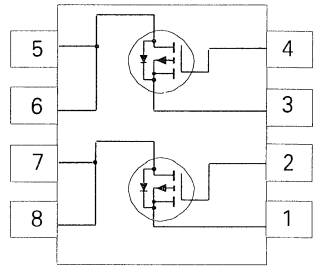
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -3.5A, -20V. $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = 10V
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9947	Units
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 3.5	A
	- Continuous T_A = 70°C	(Note 1a)	± 2.5	
	- Pulsed T_A = 25°C		± 10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2.2	-3	V
		T_J = 125°C	-0.8	-1.9	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -3.5 A		0.08	0.1	Ω
		T_J = 125°C		0.11	0.16	
		V_{GS} = -4.5 V, I_D = -1 A		0.165	0.19	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-14			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -3.5 A		5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		785		pF
C_{oss}	Output Capacitance			500		pF
C_{rss}	Reverse Transfer Capacitance			245		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		9	40	ns
t_r	Turn - On Rise Time			17	25	ns
$t_{D(off)}$	Turn - Off Delay Time			26	30	ns
t_f	Turn - Off Fall Time			13	20	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -3.5 A, V_{GS} = -10 V		19	30	nC
Q_{gs}	Gate-Source Charge				6	nC
Q_{gd}	Gate-Drain Charge				12	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.7 A (Note 2)		-0.9	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

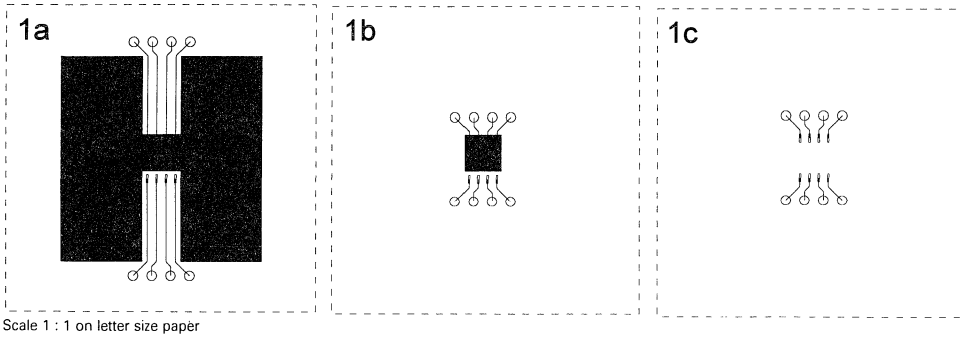
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%..

Typical Electrical Characteristics

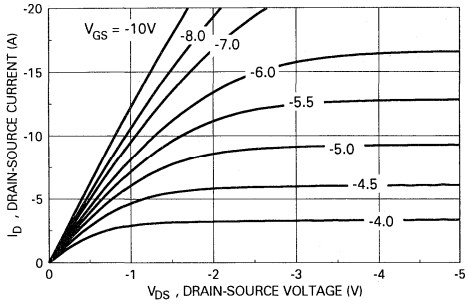


Figure 1. On-Region Characteristics

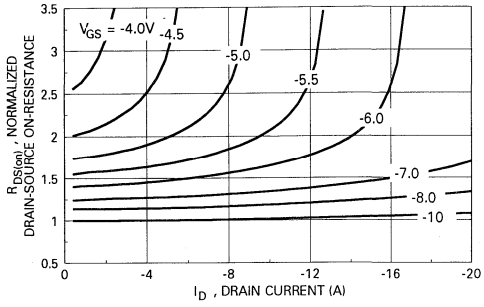


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

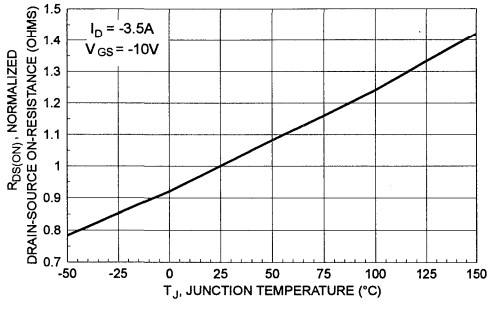


Figure 3. On-Resistance Variation with Temperature

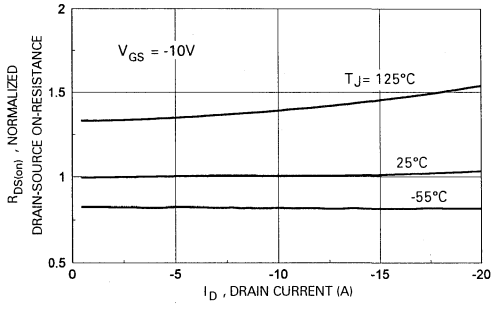


Figure 4. On-Resistance Variation with Drain Current and Temperature

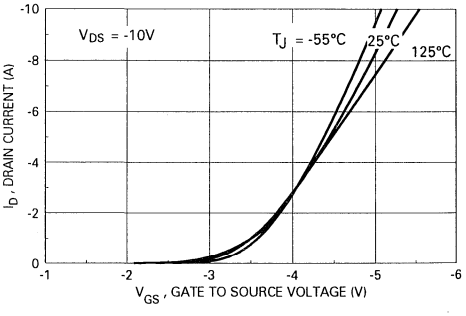


Figure 5. Transfer Characteristics

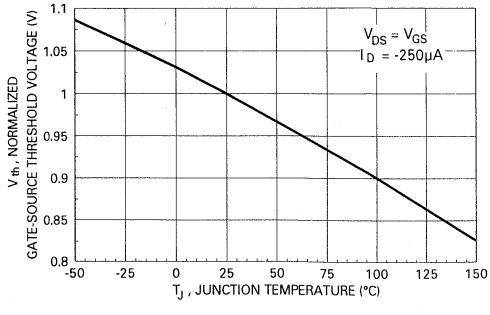


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

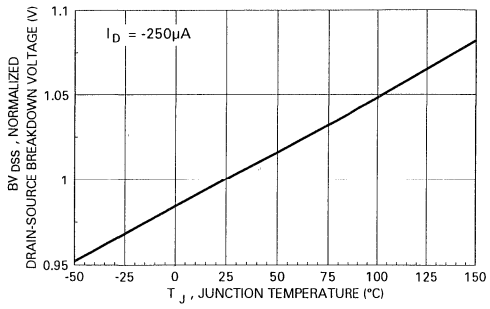


Figure 7. Breakdown Voltage Variation with Temperature

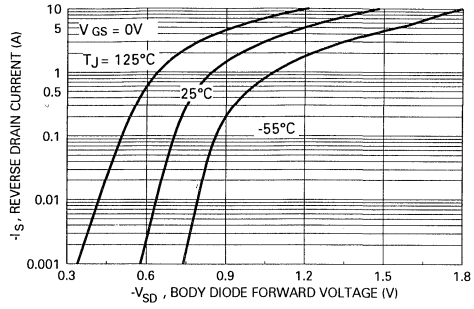


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

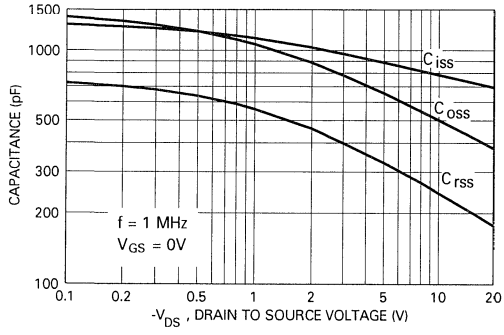


Figure 9. Capacitance Characteristics

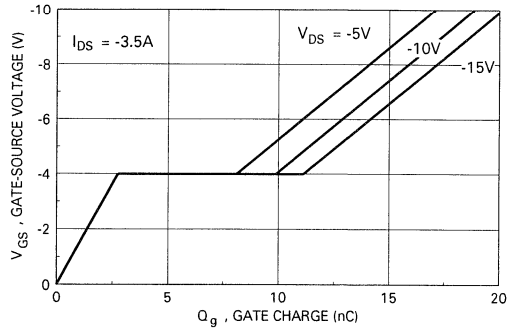


Figure 10. Gate Charge Characteristics

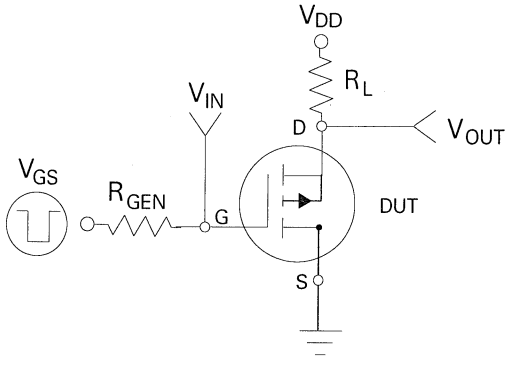


Figure 11. Switching Test Circuit

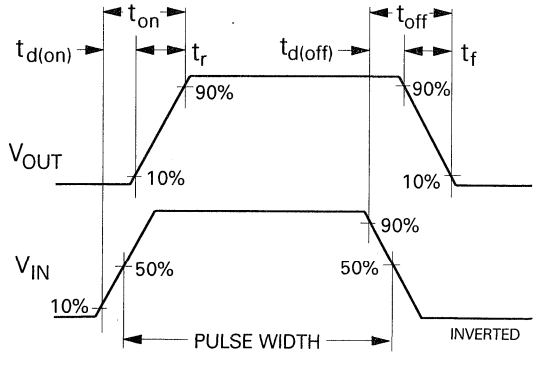


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

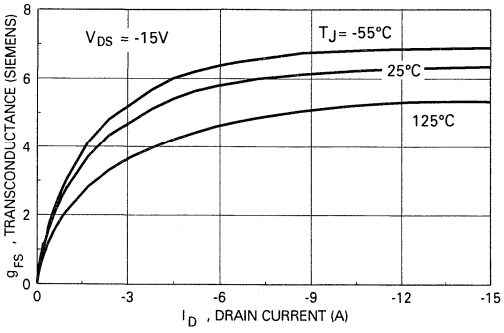


Figure 13. Transconductance Variation with Drain Current and Temperature

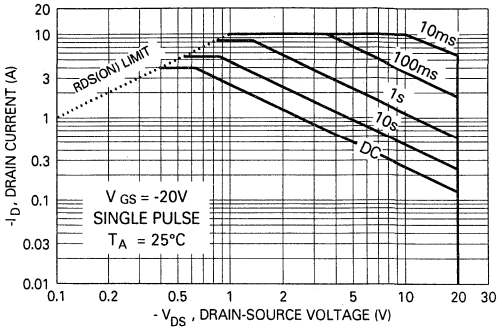


Figure 14. Maximum Safe Operating Area

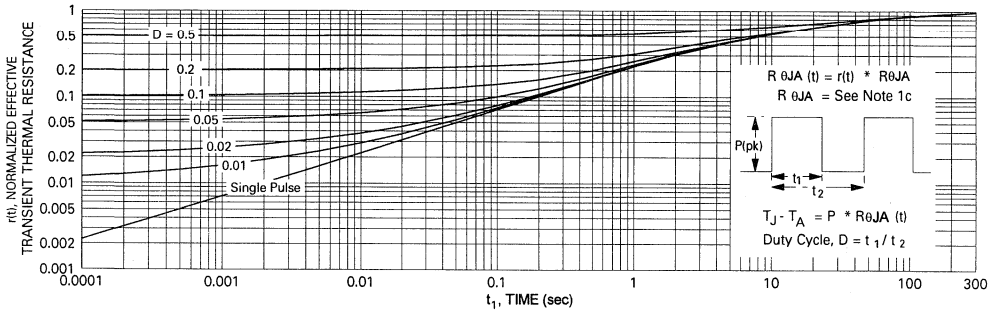


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

4

National Semiconductor™

May 1996

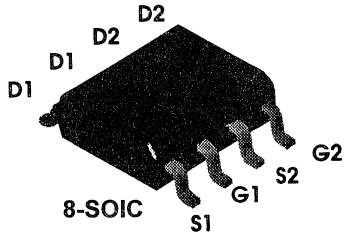
NDS9948
Dual P-Channel Enhancement Mode Field Effect Transistor

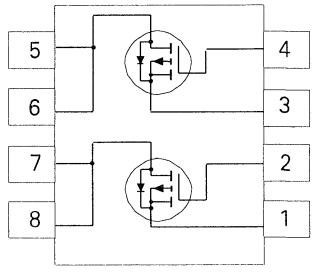
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -2.3A, -60V. $R_{DS(ON)}$ = 0.25Ω @ V_{GS} = -10V.
- High density cell design for low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9948	Units
V_{DSS}	Drain-Source Voltage		-60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 2.3	A
	- Pulsed T_A = 25°C		± 10	
	- Continuous T_A = 70°C	(Note 1a)	± 1.8	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -40 V, V_{GS} = 0 V			-2	µA
		T_J = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2.4	-3	V
		T_J=125°C	-0.8	-2	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.3 A		0.21	0.25	Ω
		T_J=125°C		0.3	0.4	
		V_{GS} = -4.5 V, I_D = -1.6 A		0.36	0.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-10			A
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -2.3 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		570		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -30 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		8	15	ns
t_r	Turn - On Rise Time			20	40	ns
$t_{D(off)}$	Turn - Off Delay Time			20	40	ns
t_f	Turn - Off Fall Time			5	20	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -2.3 A, V_{GS} = -10 V		16	25	nC
Q_{gs}	Gate-Source Charge			2	5	nC
Q_{gd}	Gate-Drain Charge			4	8	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.3 A (Note 2)		-0.98	-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

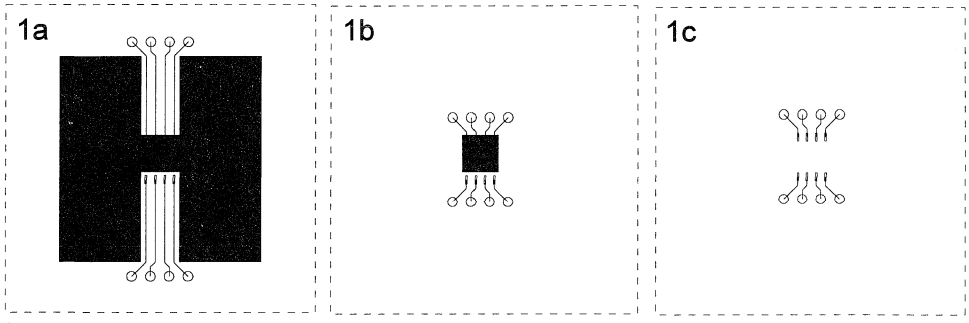
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

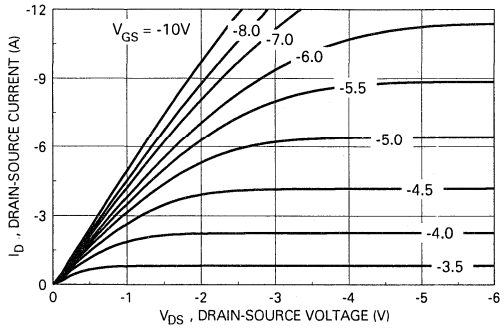


Figure 1. On-Region Characteristics.

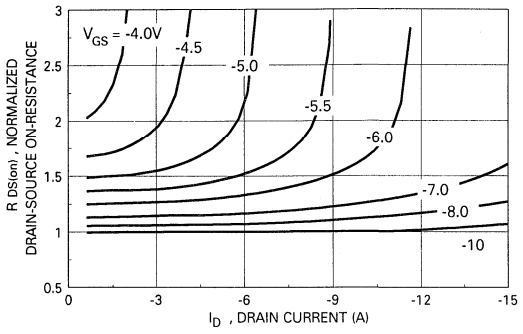


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

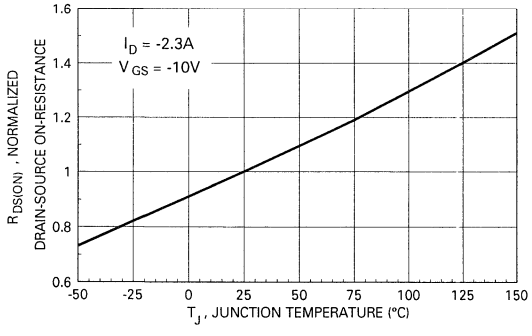


Figure 3. On-Resistance Variation with Temperature.

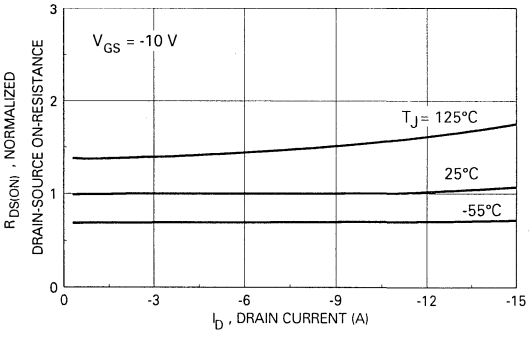


Figure 4. On-Resistance Variation with Drain Current and Temperature.

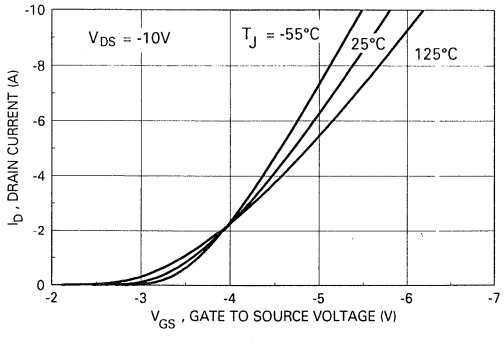


Figure 5. Transfer Characteristics

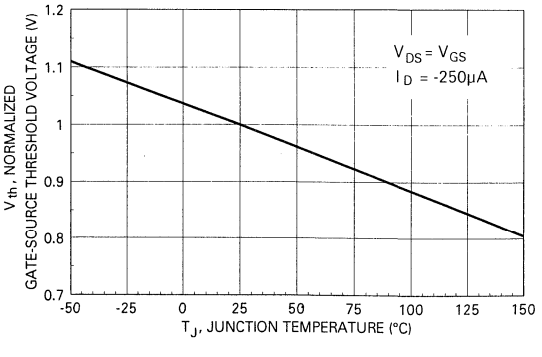


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

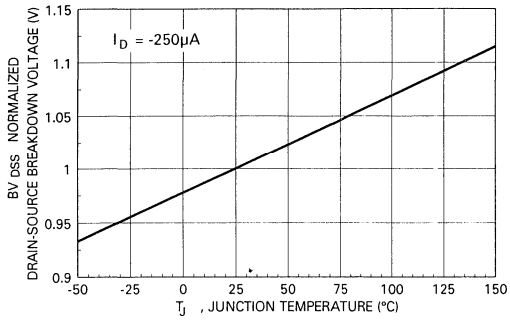


Figure 7. Breakdown Voltage Variation with Temperature.

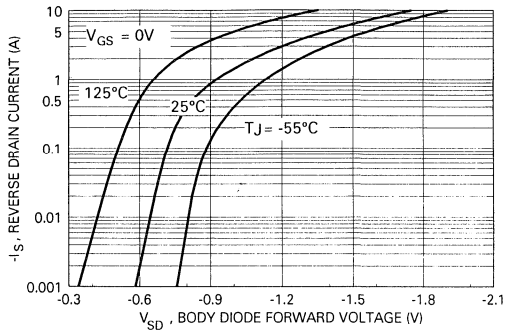


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

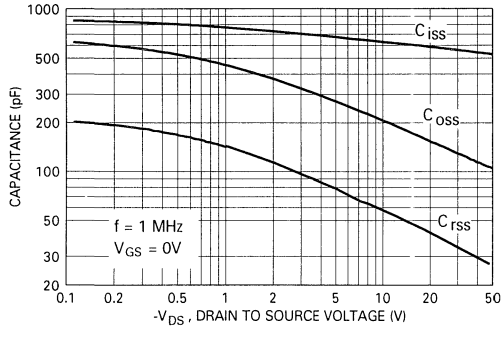


Figure 9. Capacitance Characteristics.

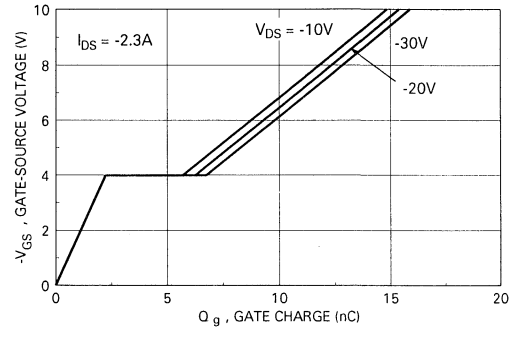


Figure 10. Gate Charge Characteristics

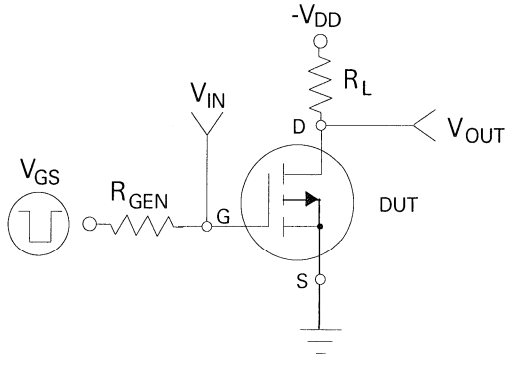


Figure 11. Switching Test Circuit

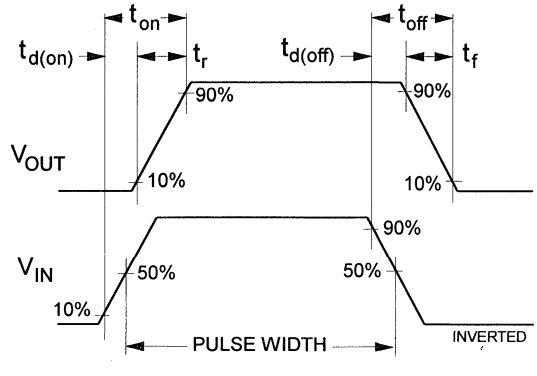


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

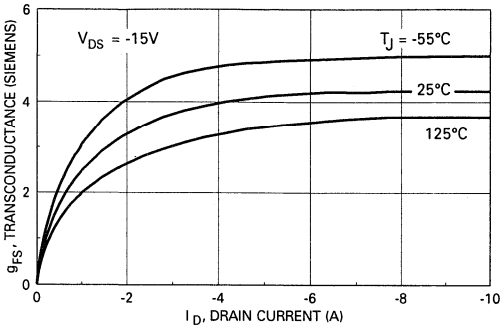


Figure 13. Transconductance Variation with Drain Current and Temperature.

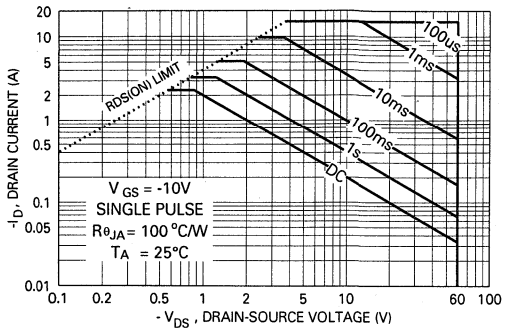


Figure 14. Maximum Safe Operating Area.

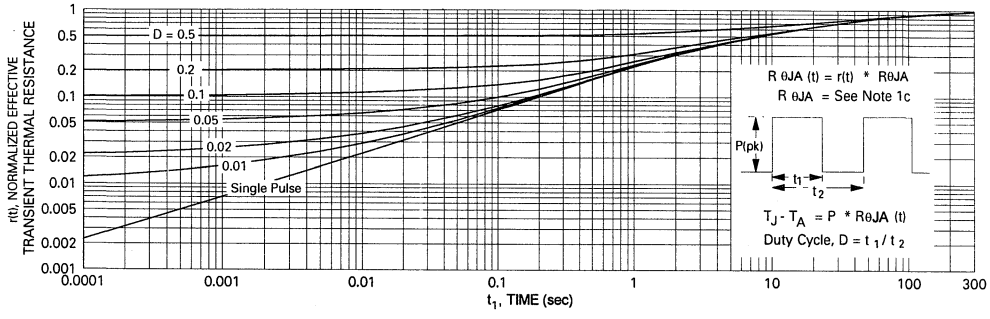


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

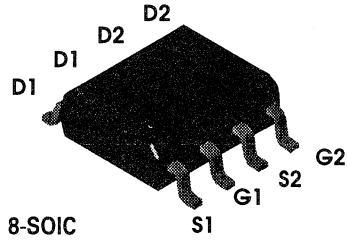
NDS9952A
Dual N & P-Channel Enhancement Mode Field Effect Transistor

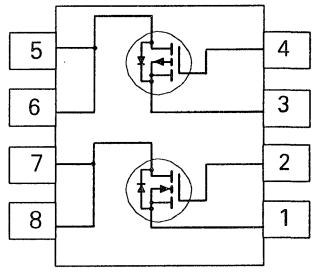
General Description

These dual N- and P-channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.7A, 30V, $R_{DS(ON)}$=0.08Ω @ V_{GS}=10V.
  P-Channel -2.9A, -30V, $R_{DS(ON)}$=0.13Ω @ V_{GS}=-10V.
- High density cell design or extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		30	-30	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 3.7	± 2.9	A
	- Pulsed		± 15	± 10	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	30			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	N-Ch			2	µA
		T_J = 55°C				25	µA
		V_{DS} = -24 V, V_{GS} = 0 V	P-Ch			-2	µA
		T_J = 55°C				-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.7	2.8	V
		T_J = 125°C		0.7	1.2	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-1.6	-2.8	
		T_J = 125°C		-0.85	-1.25	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.0 A	N-Ch		0.06	0.08	Ω
		T_J = 125°C			0.08	0.13	
		V_{GS} = 4.5 V, I_D = 0.5 A			0.08	0.11	
		T_J = 125°C			0.11	0.18	
		V_{GS} = -10 V, I_D = -1.0 A	P-Ch		0.11	0.13	
		T_J = 125°C			0.15	0.21	
		V_{GS} = -4.5 V, I_D = -0.5 A			0.17	0.2	
		T_J = 125°C			0.24	0.32	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	15			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-10			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.7 A	N-Ch		6		S
		V_{DS} = -15 V, I_D = -2.9 A	P-Ch		4		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		320		pF
			P-Ch		350		
C_{oss}	Output Capacitance		N-Ch		225		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		260		
C_{rss}	Reverse Transfer Capacitance		N-Ch		85		pF
			P-Ch		100		

4

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	N-Ch		10	15	ns
			P-Ch		9	40	
t_r	Turn - On Rise Time		N-Ch		13	20	ns
		P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	P-Ch		21	40	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		21	50	ns
			P-Ch		21	90	
t_f	Turn - Off Fall Time		N-Ch		5	50	ns
			P-Ch		8	50	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 3.7 A, V_{GS} = 10 V	N-Ch		9.5	27	nC
			P-Ch		10	25	
Q_{gs}	Gate-Source Charge		N-Ch		1.5		nC
		P-Channel V_{DS} = -10 V, I_D = -2.9 A, V_{GS} = -10 V	P-Ch		1.6		
Q_{gd}	Gate-Drain Charge		N-Ch		3.3		nC
			P-Ch		3.4		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.2	A
			P-Ch			-1.2	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)	N-Ch		0.8	1.3	V
		V_{GS} = 0 V, I_S = -1.25 A (Note 2)	P-Ch		-0.8	-1.3	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs	N-Ch			75	ns
		V_{GS} = 0 V, I_F = -1.25 A, dI_F/dt = 100 A/µs	P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

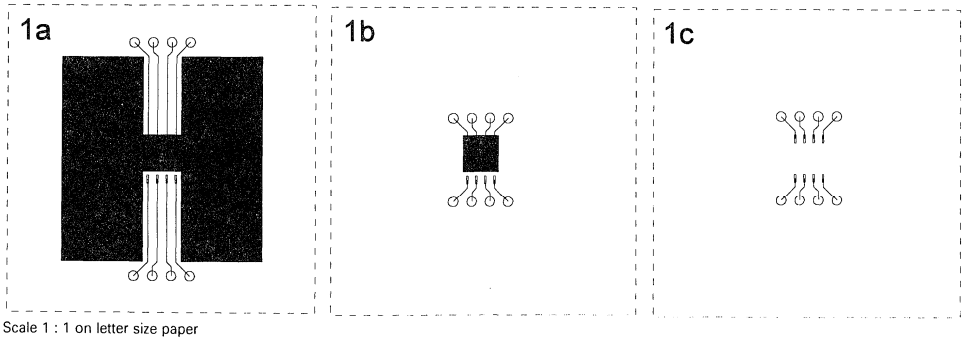
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

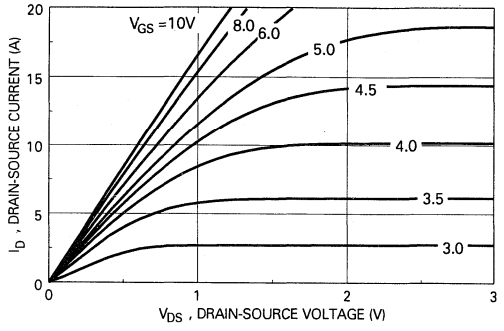


Figure 1. N-Channel On-Region Characteristics.

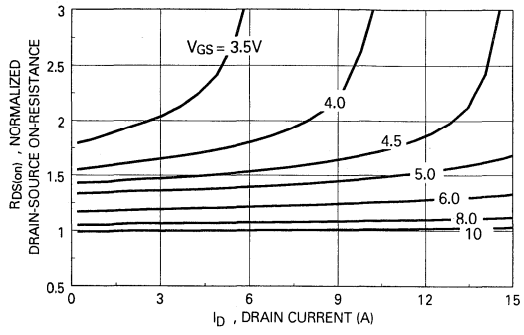


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

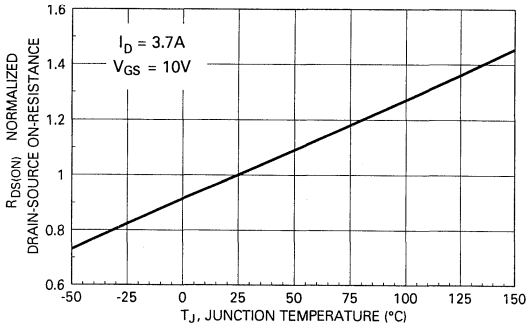


Figure 3. N-Channel On-Resistance Variation with Temperature.

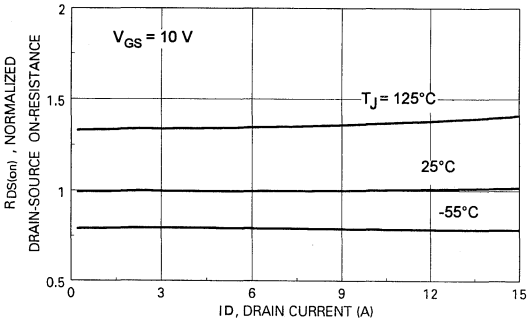


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

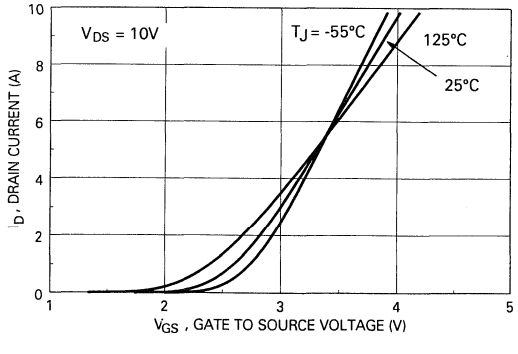


Figure 5. N-Channel Transfer Characteristics.

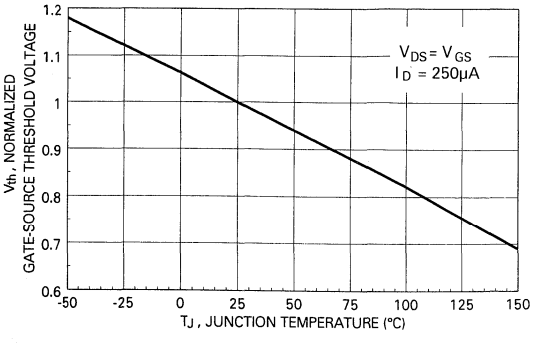


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

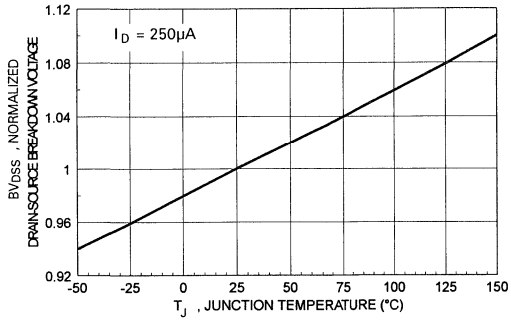


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

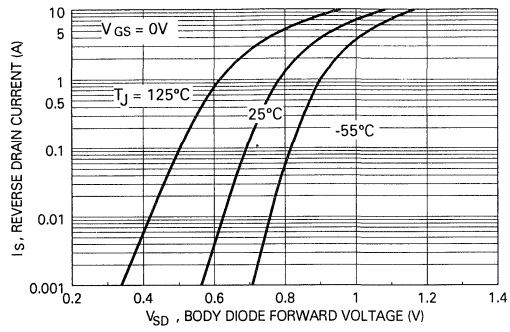


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

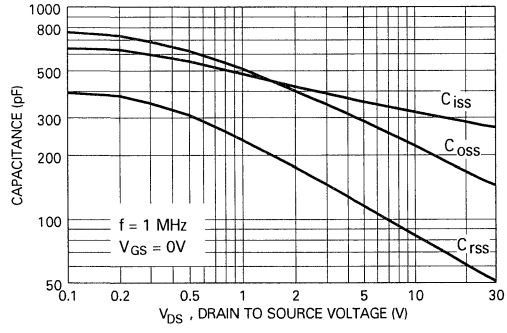


Figure 9. N-Channel Capacitance Characteristics.

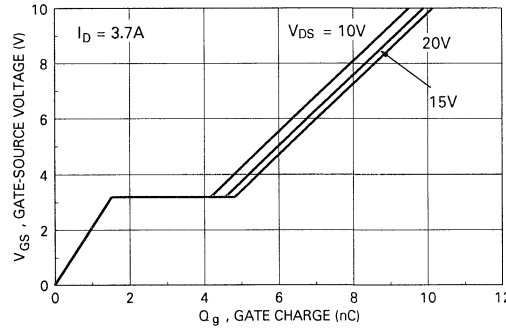


Figure 10. N-Channel Gate Charge Characteristics.

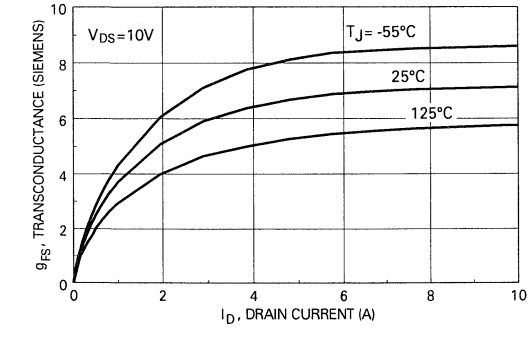


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

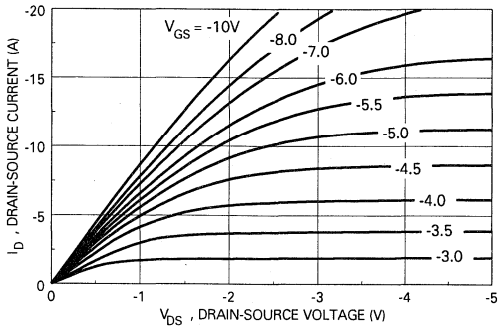


Figure 12. P-Channel On-Region Characteristics.

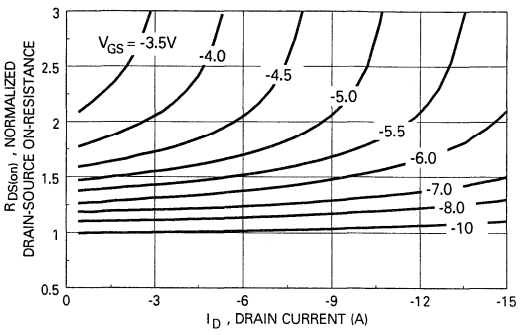


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

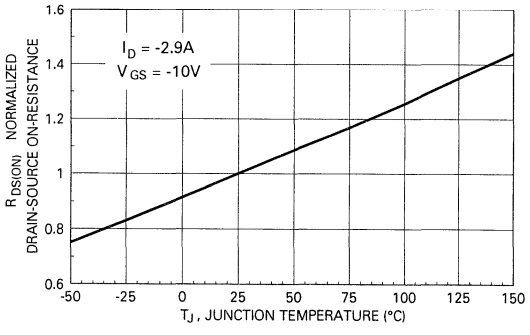


Figure 14. P-Channel On-Resistance Variation with Temperature.

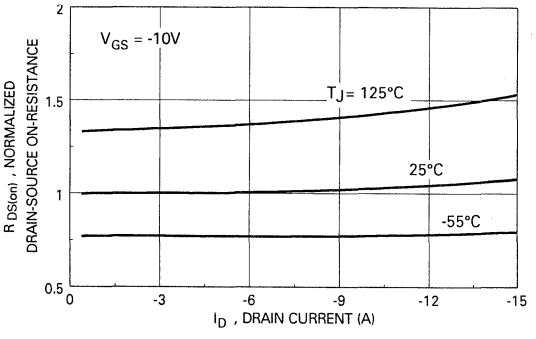


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

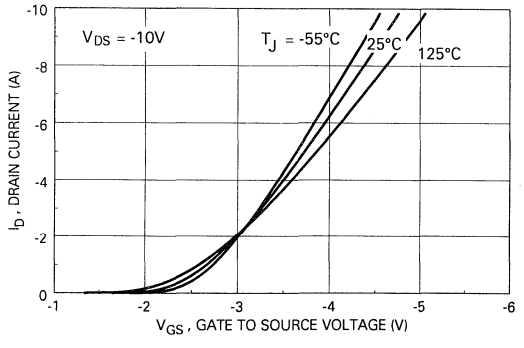


Figure 16. P-Channel Transfer Characteristics.

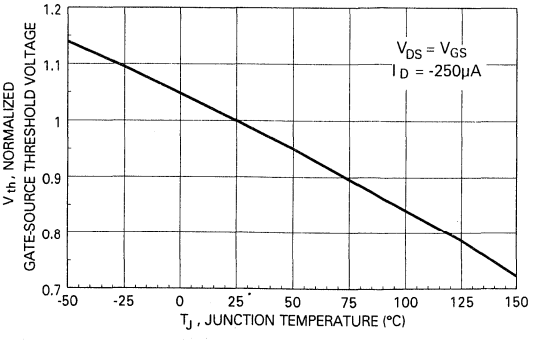


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

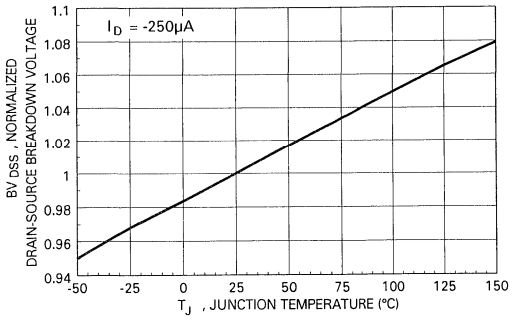


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

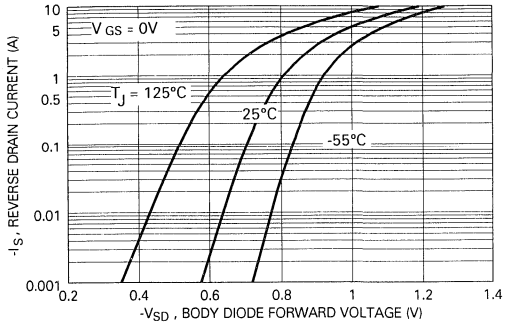


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

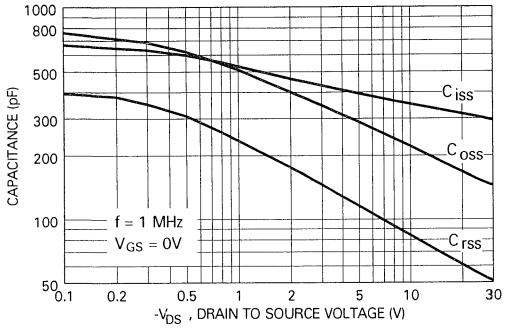


Figure 20. P-Channel Capacitance Characteristics.

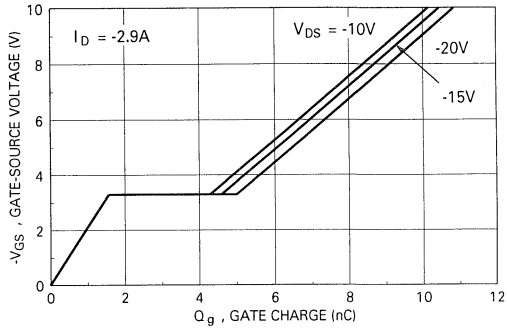


Figure 21. P-Channel Gate Charge Characteristics.

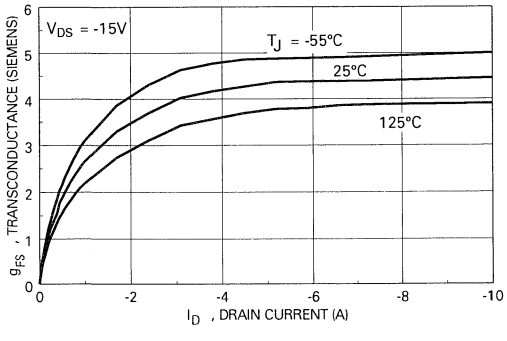


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

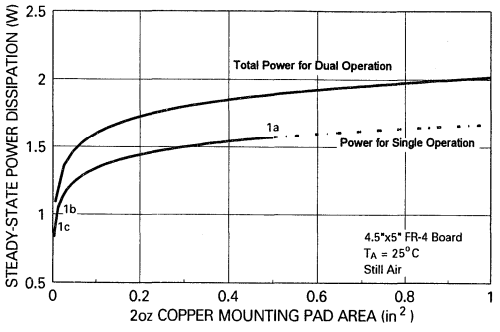


Figure 23. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

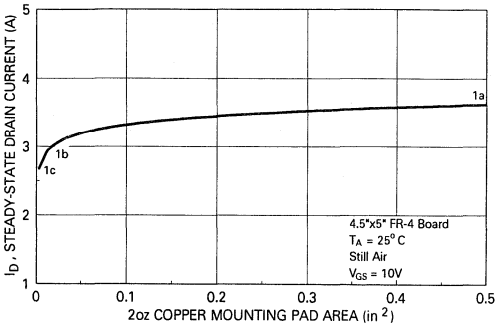


Figure 24. N-Ch Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

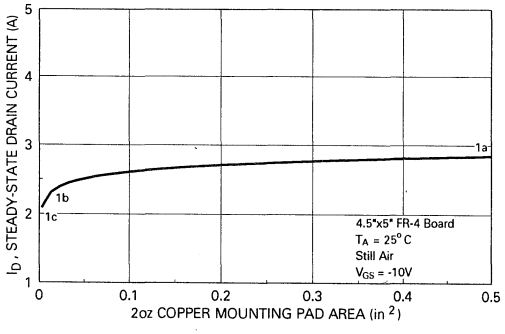


Figure 25. P-Ch Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

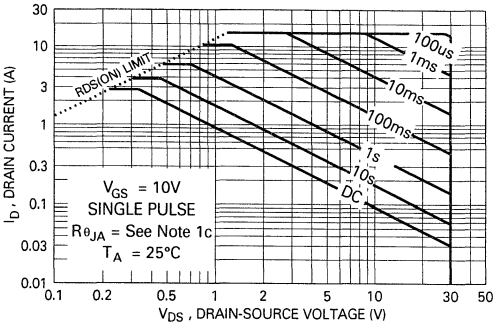


Figure 26. N-Channel Maximum Safe Operating Area.

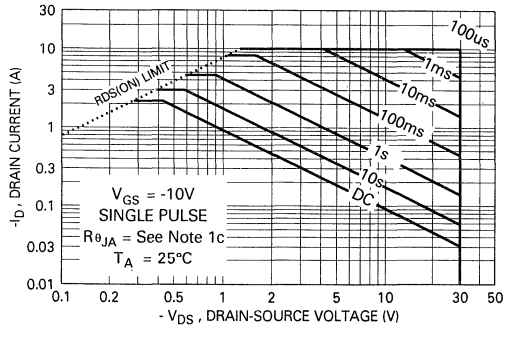


Figure 27. P-Channel Maximum Safe Operating Area.

Typical Thermal Characteristics: N & P-Channel

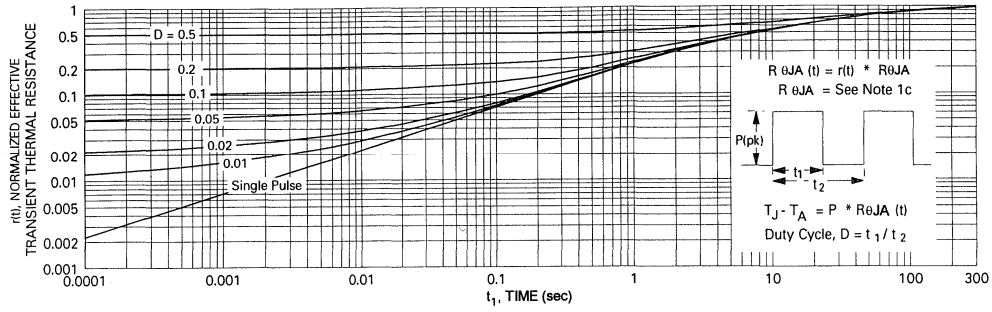


Figure 28. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

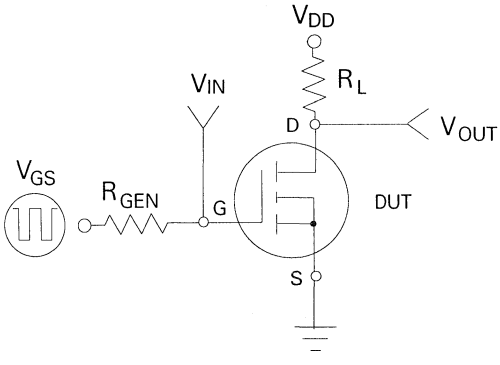


Figure 29. N or P-Channel Switching Test Circuit.

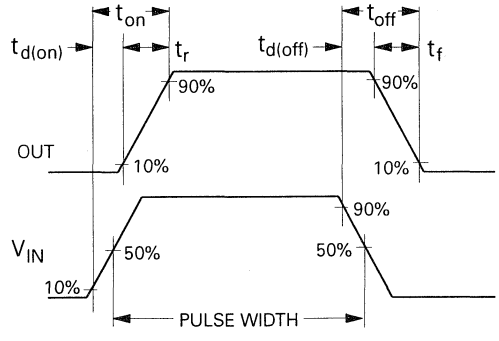


Figure 30. N or P-Channel Switching Waveforms.

National Semiconductor™

May 1996

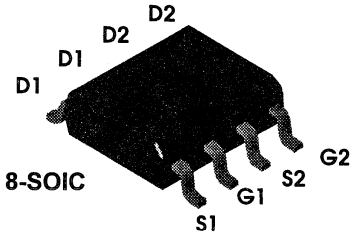
NDS9953A
Dual P-Channel Enhancement Mode Field Effect Transistor

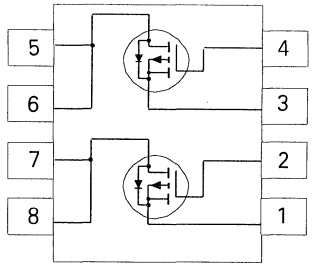
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- -2.9A, -30V. $R_{DS(ON)}$ = 0.13Ω @ V_{GS} = -10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		NDS9953A	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 2.9	A
	- Pulsed		± 10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-2	µA
		T_J = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.6	-2.8	V
		T_J = 125°C	-0.85	-1.25	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1.0 A		0.11	0.13	Ω
		T_J = 125°C		0.15	0.21	
		V_{GS} = -4.5 V, I_D = -0.5 A		0.17	0.2	
		T_J = 125°C		0.24	0.32	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-10			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-1.5			
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -2.9 A		4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		350		pF
C_{oss}	Output Capacitance			260		pF
C_{rss}	Reverse Transfer Capacitance			100		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		9	40	ns
t_r	Turn - On Rise Time			21	40	ns
$t_{D(off)}$	Turn - Off Delay Time			21	90	ns
t_f	Turn - Off Fall Time			8	50	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -2.9 A, V_{GS} = -10 V		10	25	nC
Q_{gs}	Gate-Source Charge			1.6		nC
Q_{gd}	Gate-Drain Charge			3.4		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.25 A (Note 2)		-0.8	-1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = -1.25 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

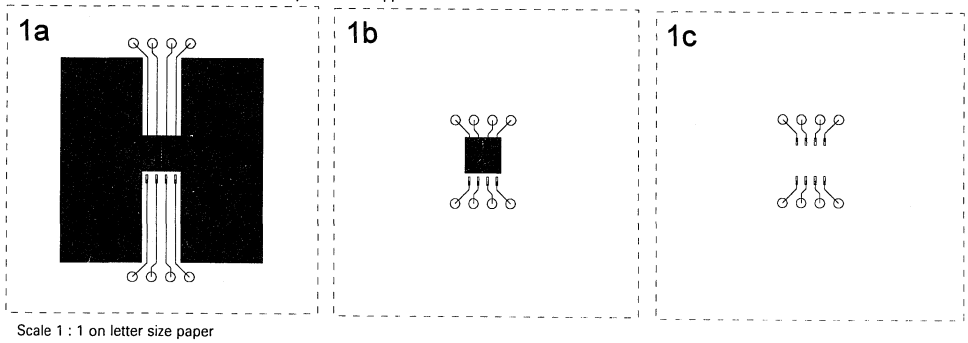
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

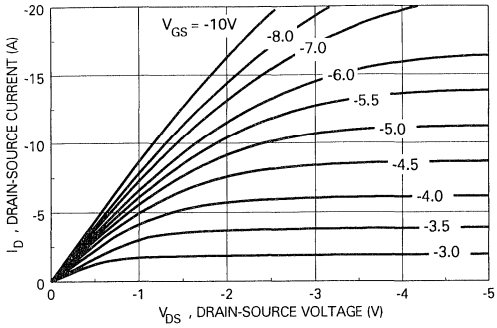


Figure 1. On-Region Characteristics.

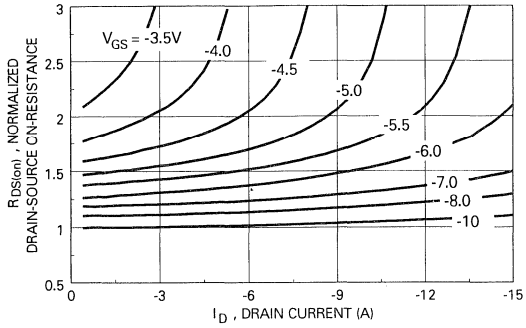


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

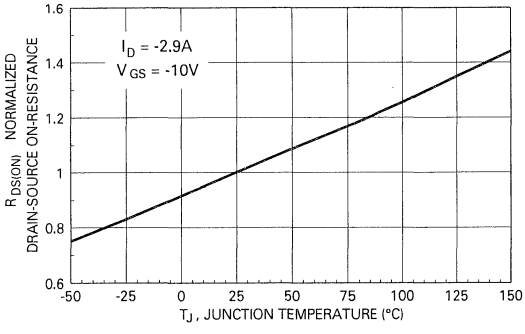


Figure 3. On-Resistance Variation with Temperature.

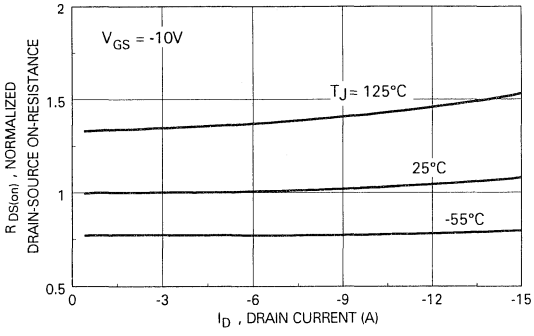


Figure 4. On-Resistance Variation with Drain Current and Temperature.

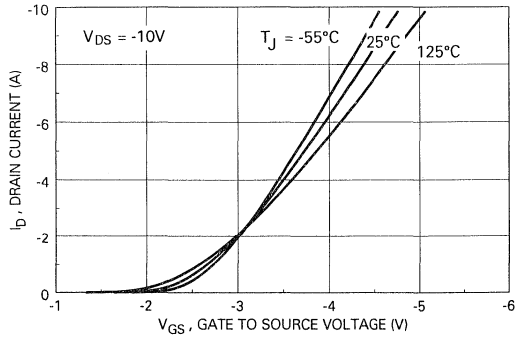


Figure 5. Transfer Characteristics.

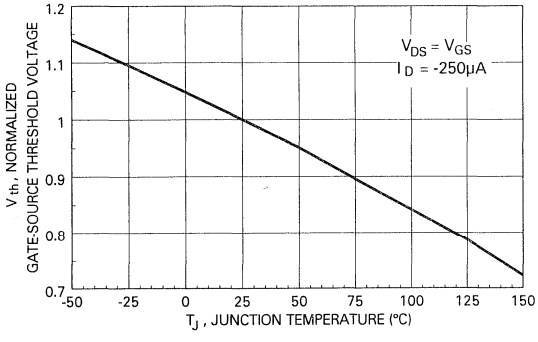


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

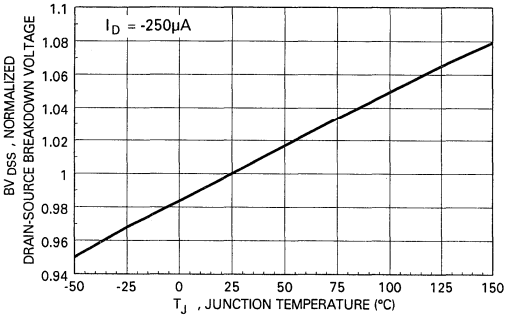


Figure 7. Breakdown Voltage Variation with Temperature.

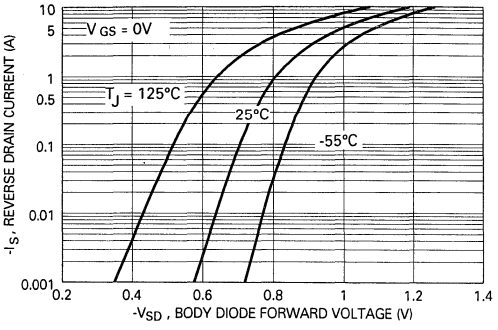


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

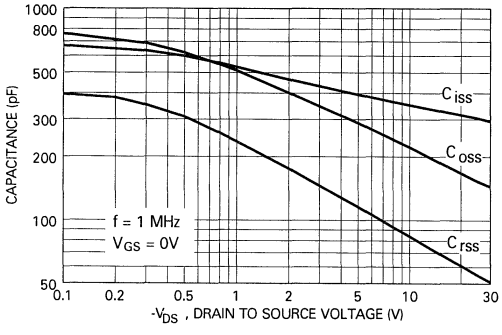


Figure 9. Capacitance Characteristics.

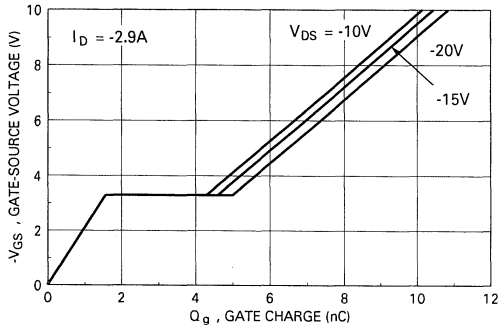


Figure 10. Gate Charge Characteristic.

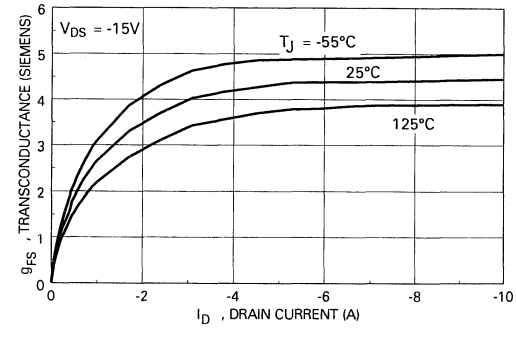


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

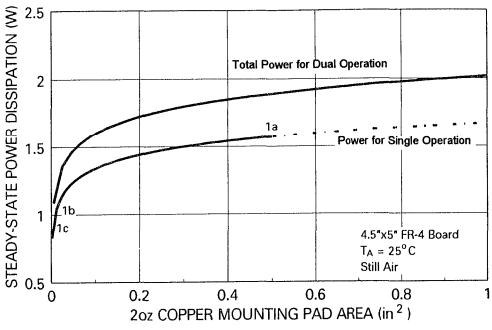


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

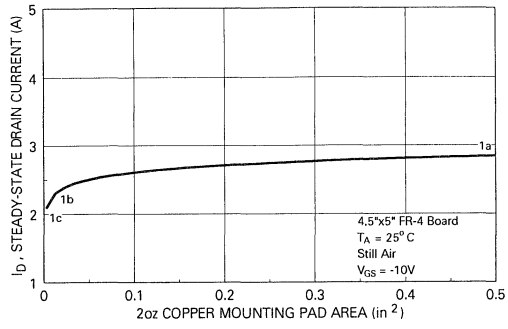


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

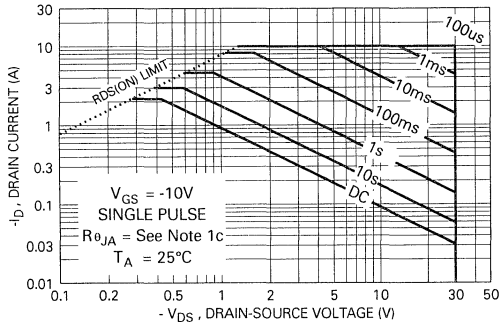


Figure 14. Maximum Safe Operating Area.

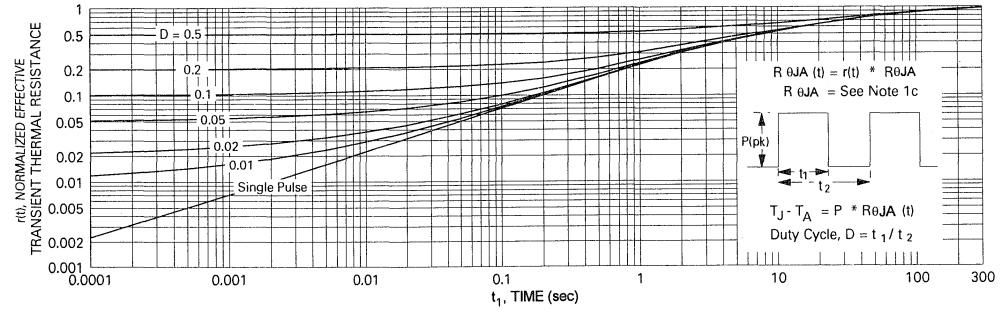


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

NDS9955

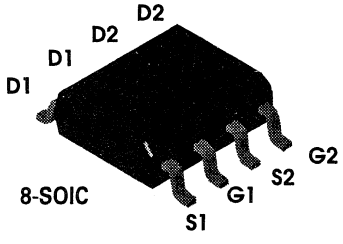
Dual N-Channel Enhancement Mode Field Effect Transistor

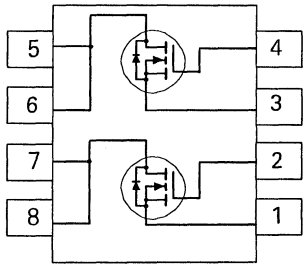
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.0A, 50V. $R_{DS(ON)}$ = 0.13Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





4

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9955	Units
V_{DSS}	Drain-Source Voltage		50	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	(Note 1a)	± 3.0	A
	- Continuous @ T_A = 70°C	(Note 1a)	± 2.3	
	- Pulsed @ T_A = 25°C		± 10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		T_J = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		T_J = 125°C	0.7		2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.0 A		0.084	0.13	Ω
		T_J = 125°C		0.13	0.2	
		V_{GS} = 4.5 V, I_D = 1.5 A		0.11	0.2	
		T_J = 125°C		0.17	0.3	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	10			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	3.5			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 3.0 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		435		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	20	ns
t_r	Turn - On Rise Time			4	20	ns
$t_{D(off)}$	Turn - Off Delay Time			24	70	ns
t_f	Turn - Off Fall Time			7	50	ns
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 2 A, V_{GS} = 10 V		13	30	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			4.2		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5A (Note 2)		0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 1.5 A, dI_F/dt = 100 A/µs		52	100	ns
I_{rr}	Reverse Recovery Current			2.3		A

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

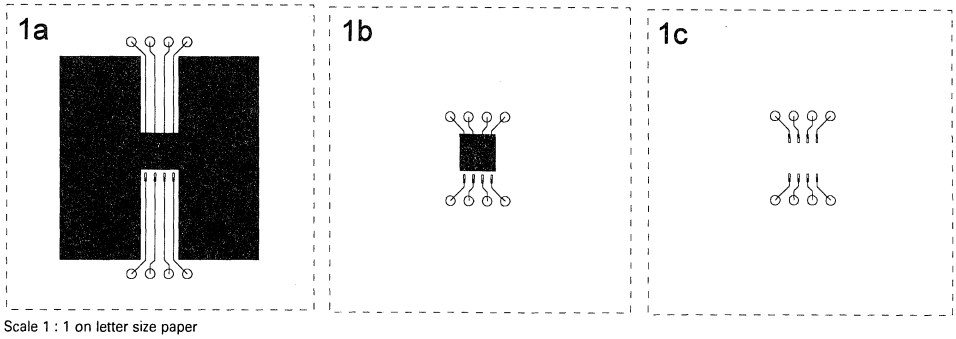
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

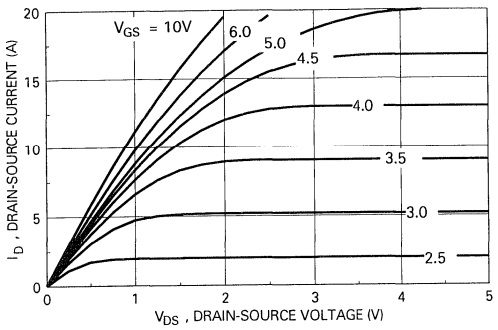


Figure 1. On-Region Characteristics.

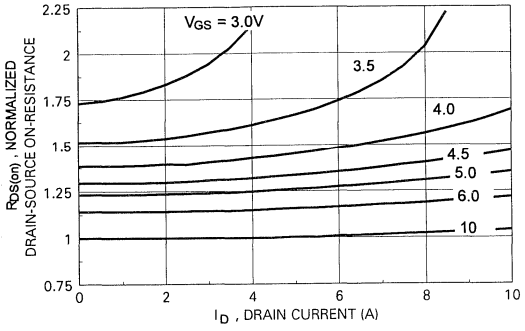


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

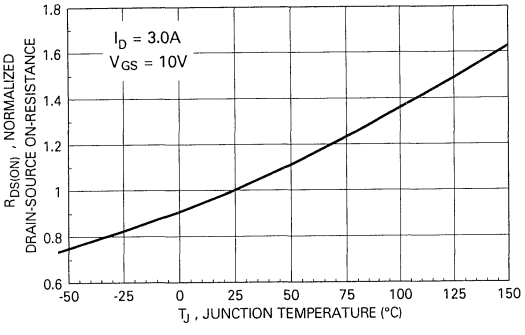


Figure 3. On-Resistance Variation with Temperature.

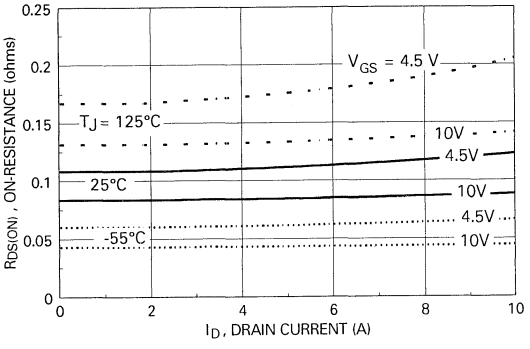


Figure 4. On-Resistance Variation with Drain Current and Temperature.

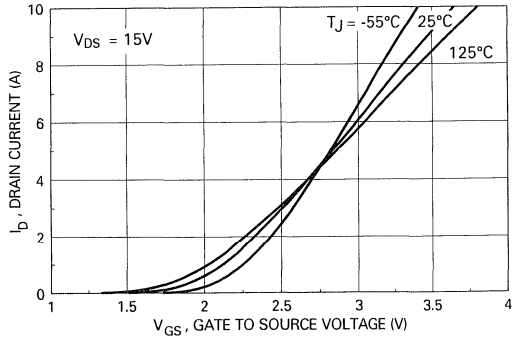


Figure 5. Transfer Characteristics.

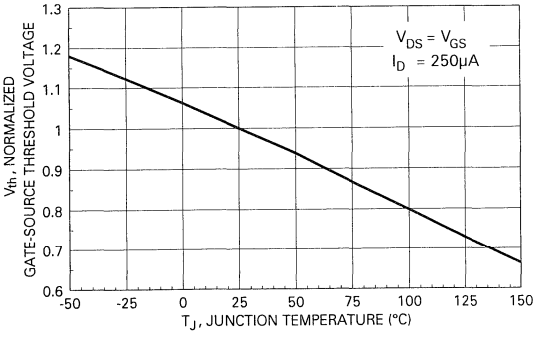


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

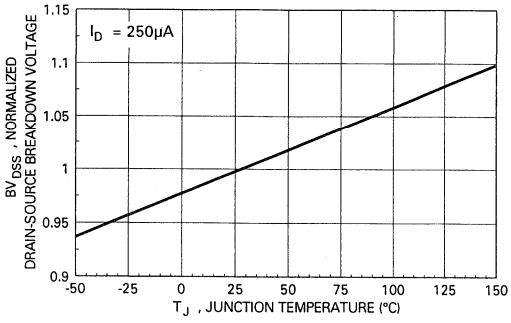


Figure 7. Breakdown Voltage Variation with Temperature.

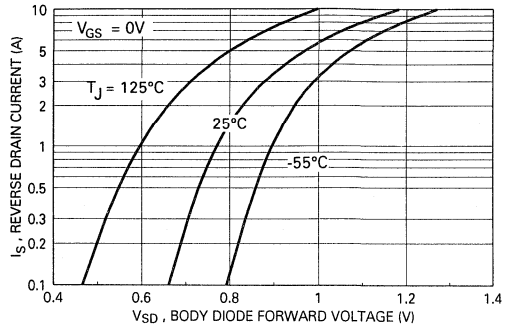


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

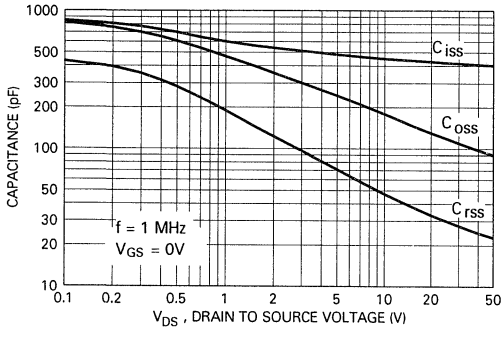


Figure 9. Capacitance Characteristics.

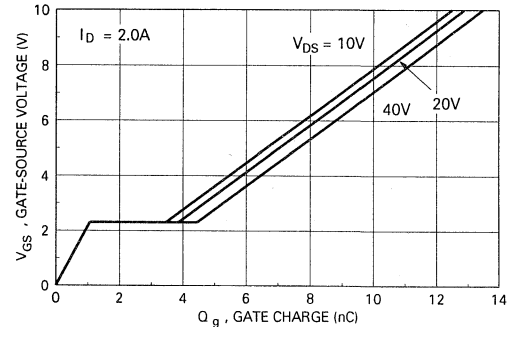


Figure 10. Gate Charge Characteristics.

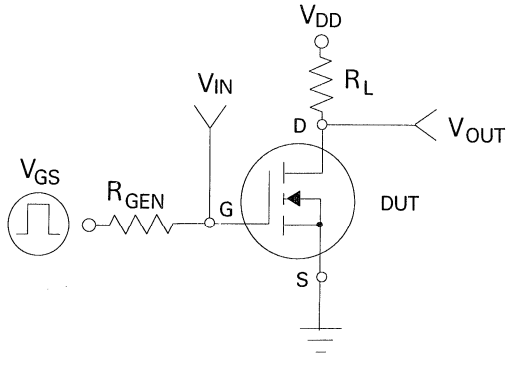


Figure 11. Switching Test Circuit.

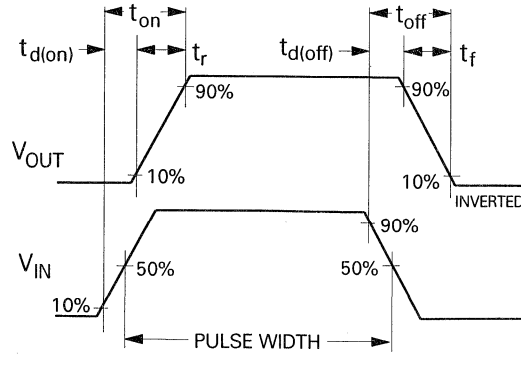


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

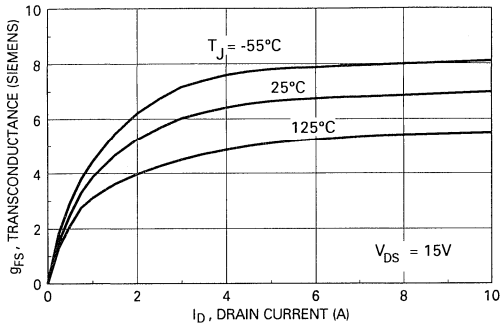


Figure 13. Transconductance Variation with Drain Current and Temperature.

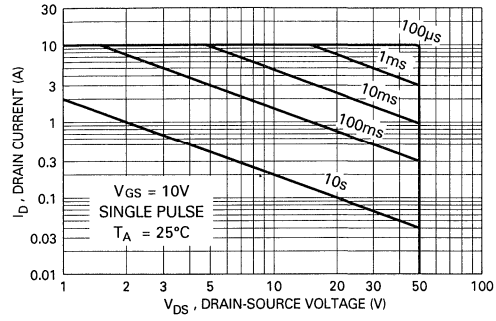


Figure 14. Maximum Safe Operating Area.

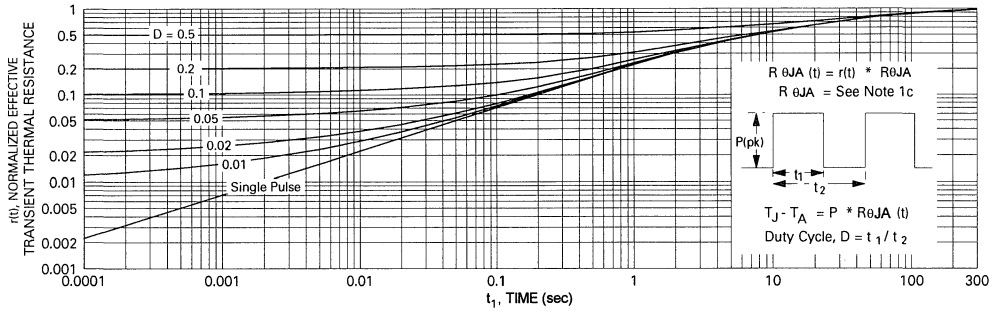


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

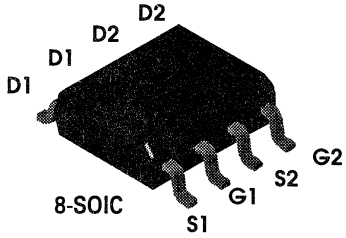
NDS9956A
Dual N-Channel Enhancement Mode Field Effect Transistor

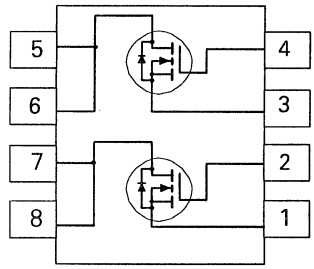
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.7A, 30V. $R_{DS(ON)}$ = 0.08Ω @ V_{GS} = 10V
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





4

Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter		NDS9956A	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 3.7	A
	- Pulsed		± 15	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		T_J = 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.7	2.8	V
		T_J = 125°C	0.7	1.2	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.2 A		0.06	0.08	Ω
		T_J = 125°C		0.08	0.13	
		V_{GS} = 4.5 V, I_D = 1.0 A		0.08	0.11	
		T_J = 125°C		0.11	0.18	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	15			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	3.5			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.7 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		320		pF
C_{oss}	Output Capacitance			225		pF
C_{rss}	Reverse Transfer Capacitance			85		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn - On Rise Time			13	20	ns
$t_{D(off)}$	Turn - Off Delay Time			21	50	ns
t_f	Turn - Off Fall Time			5	50	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 3.7 A, V_{GS} = 10 V		9.5	27	nC
Q_{gs}	Gate-Source Charge			1.5		nC
Q_{gd}	Gate-Drain Charge			3.3		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				1.2	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

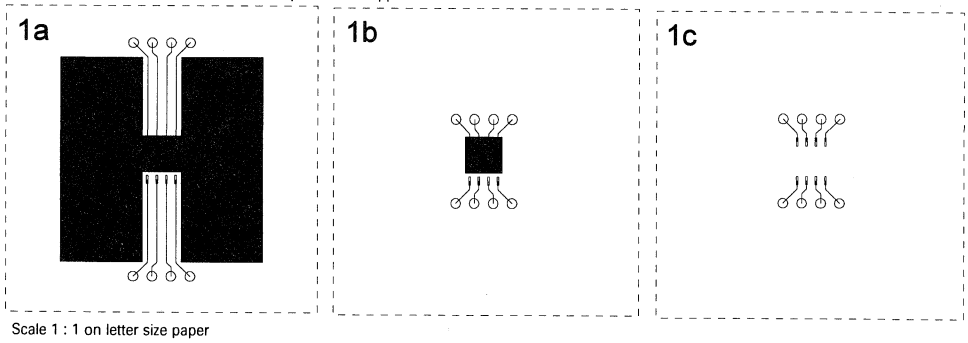
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

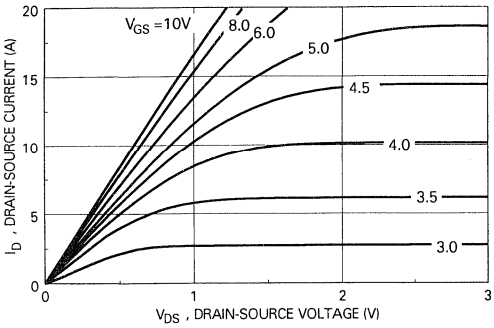


Figure 1. On-Region Characteristics.

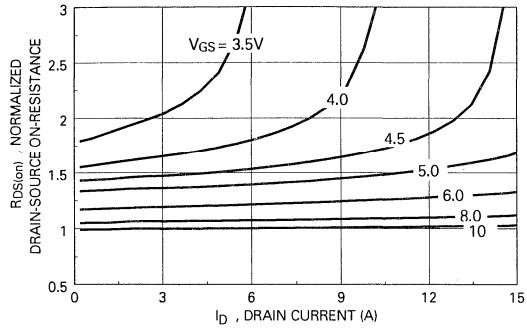


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

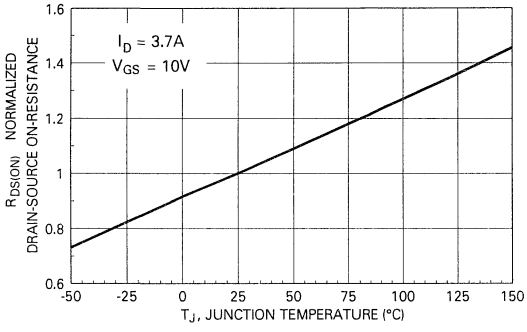


Figure 3. On-Resistance Variation with Temperature.

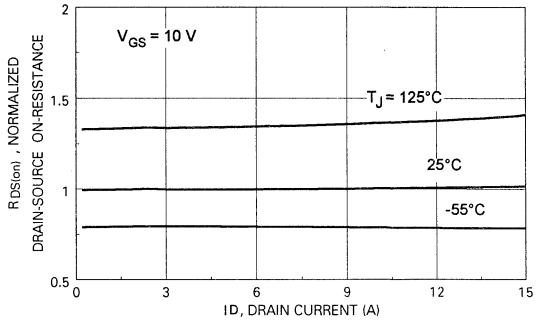


Figure 4. On-Resistance Variation with Drain Current and Temperature.

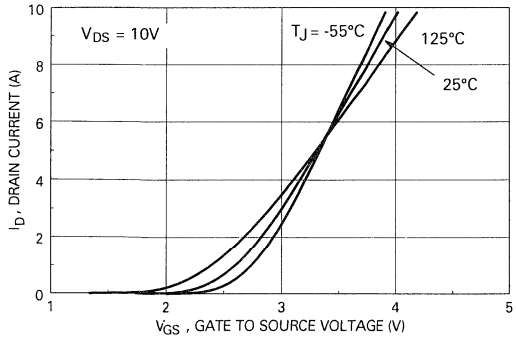


Figure 5. Transfer Characteristics.

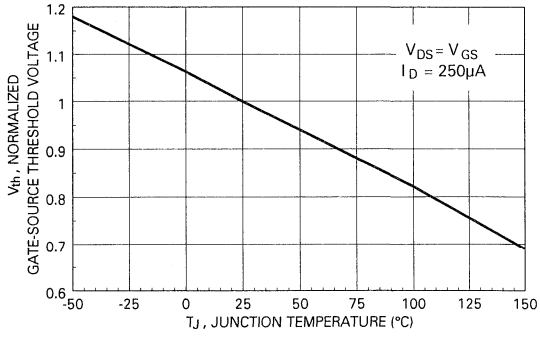


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

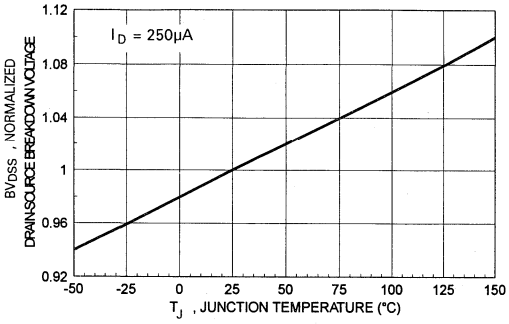


Figure 7. Breakdown Voltage Variation with Temperature.

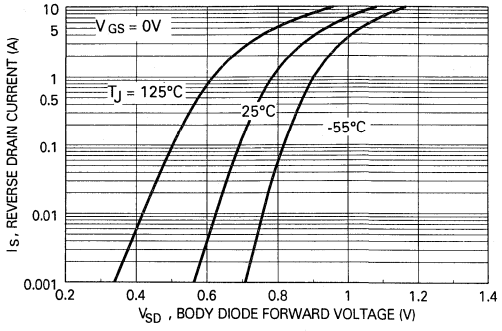


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

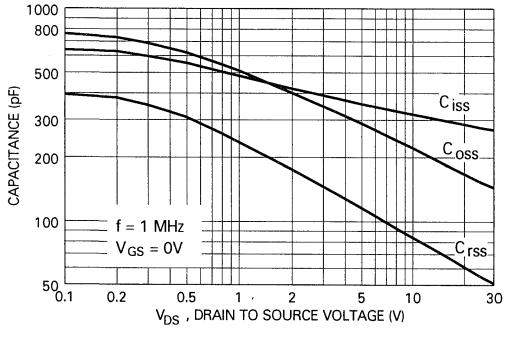


Figure 9. Capacitance Characteristics.

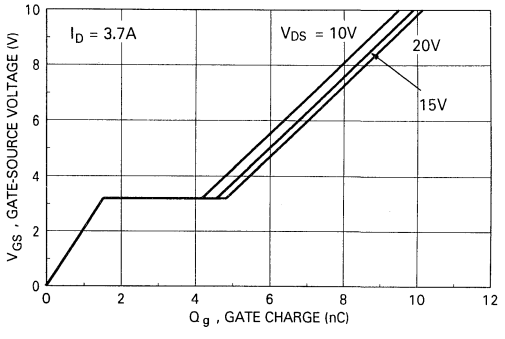


Figure 10. Gate Charge Characteristics.

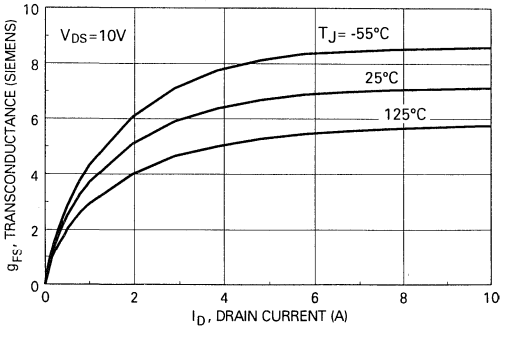


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

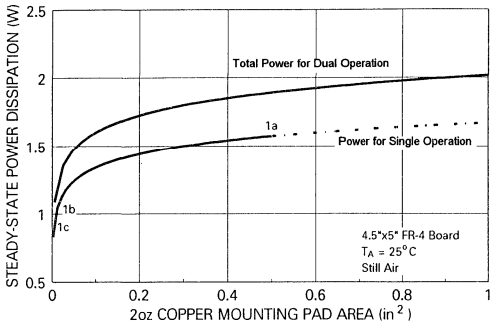


Figure 12. SO-8 Dual Package Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

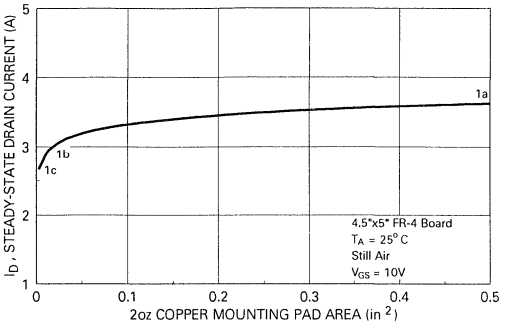


Figure 13. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

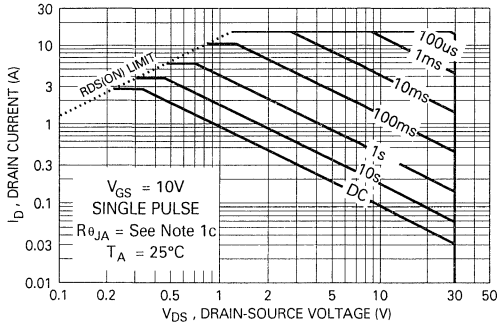


Figure 14. Maximum Safe Operating Area.

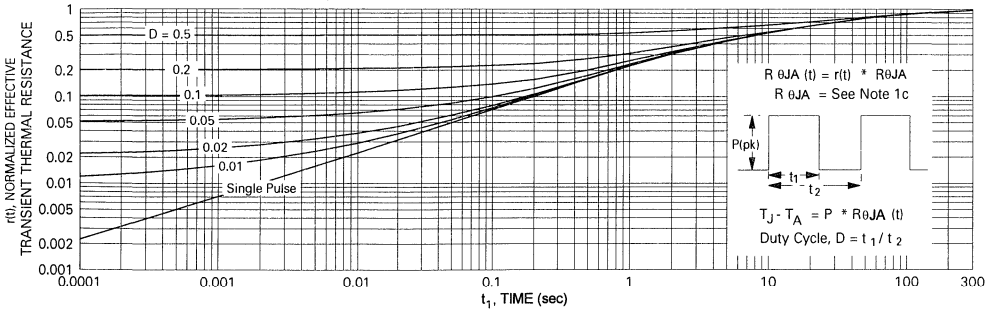


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

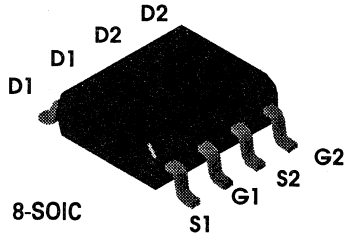
NDS9957
Dual N-Channel Enhancement Mode Field Effect Transistor

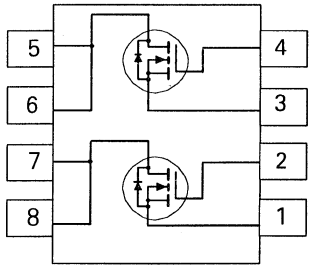
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.6A, 60V. $R_{DS(ON)}$ = 0.16Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.





4

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9957	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 2.6	A
	- Pulsed		± 10	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			1	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		T_A = 125°C	0.7	1.1	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.6 A		0.145	0.16	Ω
		T_A = 125°C		0.25	0.3	
		V_{GS} = 4.5 V, I_D = 2.1 A		0.19	0.25	
		T_A = 125°C		0.32	0.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 2.6 A		4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1.0 MHz		200		pF
C_{oss}	Output Capacitance			60		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		6	20	ns
t_r	Turn - On Rise Time			11	25	ns
$t_{D(off)}$	Turn - Off Delay Time			17	30	ns
t_f	Turn - Off Fall Time			4	15	ns
Q_g	Total Gate Charge	V_{DS} = 30 V, I_D = 2.6 A, V_{GS} = 10 V		7.5	12	nC
Q_{gs}	Gate-Source Charge			2.8		nC
Q_{gd}	Gate-Drain Charge			0.8		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.6 A (Note 2)		0.9	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

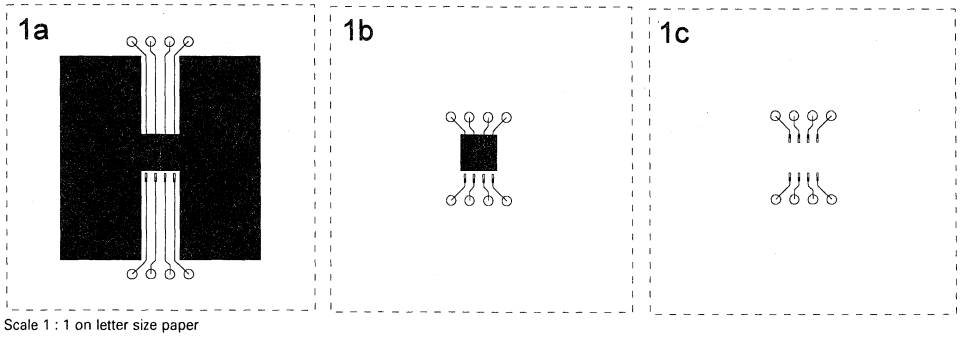
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in^2 pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in^2 pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

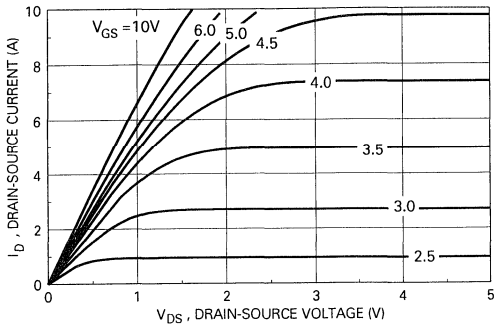


Figure 1. On-Region Characteristics.

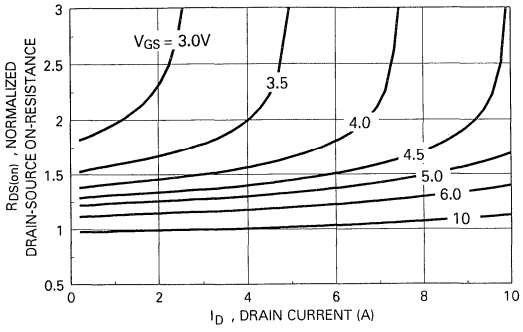


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

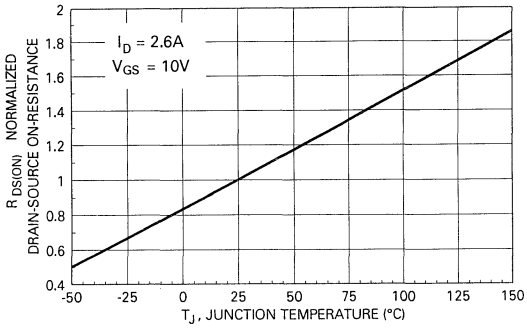


Figure 3. On-Resistance Variation with Temperature.

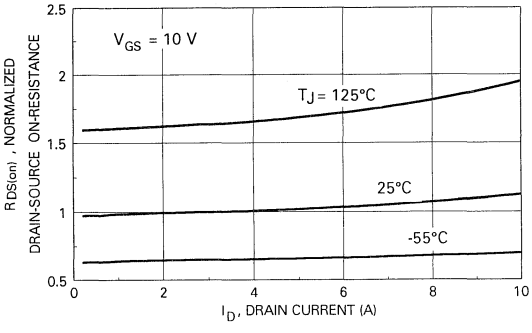


Figure 4. On-Resistance Variation with Drain Current and Temperature.

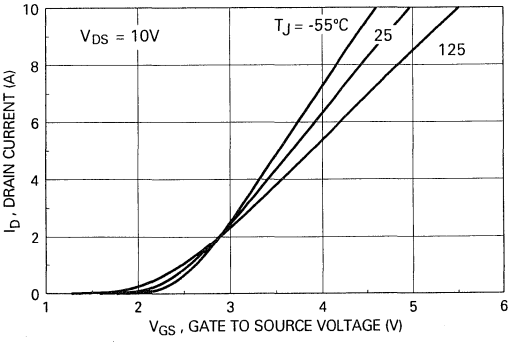


Figure 5. Transfer Characteristics.

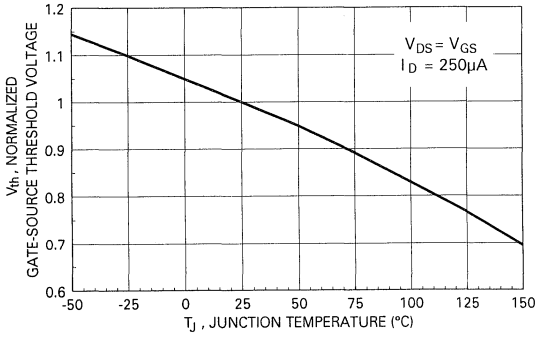


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

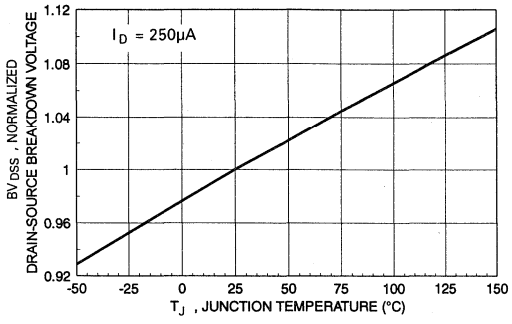


Figure 7. Breakdown Voltage Variation with Temperature.

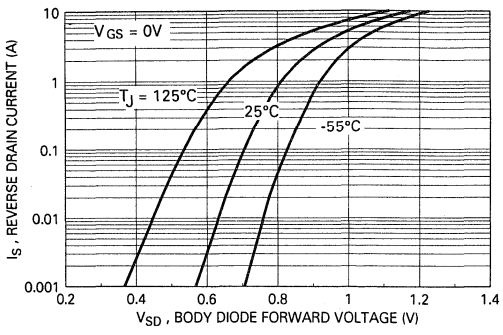


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

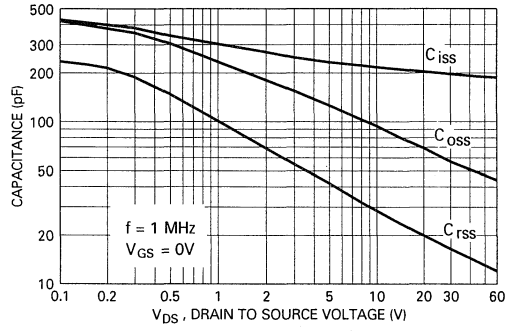


Figure 9. Capacitance Characteristics.

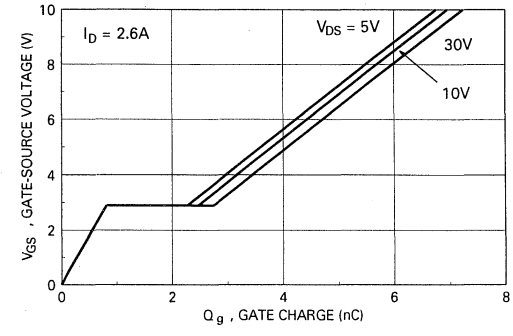


Figure 10. Gate Charge Characteristics.

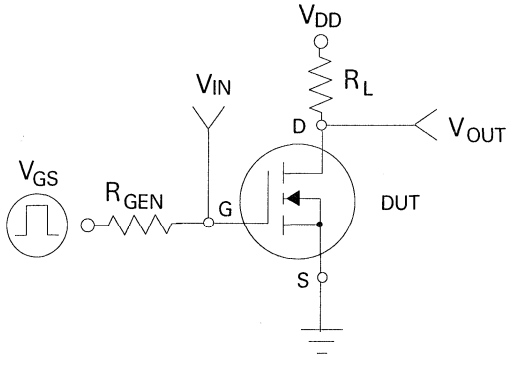


Figure 11. Switching Test Circuit

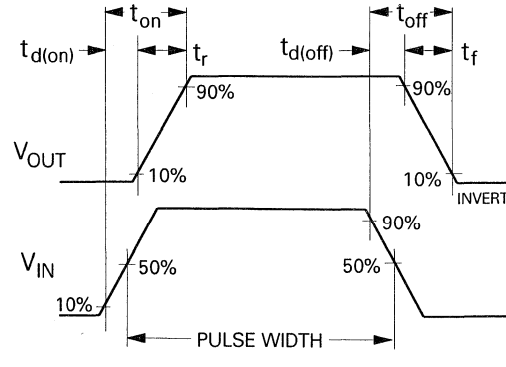


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

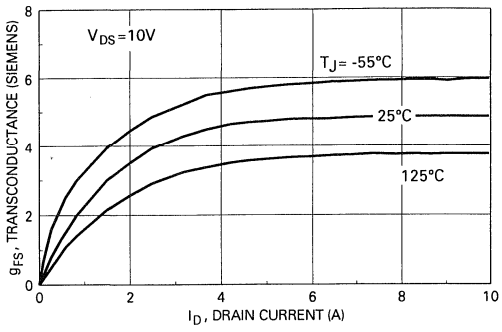


Figure 13. Transconductance Variation with Drain Current and Temperature.

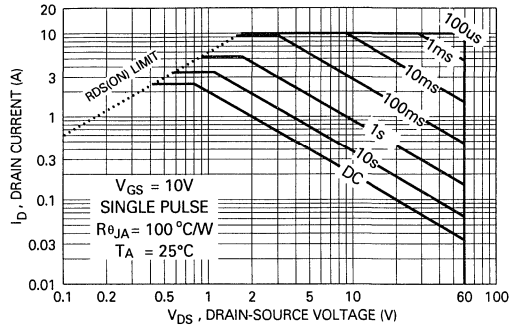


Figure 14. Maximum Safe Operating Area.

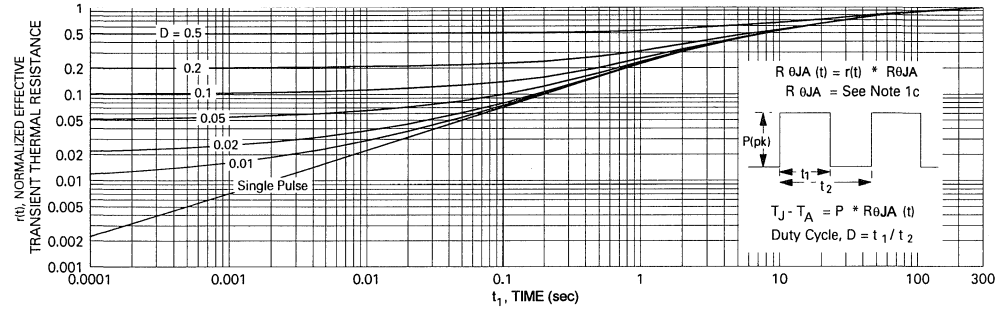


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

May 1996

NDS9958

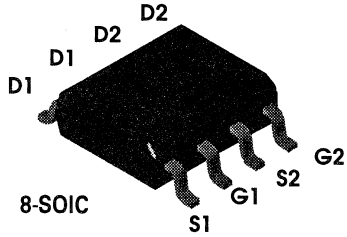
Dual N & P-Channel Enhancement Mode Field Effect Transistor

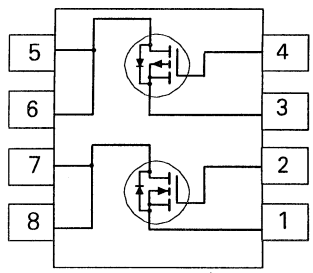
General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management, Half bridge motor control, cellular phone, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.5A, 20V, $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = 10V.
  P-Channel -3.5A , -20V, $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = -10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.





4

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage		20	-20	V
V_{GSS}	Gate-Source Voltage		± 20	± 20	V
I_D	Drain Current - Continuous T_A = 25°C	(Note 1a)	± 3.5	± 3.5	A
	- Continuous T_A = 70°C	(Note 1a)	± 2.8	± 2.8	
	- Pulsed T_A = 25°C		± 14	± 14	
P_D	Power Dissipation for Dual Operation		2		W
	Power Dissipation for Single Operation	(Note 1a)	1.6		
		(Note 1b)	1		
		(Note 1c)	0.9		
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40		°C/W

Electrical Characteristics (T_A= 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 70°C				5	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	µA
		T_J = 70°C				-5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	1	1.5	3	V
		T_J = 125°C		0.7	1.1	2.2	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-1	-2.2	-3	
		T_J = 125°C		-0.8	-1.9	-2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 3.5 A	N-Ch		0.062	0.1	Ω
		T_J = 125°C			0.085	0.14	
		V_{GS} = -10 V, I_D = -3.5 A	P-Ch		0.08	0.1	
		T_J = 125°C			0.11	0.16	
		V_{GS} = 6V, I_D = 3.0 A	N-Ch		0.073	0.12	
		V_{GS} = -6 V, I_D = -3.0 A	P-Ch		0.112	0.12	
		V_{GS} = 4.5 V, I_D = 1.0 A	N-Ch		0.08	0.15	
		V_{GS} = -4.5 V, I_D = -1.0 A	P-Ch		0.165	0.19	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	N-Ch	14			A
		V_{GS} = -10 V, V_{DS} = -5 V	P-Ch	-14			
		V_{GS} = 4.5 V, V_{DS} = 5 V	N-Ch	3.5			
		V_{GS} = -4.5 V, V_{DS} = -5 V	P-Ch	-2.5			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 3.5 A	N-Ch		7		S
		V_{DS} = -15 V, I_D = -3.5 A	P-Ch		5		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		525		pF
			P-Ch		785		
C_{oss}	Output Capacitance		N-Ch		315		pF
		P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	P-Ch		500		
C_{rss}	Reverse Transfer Capacitance		N-Ch		185		pF
			P-Ch		245		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω P-Channel V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	N-Ch		6	10	ns
			P-Ch		9	40	
t_r	Turn - On Rise Time		N-Ch		12	25	ns
			P-Ch		17	25	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		22	30	ns
			P-Ch		26	30	
t_f	Turn - Off Fall Time		N-Ch		8	20	ns
			P-Ch		13	20	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 3.5 A, V_{GS} = 10 V P-Channel V_{DS} = -10 V, I_D = -3.5 A, V_{GS} = -10 V	N-Ch		17	30	nC
			P-Ch		19	30	
Q_{gs}	Gate-Source Charge		N-Ch		1.2	6	nC
			P-Ch		3	6	
Q_{gd}	Gate-Drain Charge		N-Ch		5	12	nC
			P-Ch		9	12	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.7	A
			P-Ch			-1.7	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.7 A (Note 2)	N-Ch		0.86	1.2	V
		V_{GS} = 0 V, I_S = -1.7 A (Note 2)	P-Ch		-0.9	-1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 3.5 A, dI_F/dt = 100 A/µs	N-Ch			100	ns
			P-Ch			100	

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

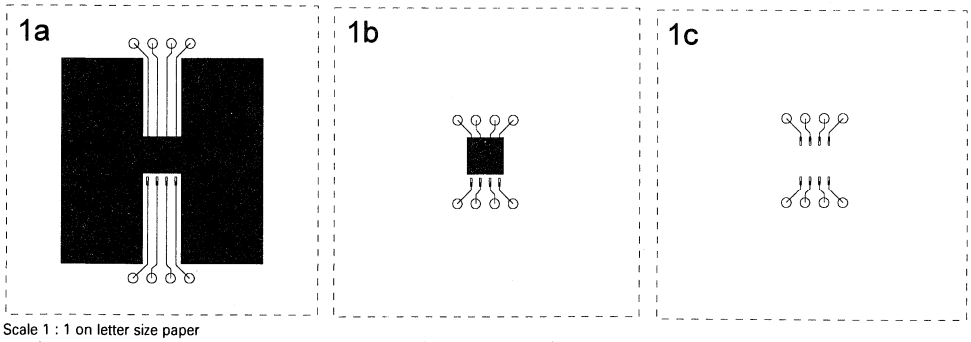
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

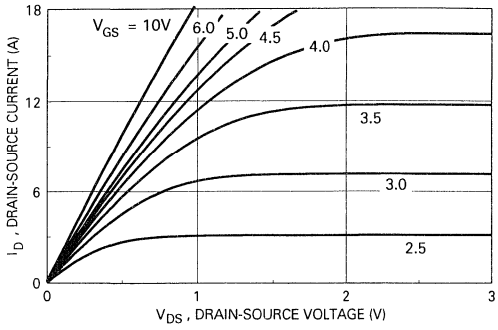


Figure 1. On-Region Characteristics.

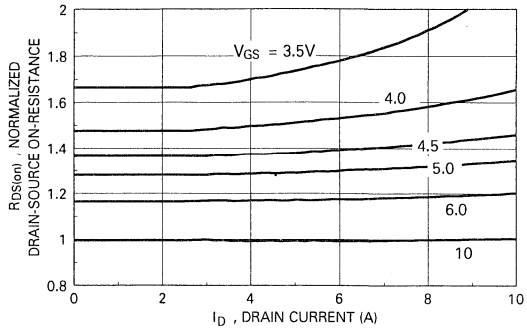


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

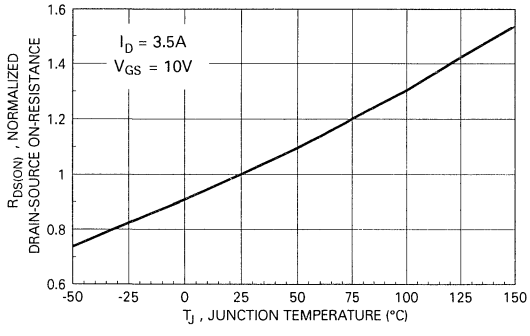


Figure 3. On-Resistance Variation with Temperature.

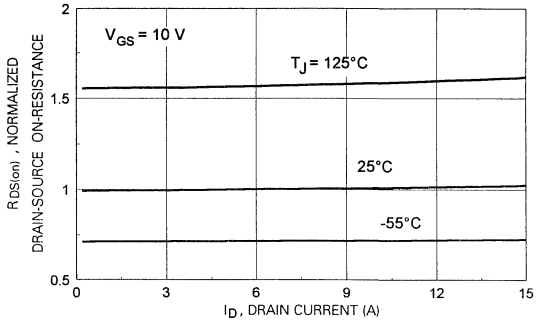


Figure 4. On-Resistance Variation with Drain Current and Temperature.

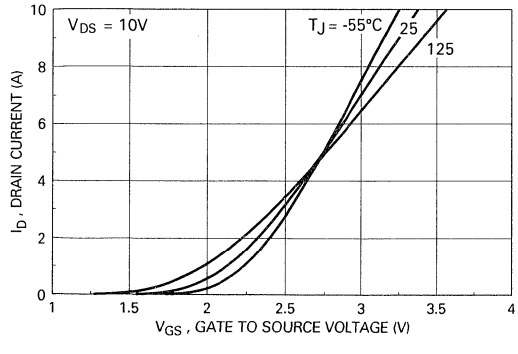


Figure 5. Transfer Characteristics.

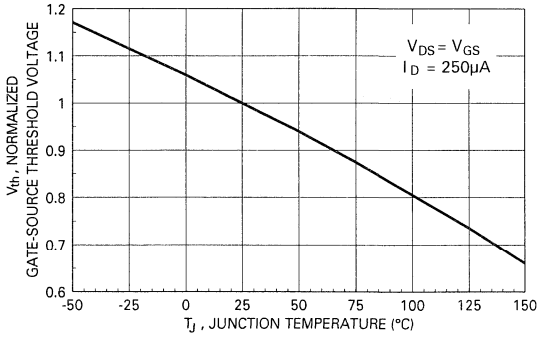


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

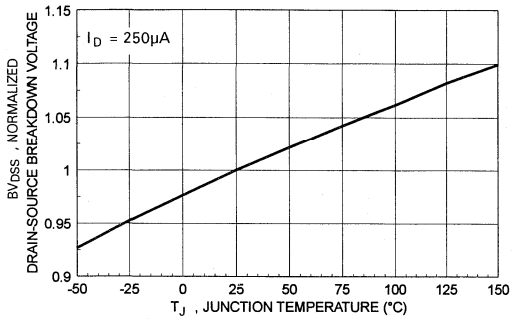


Figure 7. Breakdown Voltage Variation with Temperature.

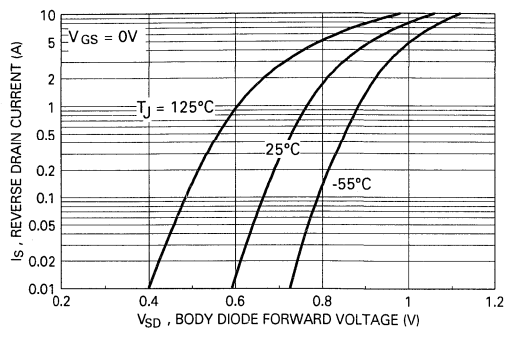


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

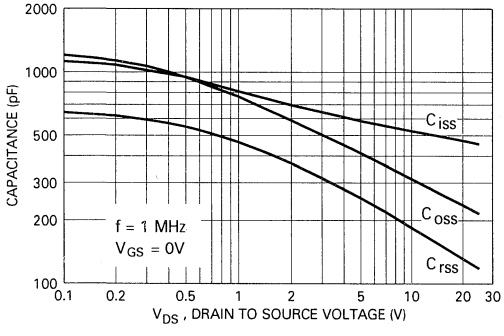


Figure 9. Capacitance Characteristics.

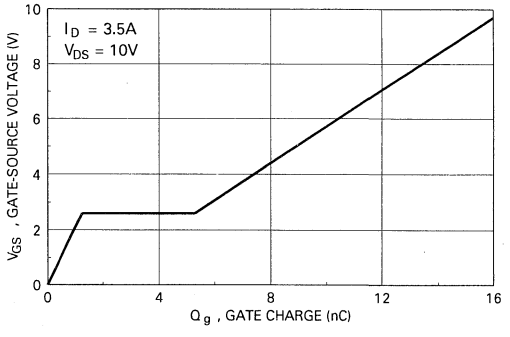


Figure 10. Gate Charge Characteristics.

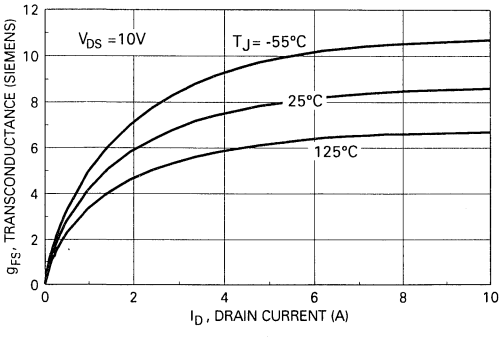


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel

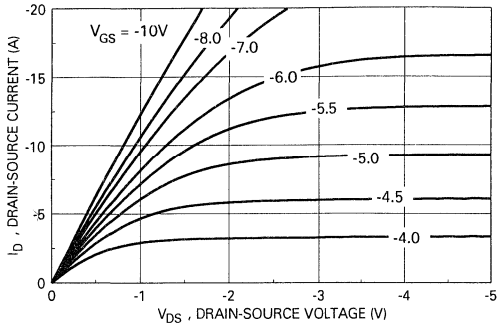


Figure 12. On-Region Characteristics.

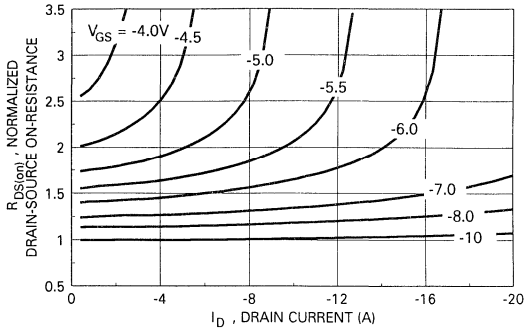


Figure 13. On-Resistance Variation with Gate Voltage and Drain Current.

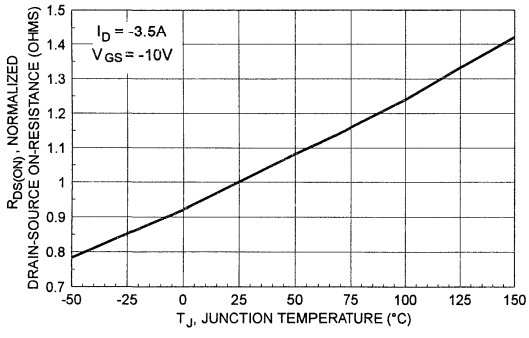


Figure 14. On-Resistance Variation with Temperature.

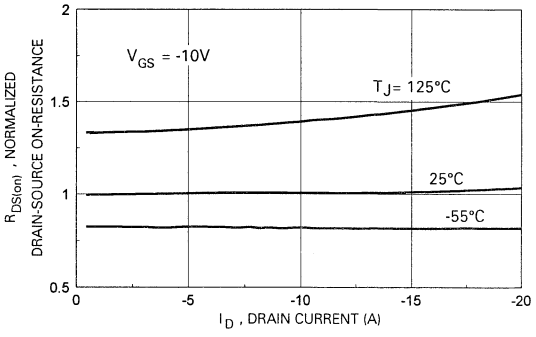


Figure 15. On-Resistance Variation with Drain Current and Temperature.

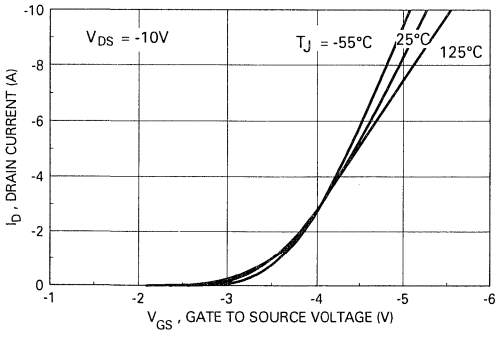


Figure 16. Drain Current Variation with Gate Voltage and Temperature.

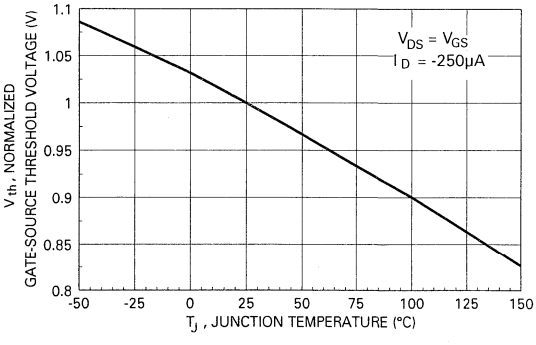


Figure 17. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

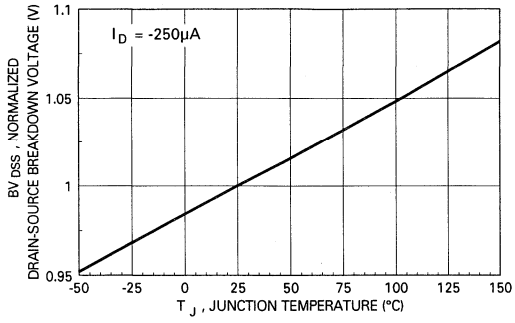


Figure 18. Breakdown Voltage Variation with Temperature.

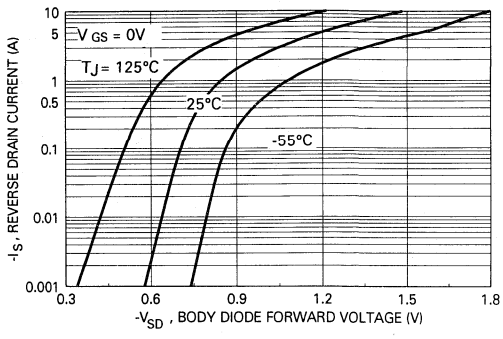


Figure 19. Body Diode Forward Voltage Variation with Current and Temperature

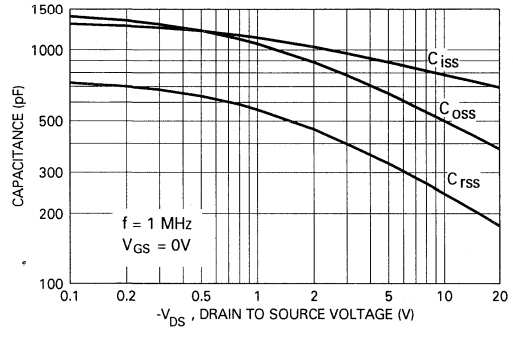


Figure 20. Capacitance Characteristics.

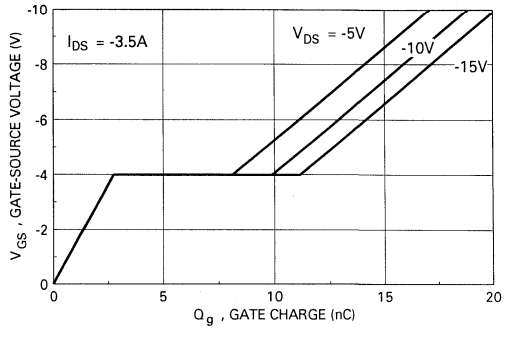


Figure 21. Gate Charge Characteristics

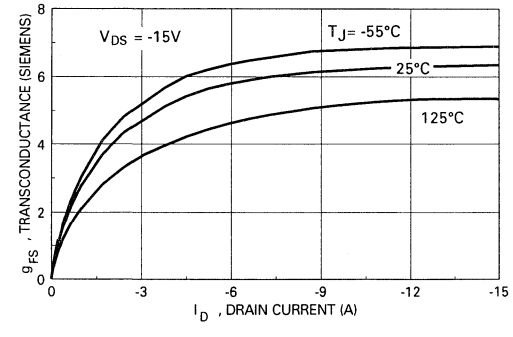


Figure 22. Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristic: N & P-Channel (continued)

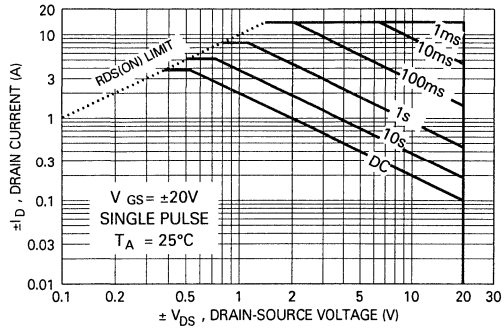


Figure 23. Maximum Safe Operating Area.

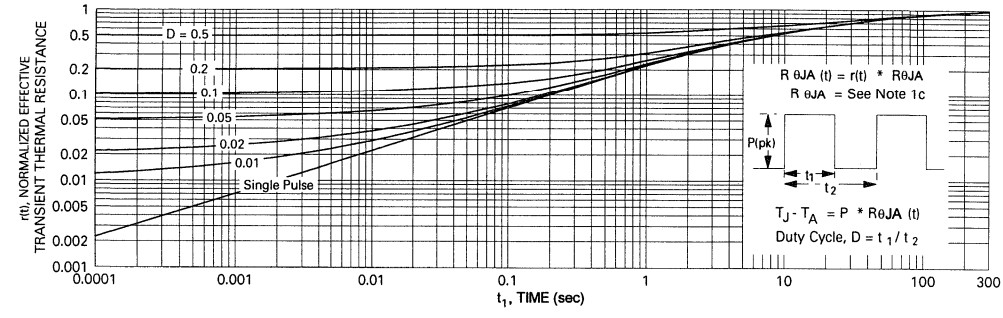


Figure 24. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

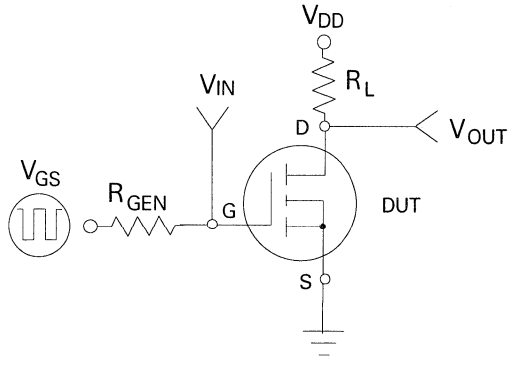


Figure 25. N or P-Channel Switching Test Circuit

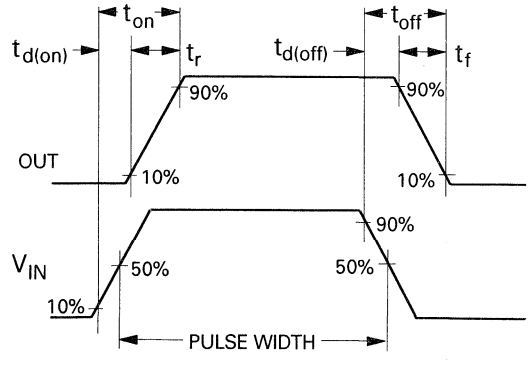


Figure 26. N or P-Channel Switching Waveforms

National Semiconductor™

May 1996

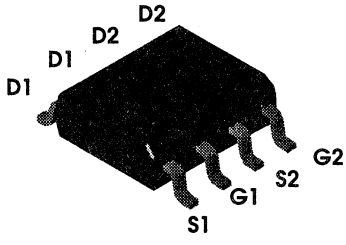
NDS9959
Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.0A, 50V. $R_{DS(ON)}$ = 0.3Ω @ V_{GS} = 10V
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual MOSFET in surface mount package.



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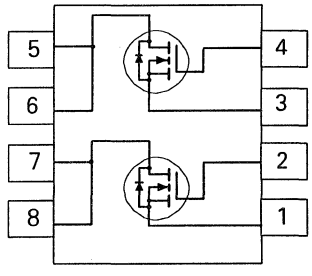


4

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDS9959	Units
V_{DSS}	Drain-Source Voltage		50	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous @ T_A = 25°C	(Note 1a)	± 2.0	A
	- Continuous @ T_A = 70°C	(Note 1a)	± 1.6	
	- Pulsed @ T_A = 25°C		± 8	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J,T_{STG}	Operating and Storage Temperature Range		-55 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			2	µA
		T_J= 55°C			25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.5 A			0.3	Ω
		V_{GS} = 5 V, I_D = 0.6 A			0.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	8			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 2.0 A	1	2.7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		152	250	pF
C_{oss}	Output Capacitance			50	85	pF
C_{rss}	Reverse Transfer Capacitance			12	25	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 0.6 A, V_{GS} = 10 V, R_L = 50 Ω, R_{GEN} = 6 Ω		4	40	ns
t_r	Turn - On Rise Time			8	70	ns
$t_{D(off)}$	Turn - Off Delay Time			9	100	ns
t_f	Turn - Off Fall Time			11	70	ns
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 1.3 A, V_{GS} = 10 V		4.3	15	nC
Q_{gs}	Gate-Source Charge			1.1		nC
Q_{gd}	Gate-Drain Charge			1.5		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				1.8	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.25 A (Note 2)		0.84	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = 1.25 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

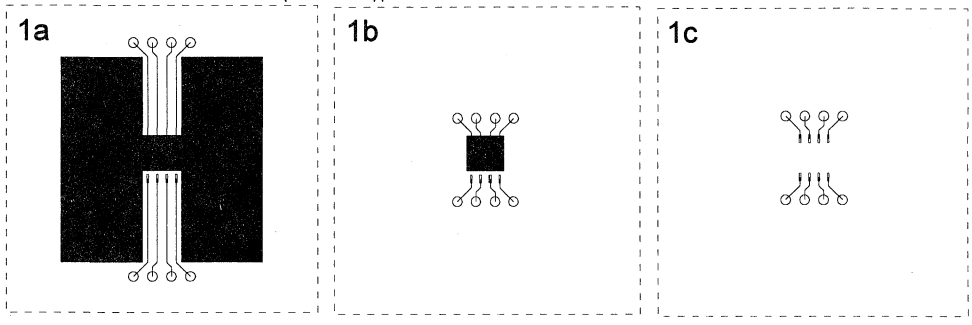
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 78°C/W when mounted on a 0.5 in² pad of 2oz copper.

b. 125°C/W when mounted on a 0.02 in² pad of 2oz copper.

c. 135°C/W when mounted on a 0.003 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

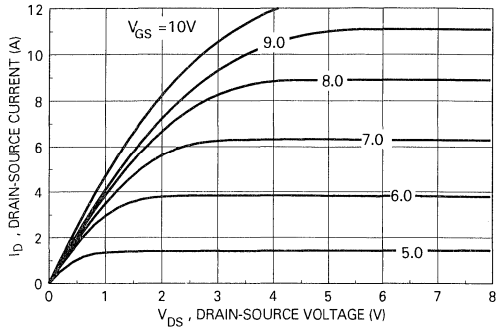


Figure 1. On-Region Characteristics.

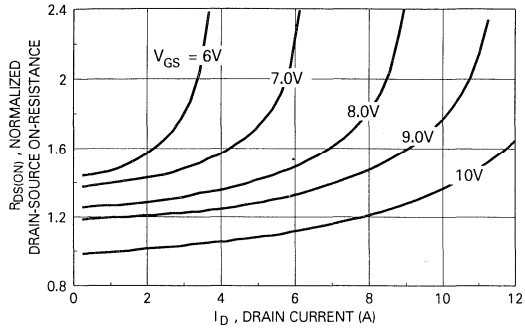


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

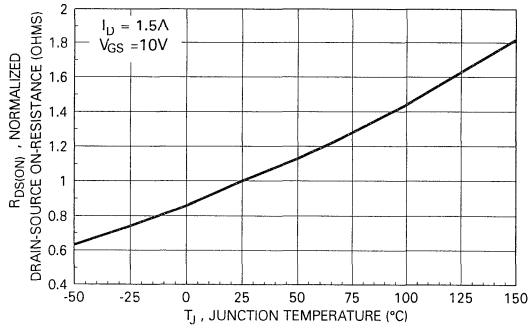


Figure 3. On-Resistance Variation with Temperature.

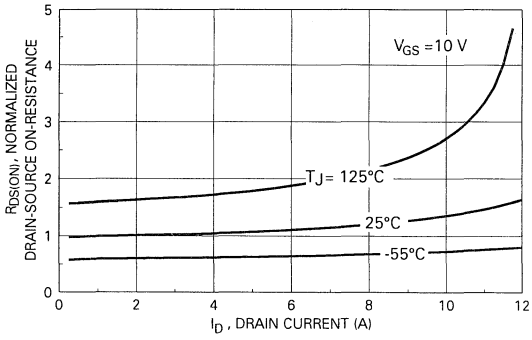


Figure 4. On-Resistance Variation with Drain Current and Temperature.

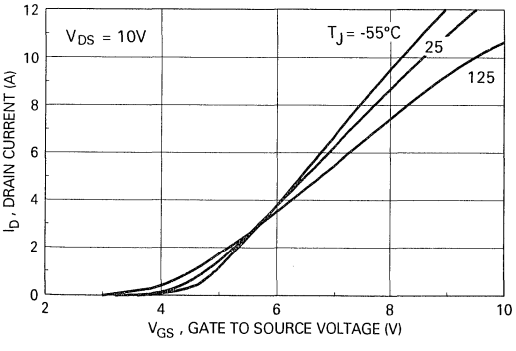


Figure 5. Transfer Characteristics.

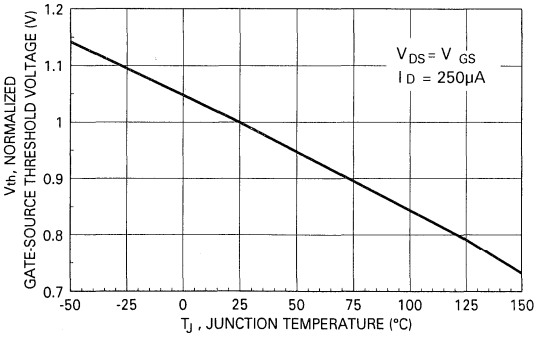


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

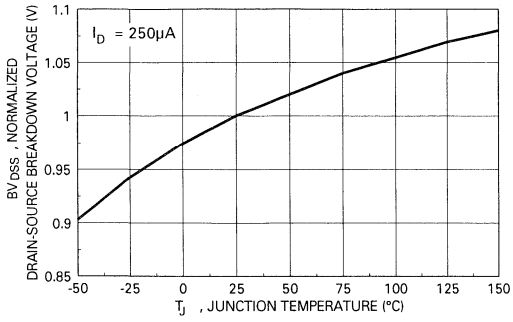


Figure 7. Breakdown Voltage Variation with Temperature.

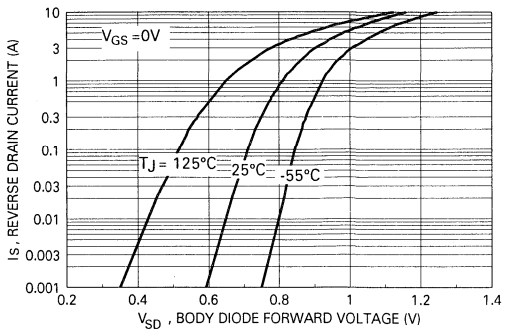


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

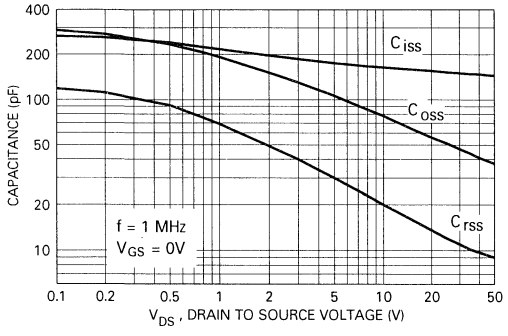


Figure 9. Capacitance Characteristics.

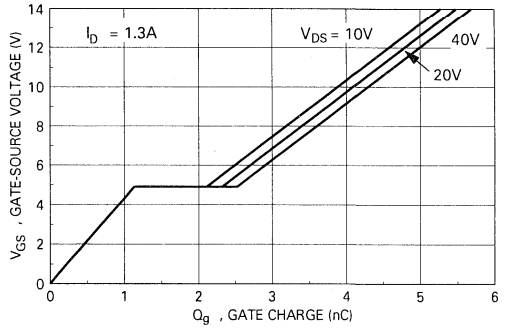


Figure 10. Gate Charge Characteristics.

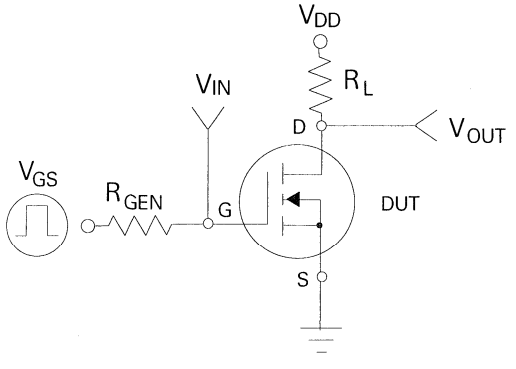


Figure 11. Switching Test Circuit

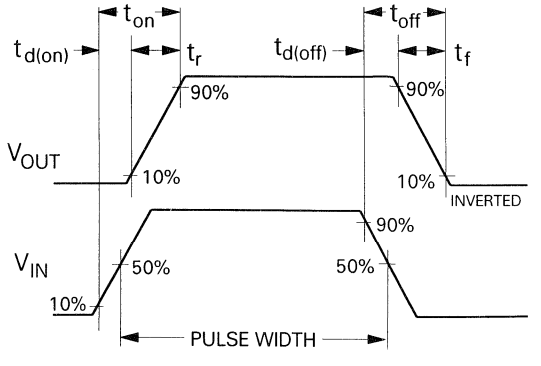


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

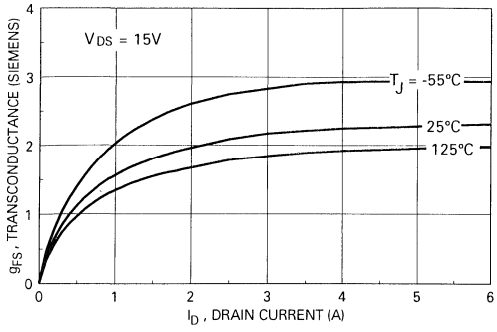


Figure 13. Transconductance Variation with Drain Current.

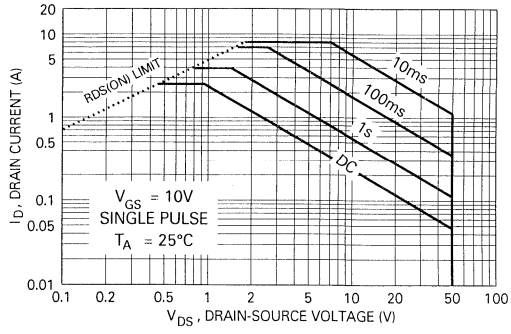


Figure 14. Maximum Safe Operating Area.

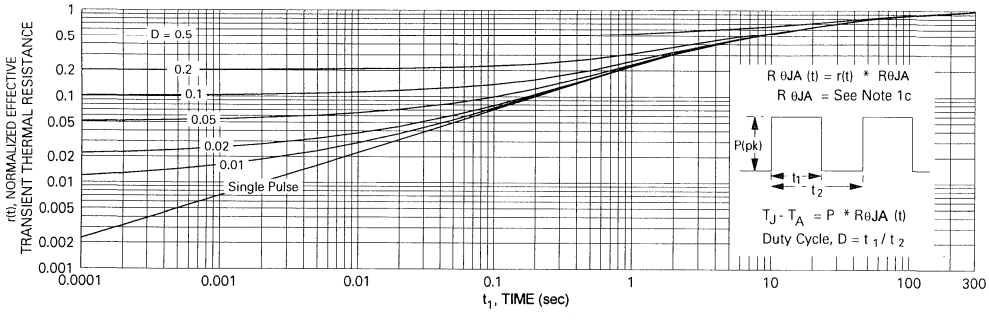


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

Section 5

SOT-223 Data Sheets

National Semiconductor™

June 1996

NDT014

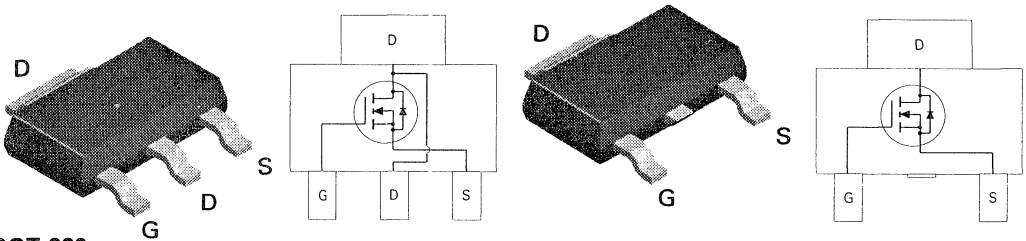
N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.7A, 60V. $R_{DS(ON)}$ = 0.2Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223

SOT-223*
(J23Z)

Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT014	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 2.7	A
	- Pulsed		± 10	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			25	µA
		V_{DS} = 48 V, V_{GS} = 0 V, T_J=125°C			250	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 1.6 A		0.18	0.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 25 V, I_D = 1.6 A		2		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		155		pF
C_{oss}	Output Capacitance			60		pF
C_{rss}	Reverse Transfer Capacitance			15		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} =30 V, I_D = 10 A, V_{GEN} = 10 V, R_{GEN} = 24 Ω		10	20	ns
t_r	Turn - On Rise Time			64	100	ns
$t_{D(off)}$	Turn - Off Delay Time			10	20	ns
t_f	Turn - Off Fall Time			10	20	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 10 A, V_{GS} = 10 V		5	11	nC
Q_{gs}	Gate-Source Charge			1.2	3.1	nC
Q_{gd}	Gate-Drain Charge			2	5.8	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.7	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				22	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.7A (Note 2)		0.95	1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 10 A, dI_F/dt = 100 A/µs			140	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

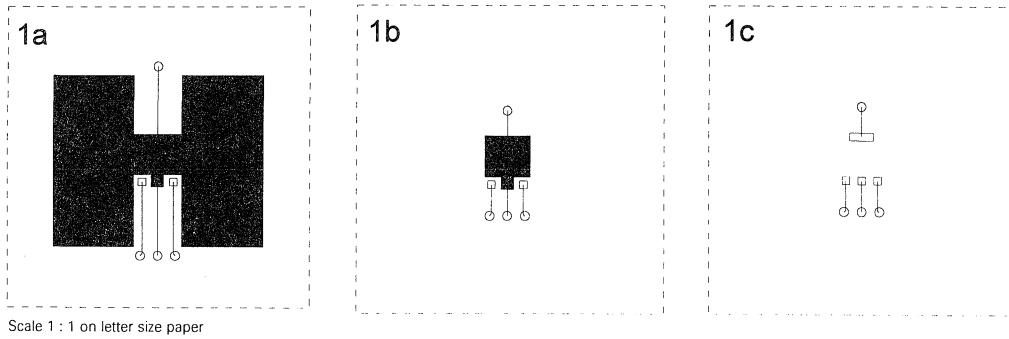
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

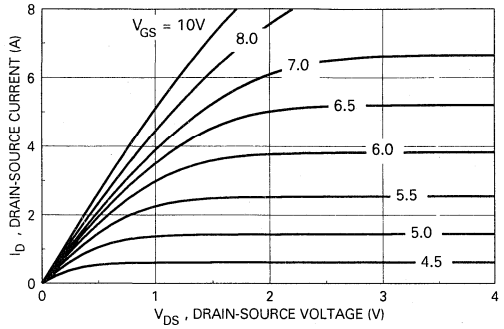


Figure 1. On-Region Characteristics

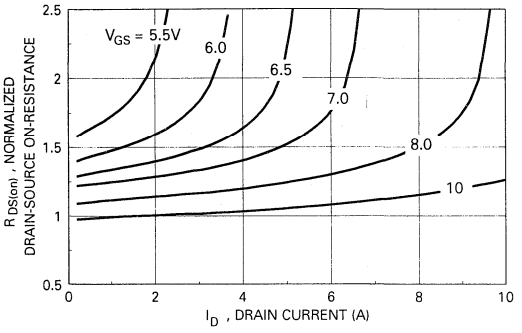


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

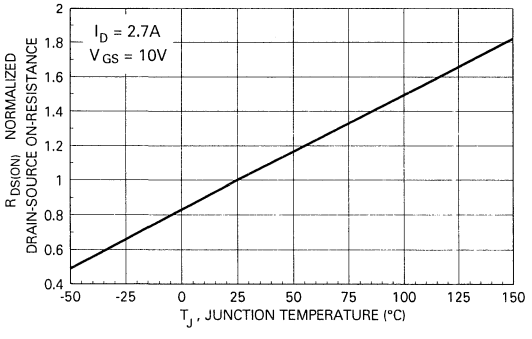


Figure 3. On-Resistance Variation with Temperature

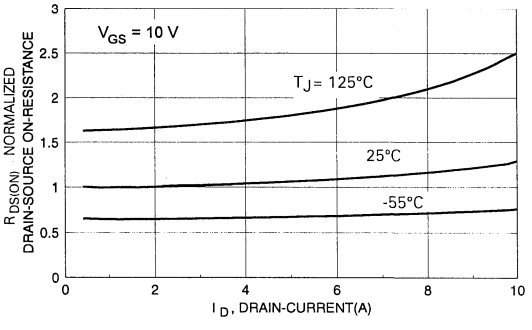


Figure 4. On-Resistance Variation with Drain Current and Temperature

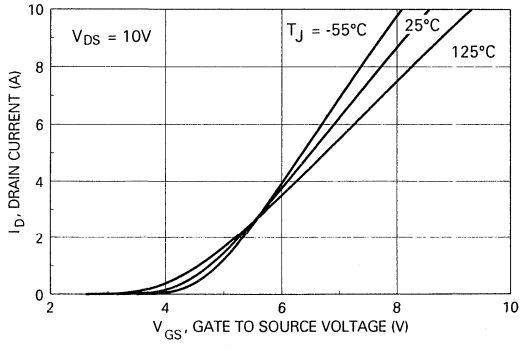


Figure 5. Transfer Characteristics

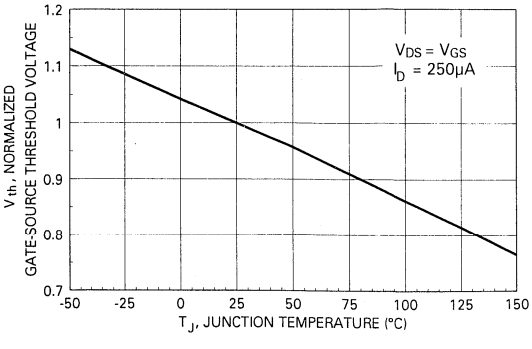


Figure 6. Gate Threshold Variation with Temperature

5

Typical Electrical Characteristics (continued)

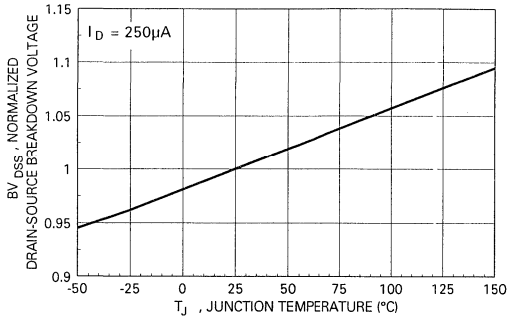


Figure 7. Breakdown Voltage Variation with Temperature

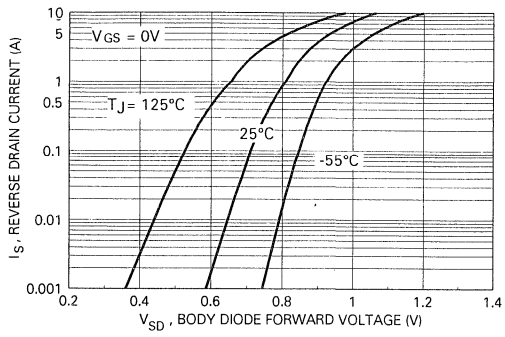


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

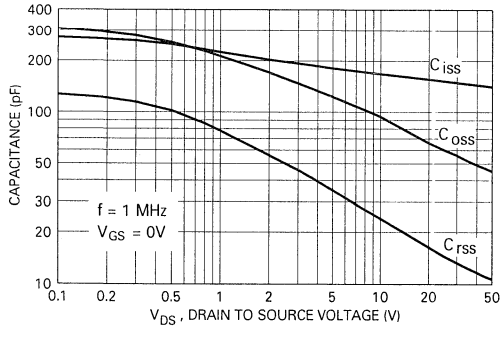


Figure 9. Capacitance Characteristics

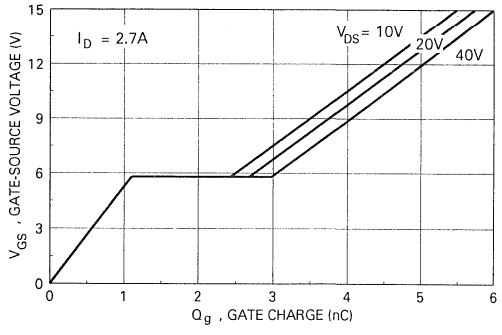


Figure 10. Gate Charge Characteristics

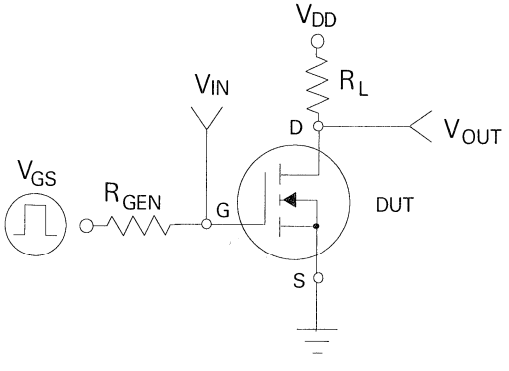


Figure 11. Switching Test Circuit

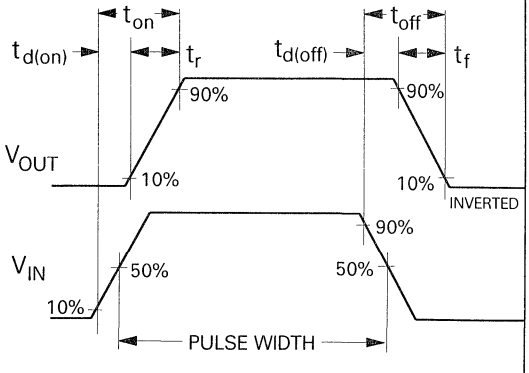


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

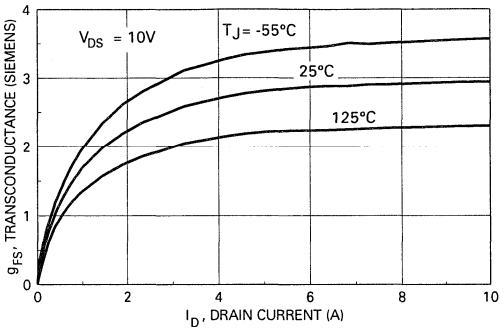


Figure 13. Transconductance Variation with Drain Current and Temperature

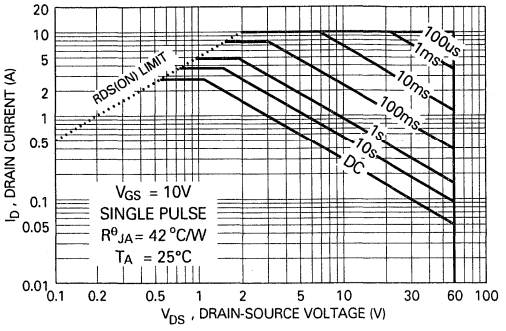


Figure 14. Maximum Safe Operating Area

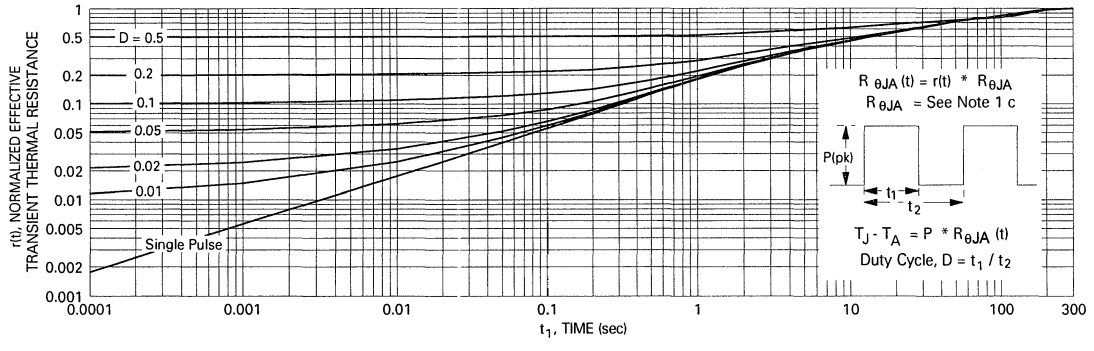


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996
PRELIMINARY

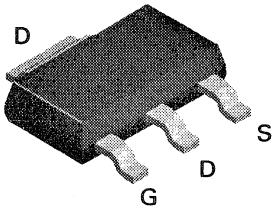
NDT014L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.6 A, 60 V. $R_{DS(ON)}$ = 0.2 Ω @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 0.16 Ω @ V_{GS} = 10 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



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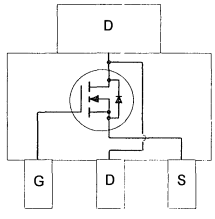
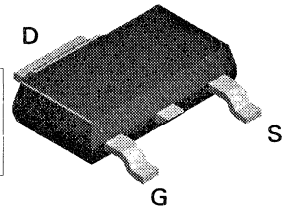
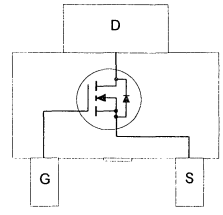






SOT-223*

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT014L	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 2.6	A
	- Pulsed		± 10	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

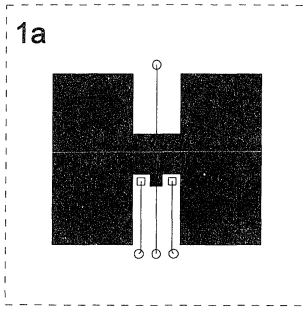
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			25	µA
		T_J = 55°C			250	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		T_J = 125°C	0.8	1.2	2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 2.6 A		0.17	0.2	Ω
		T_J = 125°C		0.25	0.36	
		V_{GS} = 10 V, I_D = 3.4 A		0.12	0.16	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	5			A
		V_{GS} = 10 V, V_{DS} = 5 V	10			
G_{FS}	Forward Transconductance	V_{GS} = 5 V, I_D = 2.6 A		4		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1.0 MHz		214		pF
C_{oss}	Output Capacitance			70		pF
C_{rss}	Reverse Transfer Capacitance			27		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 3 A, V_{GEN} = 10 V, R_{GEN} = 12 Ω		6	12	ns
t_r	Turn - On Rise Time			14	25	ns
$t_{D(off)}$	Turn - Off Delay Time			15	28	ns
t_f	Turn - Off Fall Time			10	18	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 2.6 A, V_{GS} = 4.5 V		3.6	5	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			1.4		nC

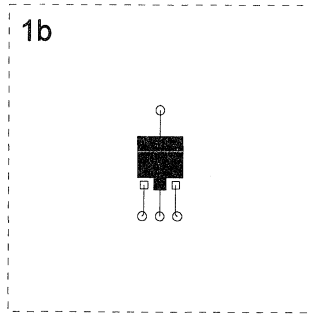
Electrical Characteristics (T_A = 25°C unless otherwise noted)

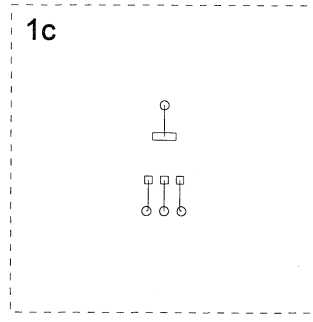
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A (Note 2)		0.85	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 2.3 A dI_F/dt = 100 A/µs			140	ns

Notes:

1. $P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$ $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is defined by users. For general reference: Applications on 4.5"x5" FR-4 PCB under still air environment, typical $R_{\theta JA}$ is found to be:
   a. 42°C/W with 1 in^2 of 2 oz copper mounting pad.
   b. 95°C/W with 0.066 in^2 of 2 oz copper mounting pad.
   c. 110°C/W with 0.0123 in^2 of 2 oz copper mounting pad.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

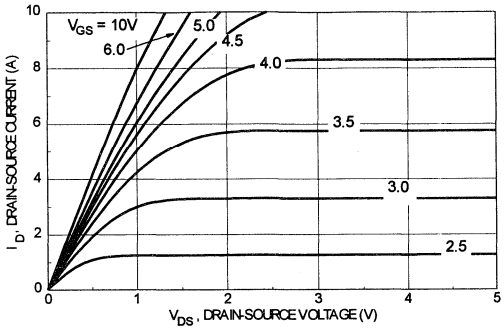


Figure 1. On-Region Characteristics.

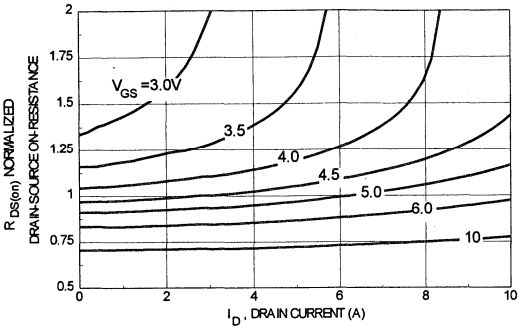


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

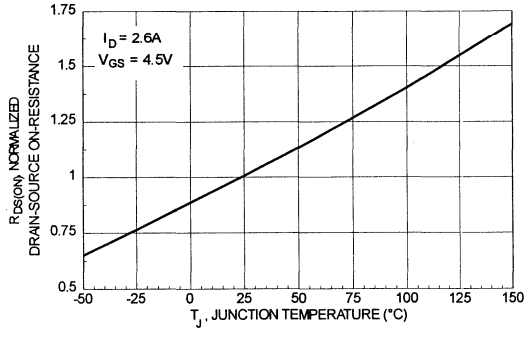


Figure 3. On-Resistance Variation with Temperature.

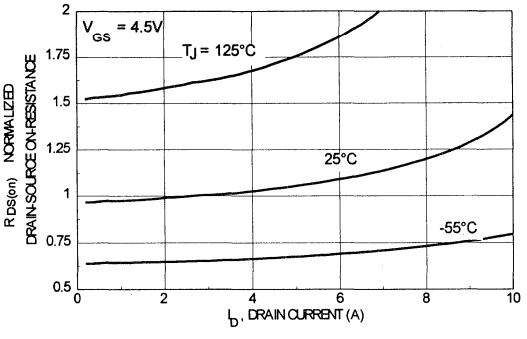


Figure 4. On-Resistance Variation with Drain Current and Temperature.

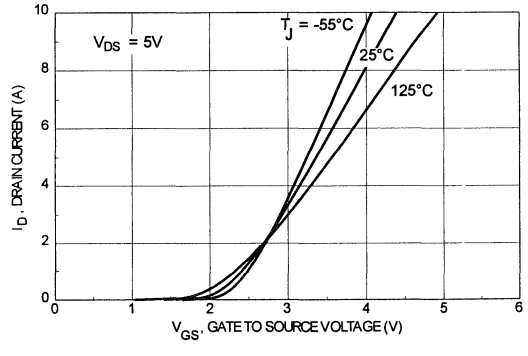


Figure 5. Transfer Characteristics.

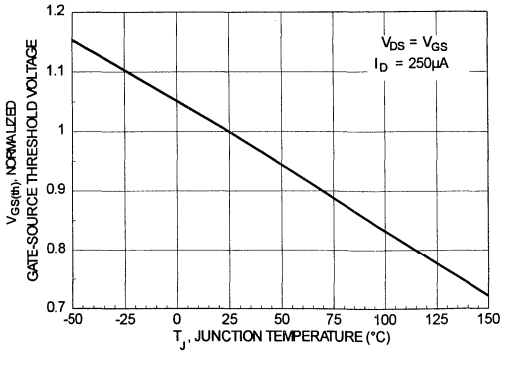


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

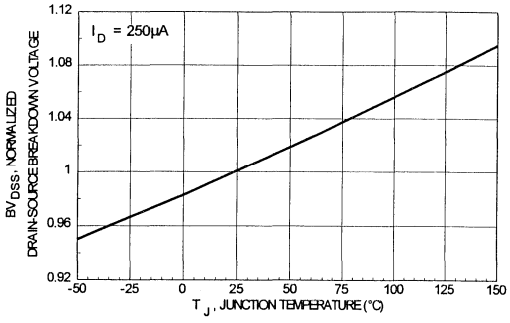


Figure 7. Breakdown Voltage Variation with Temperature.

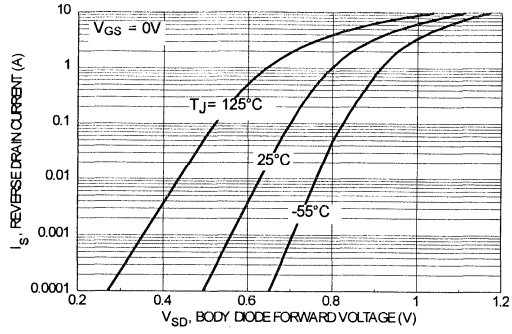


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

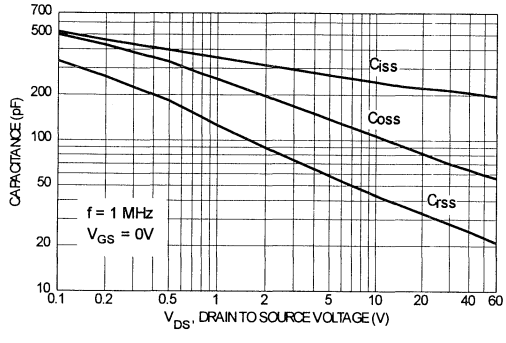


Figure 9. Capacitance Characteristics.

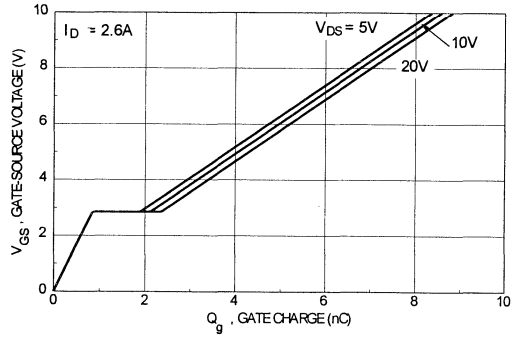


Figure 10. Gate Charge Characteristics.

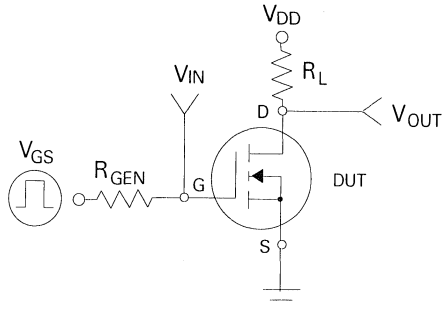


Figure 11. Switching Test Circuit

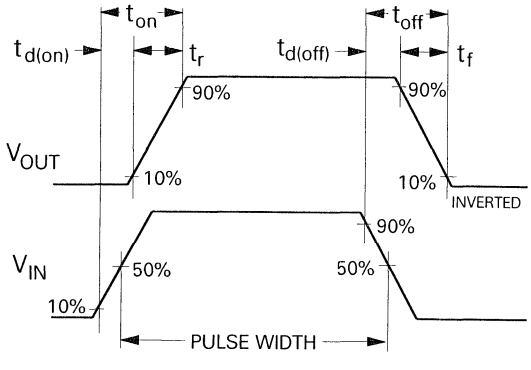


Figure 12. Switching Waveforms

Typical Thermal Characteristics

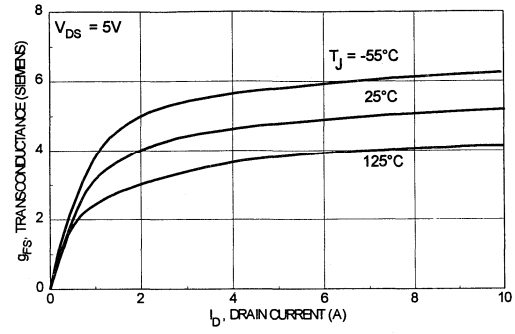


Figure 13. Transconductance Variation with Drain Current and Temperature.

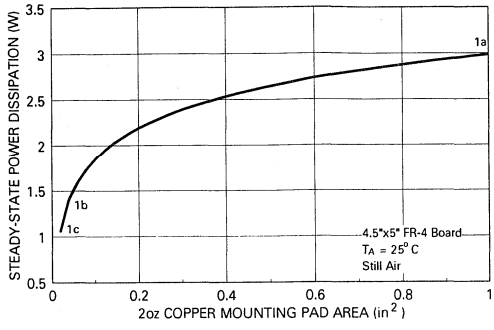


Figure 14. SOT-223 Maximum Steady- State Power Dissipation versus Copper Mounting Pad Area.

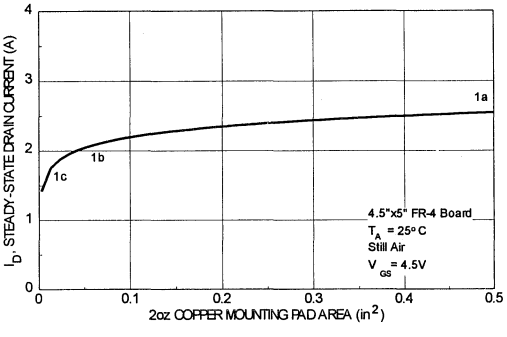


Figure 15. Maximum Steady- State Drain Current versus Copper Mounting Pad Area.

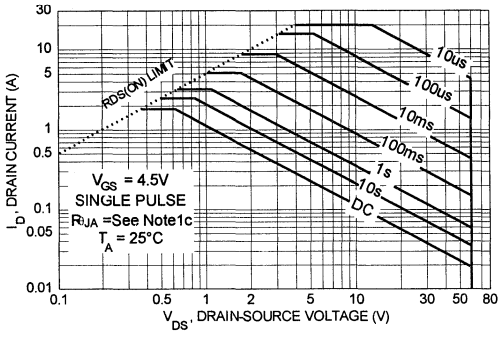


Figure 16. Maximum Safe Operating Area

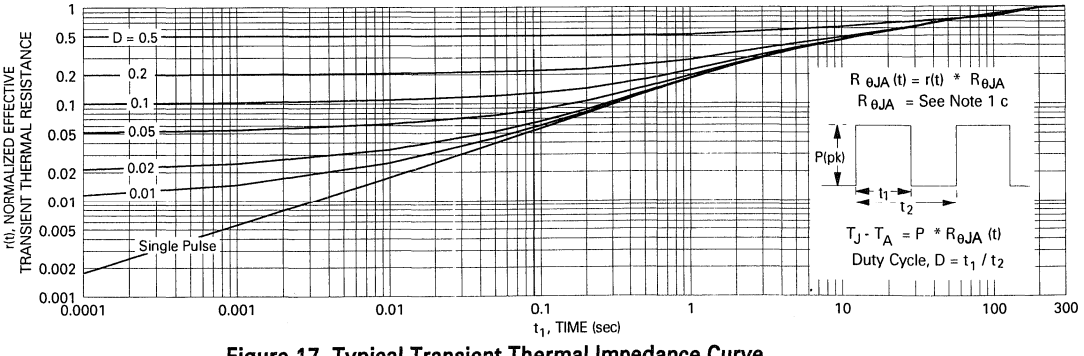


Figure 17. Typical Transient Thermal Impedance Curve.

Remark: Thermal characterization performed under the conditions of Note 1c. Should better thermal design employs, $R_{\theta JA}$ will be lower and reach thermal equivalent sooner.

National Semiconductor™

June 1996

NDT410EL

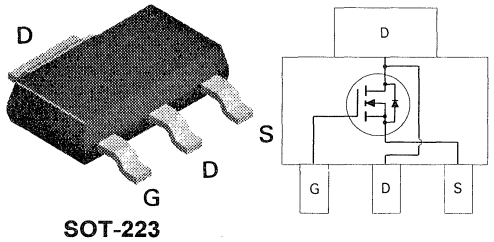
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

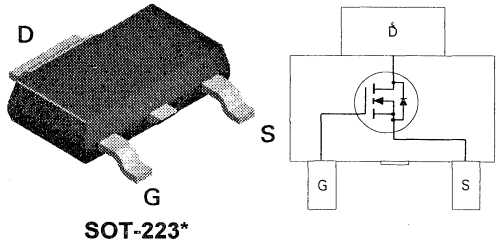
These N-Channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 2.1A 100V. $R_{DS(ON)}$ = 0.25Ω @ V_{GS} = 5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223



SOT-223*

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT410EL	Units
V_{DSS}	Drain-Source Voltage		100	V
V_{GSS}	Gate-Source Voltage		20	V
I_D	Drain Current - Continuous	(Note 1a)	2.1	A
	- Pulsed		10	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 2)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 50 V, I_D = 10A			15	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				10	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	2	V
		T_J = 125°C	0.65	1.1	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 2.1 A		0.2	0.25	Ω
		T_J = 125°C		0.37	0.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 5 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 2.1 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		528		pF
C_{oss}	Output Capacitance			85		pF
C_{rss}	Reverse Transfer Capacitance			20		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 50 V, I_D = 2.1 A, V_{GEN} = 5 V, R_{GEN} = 25 Ω		9	20	ns
t_r	Turn - On Rise Time			72	120	ns
$t_{D(off)}$	Turn - Off Delay Time			49	80	ns
t_f	Turn - Off Fall Time			47	80	ns
Q_g	Total Gate Charge	V_{DS} = 80 V, I_D = 2.1 A, V_{GS} = 5 V		10	16	nC
Q_{gs}	Gate-Source Charge			1.5		nC
Q_{gd}	Gate-Drain Charge			5.6		nC

5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A (Note 2)			1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2.3 A, dI_F/dt = 100A/µs			150	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

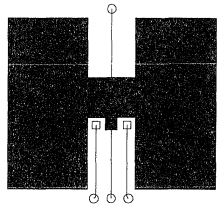
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

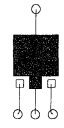
b. 95°C/W when mounted on a 0.04 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.006 in^2 pad of 2oz copper.

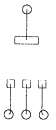
1a



1b



1c



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

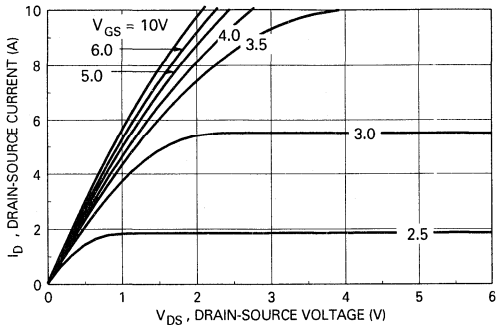


Figure 1. On-Region Characteristics.

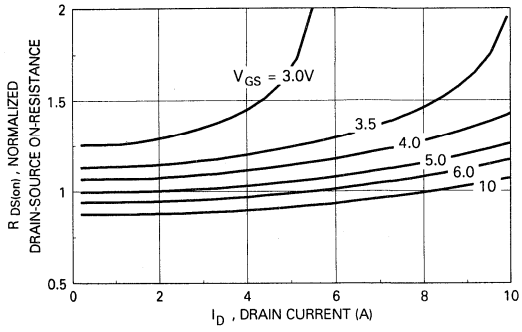


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

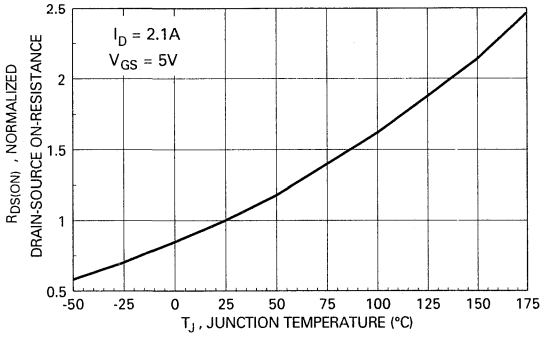


Figure 3. On-Resistance Variation with Temperature.

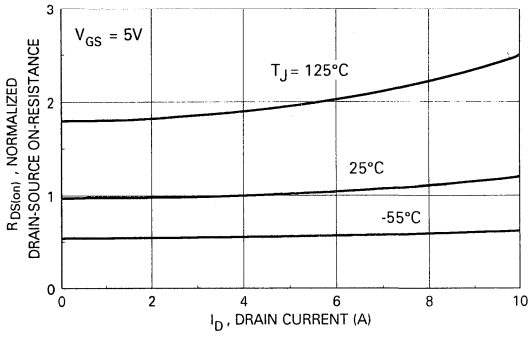


Figure 4. On-Resistance Variation with Drain Current and Temperature.

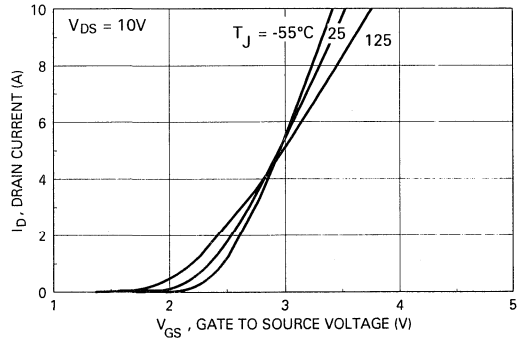


Figure 5. Transfer Characteristics.

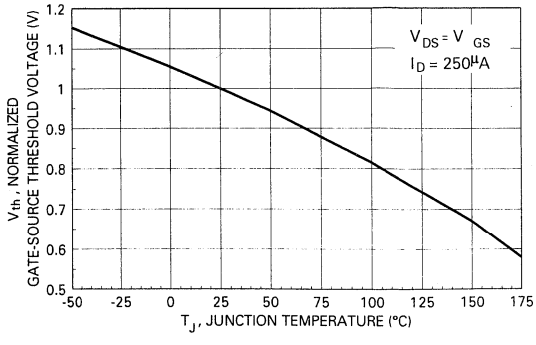


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

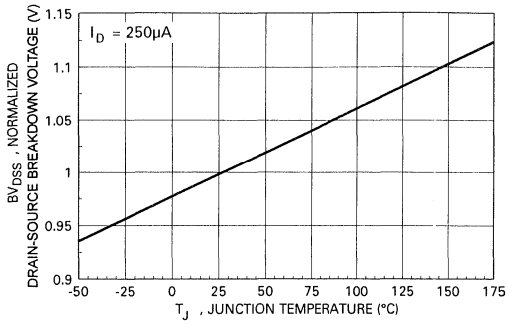


Figure 7. Breakdown Voltage Variation with Temperature.

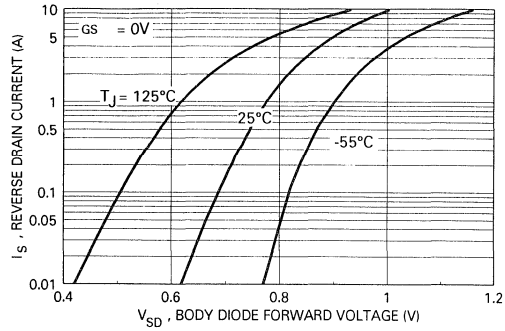


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

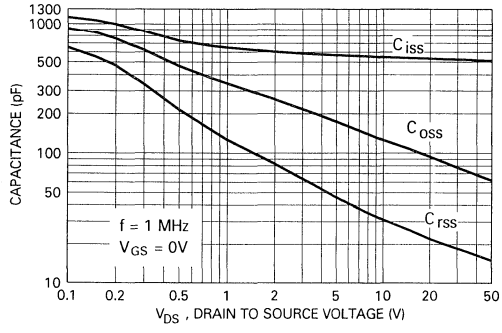


Figure 9. Capacitance Characteristics.

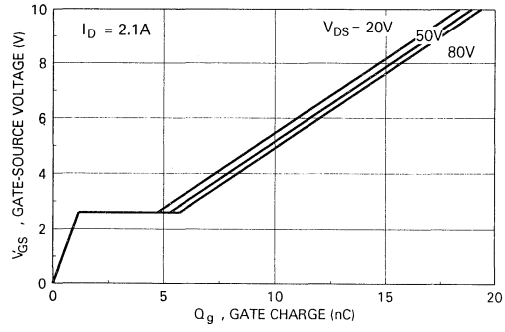


Figure 10. Gate Charge Characteristics.

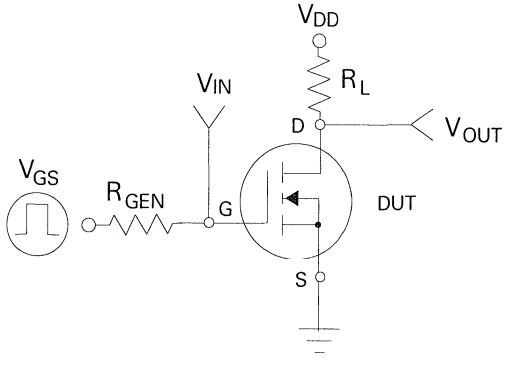


Figure 11. Switching Test Circuit

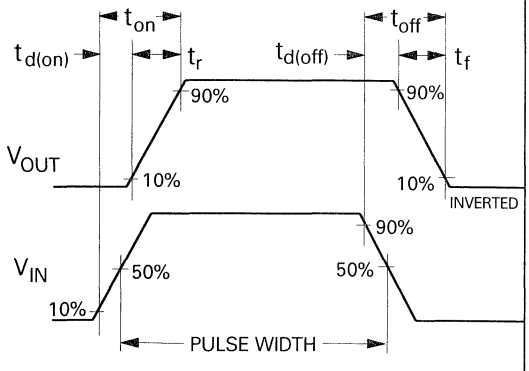


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics

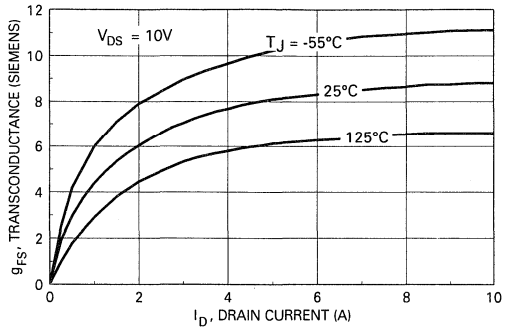


Figure 13. Transconductance Variation with Drain Current and Temperature.

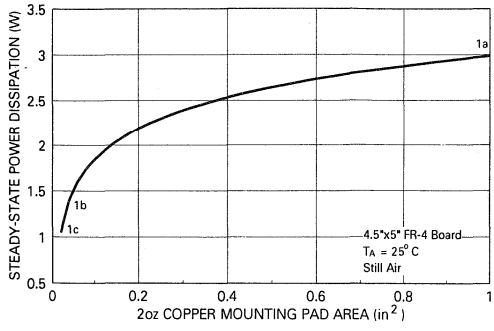


Figure 14. SOT-223 Maximum Steady- State Power Dissipation versus Copper Mounting Pad Area.

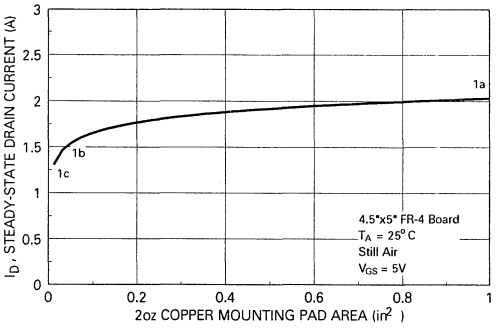


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

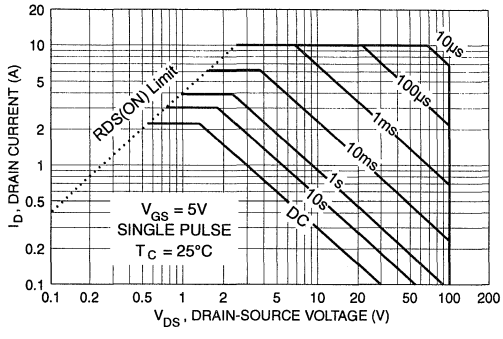


Figure 16. Maximum Safe Operating Area.

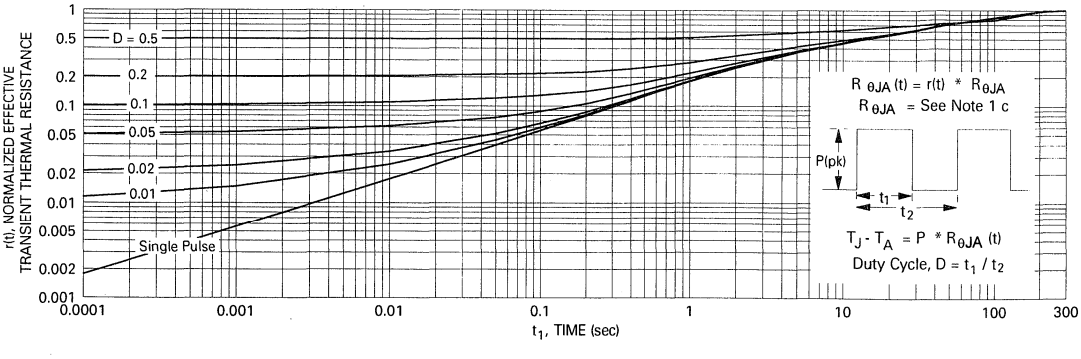


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

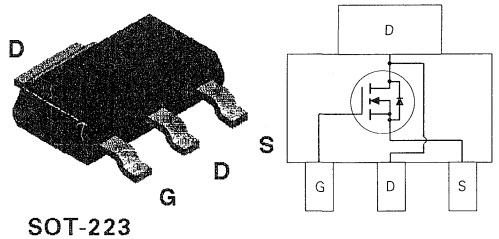
NDT451AN
N-Channel Enhancement Mode Field Effect Transistor

General Description

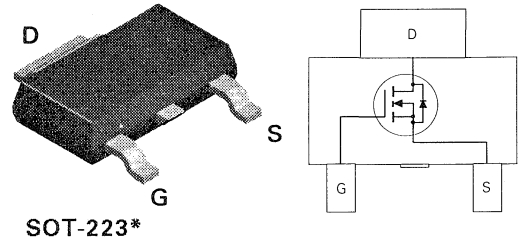
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 7.2A, 30V. $R_{DS(ON)}$ = 0.035Ω @ V_{GS} = 10V
  $R_{DS(ON)}$ = 0.05Ω @ V_{GS} = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223



SOT-223*
(J23Z)

Absolute Maximum Ratings

T_A= 25°C unless otherwise noted

Symbol	Parameter		NDT451AN	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 7.2	A
	- Pulsed		± 25	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	3	V
		T_J = 125°C	0.7	1.2	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.2 A		0.03	0.035	Ω
		T_J = 125°C		0.042	0.063	
		V_{GS} = 4.5 V, I_D = 6.0 A		0.042	0.05	
		T_J = 125°C		0.058	0.09	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	25			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	15			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.2 A		11		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		720		pF
C_{oss}	Output Capacitance			370		pF
C_{rss}	Reverse Transfer Capacitance			250		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		12	20	ns
t_r	Turn - On Rise Time			13	30	ns
$t_{D(off)}$	Turn - Off Delay Time			29	50	ns
t_f	Turn - Off Fall Time			10	20	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 7.2 A, V_{GS} = 10 V		19	30	nC
Q_{gs}	Gate-Source Charge			2.3		nC
Q_{gd}	Gate-Drain Charge			5.5		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.2A (Note 2)		0.9	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 1.25 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

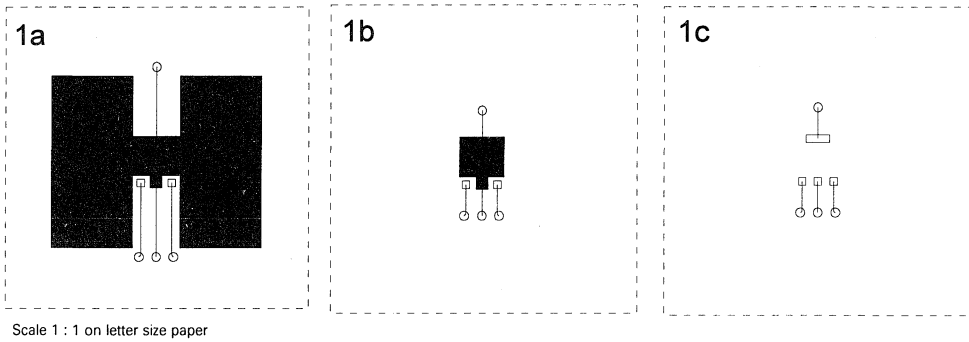
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 in² pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in² pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in² pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

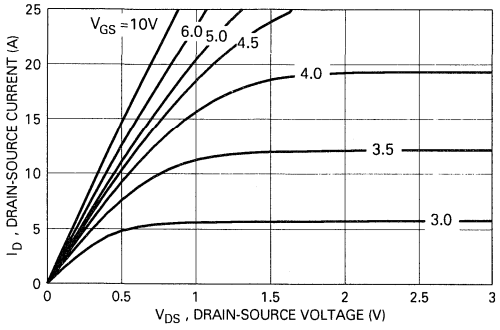


Figure 1. On-Region Characteristics.

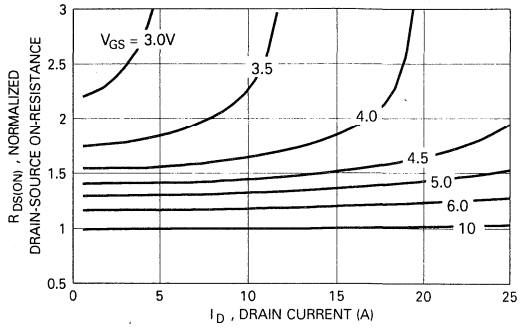


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

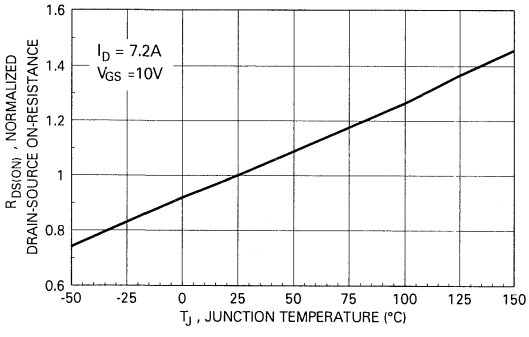


Figure 3. On-Resistance Variation with Temperature.

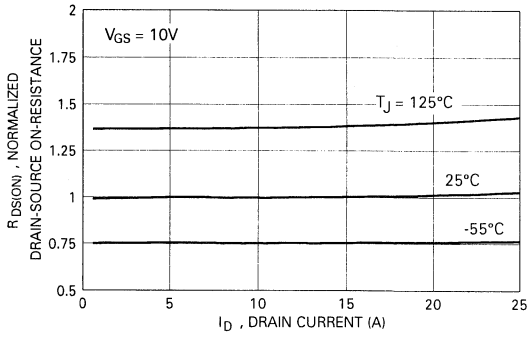


Figure 4. On-Resistance Variation with Drain Current and Temperature.

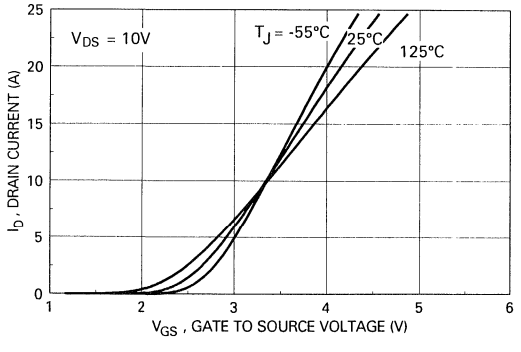


Figure 5. Transfer Characteristics.

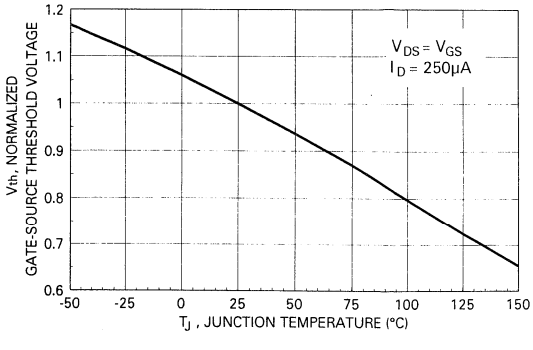


Figure 6. Gate Threshold Variation with Temperature.

5

Typical Electrical Characteristics

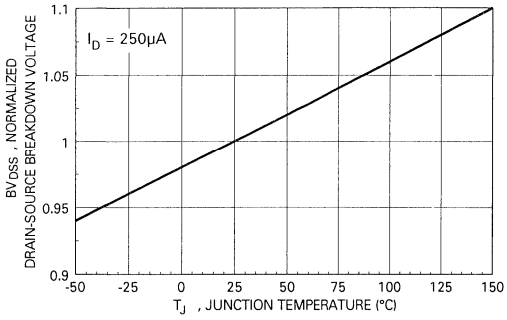


Figure 7. Breakdown Voltage Variation with Temperature.

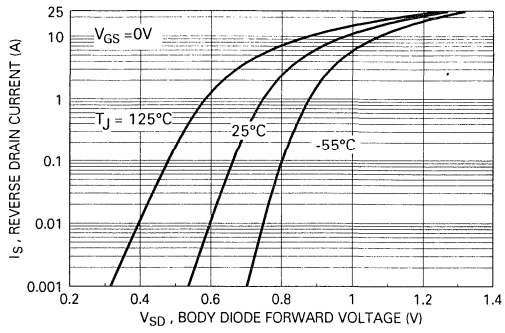


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

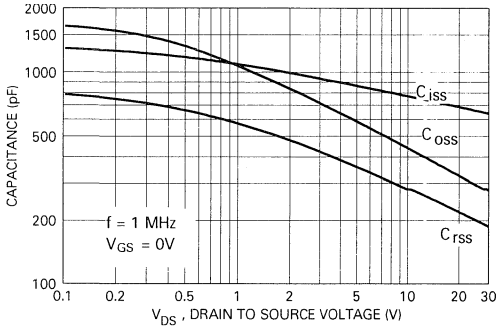


Figure 9. Capacitance Characteristics.

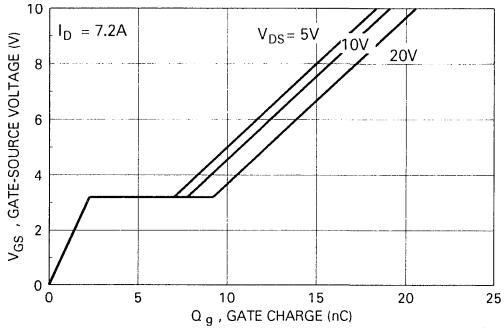


Figure 10. Gate Charge Characteristics.

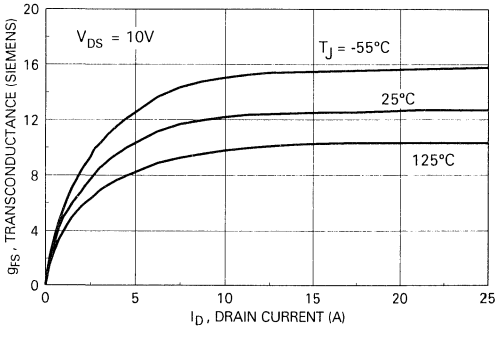


Figure 11. Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics

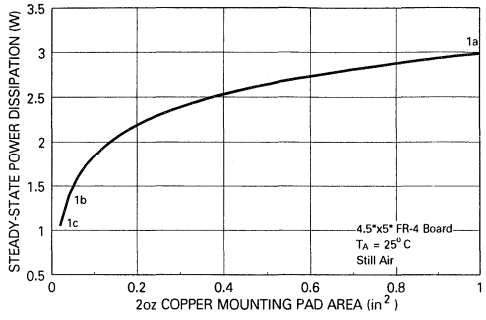


Figure 12. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

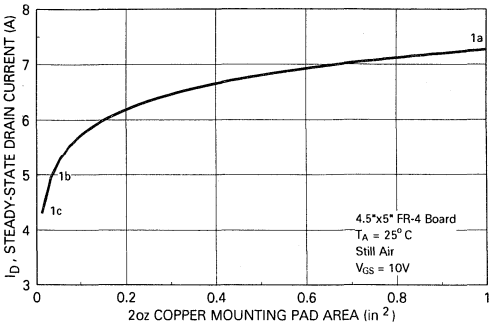


Figure 13. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

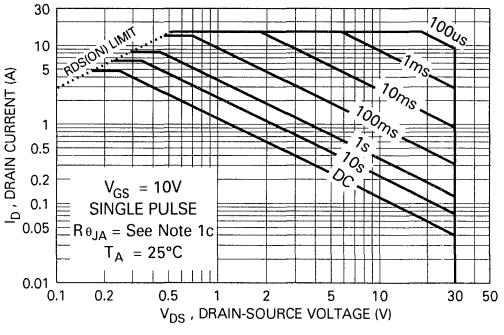


Figure 14. Maximum Safe Operating Area.

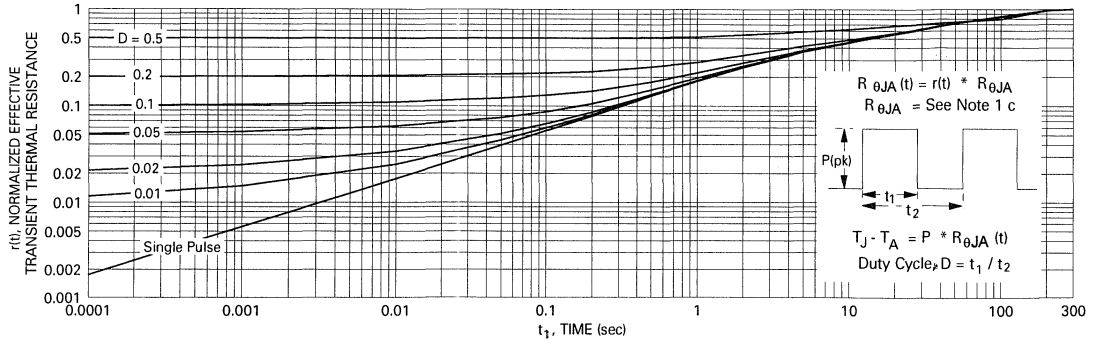


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

5

National Semiconductor™

June 1996

NDT451N

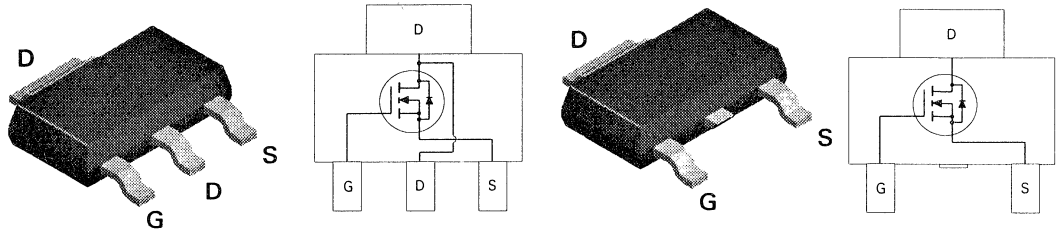
N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 5.5A, 30V. $R_{DS(ON)}$ = 0.05Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223 **SOT-223* (J23Z)**

Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT451N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 5.5	A
	- Pulsed		± 25	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			2	µA
		T_J = 55°C			20	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	3	V
		T_J = 125°C	0.7	1.2	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 5.5 A		0.042	0.05	Ω
		T_J = 125°C		0.065	0.1	
		V_{GS} = 4.5 V, I_D = 4.3 A		0.064	0.08	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	18			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	15			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.5 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		730		pF
C_{oss}	Output Capacitance			370		pF
C_{rss}	Reverse Transfer Capacitance			140		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 1.0 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		20	30	ns
t_r	Turn - On Rise Time			15	25	ns
$t_{D(off)}$	Turn - Off Delay Time			19	40	ns
t_f	Turn - Off Fall Time			10	30	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 5.5 A, V_{GS} = 10 V		16	25	nC
Q_{gs}	Gate-Source Charge			1.8	3	nC
Q_{gd}	Gate-Drain Charge			4.5	7	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 5.5 A (Note 2)		0.8	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

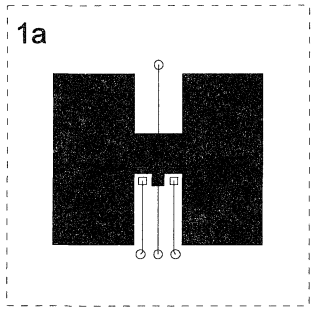
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

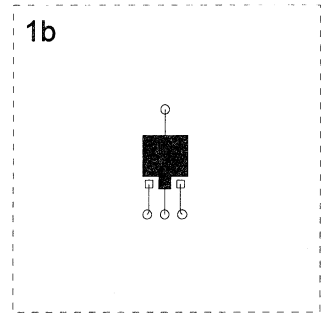
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

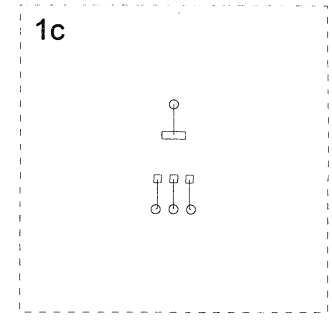
a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

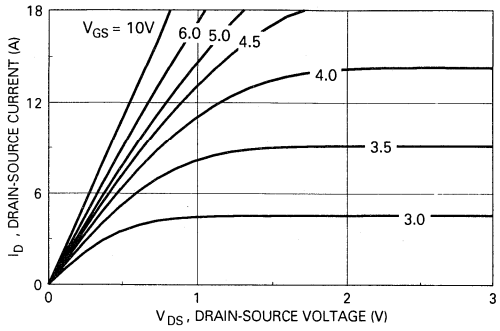


Figure 1. On-Region Characteristics

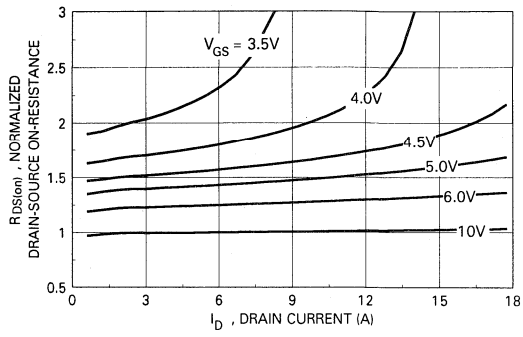


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

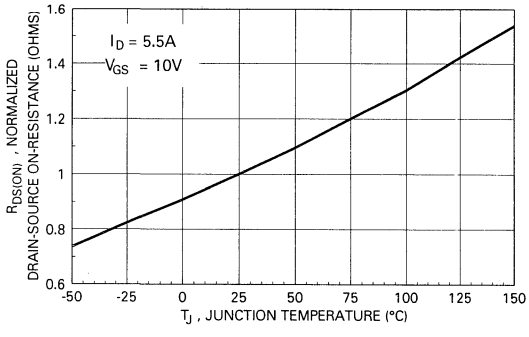


Figure 3. On-Resistance Variation with Temperature

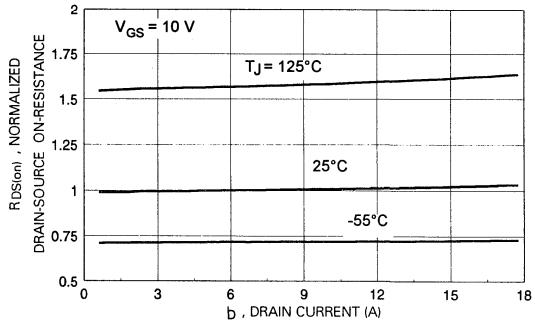


Figure 4. On-Resistance Variation with Drain Current and Temperature

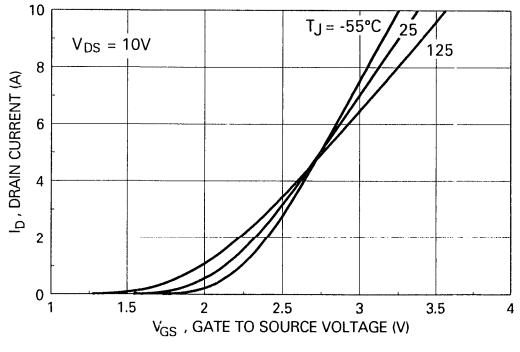


Figure 5. Transfer Characteristics

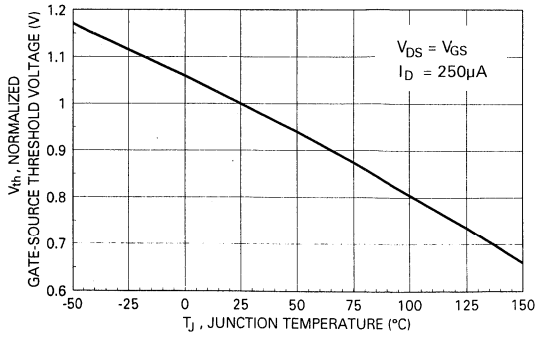


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

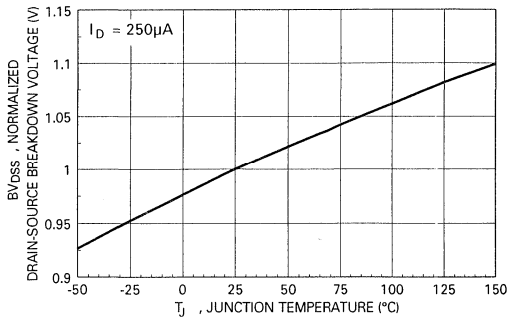


Figure 7. Breakdown Voltage Variation with Temperature

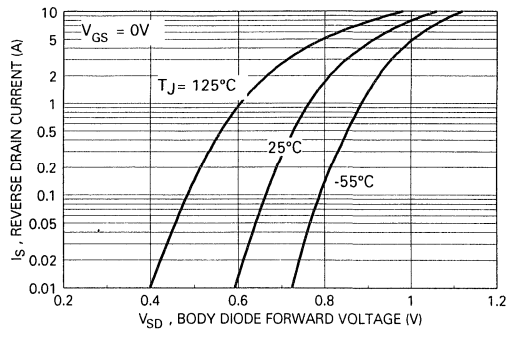


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

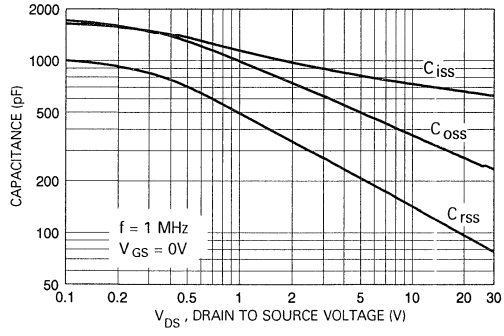


Figure 9. Capacitance Characteristics

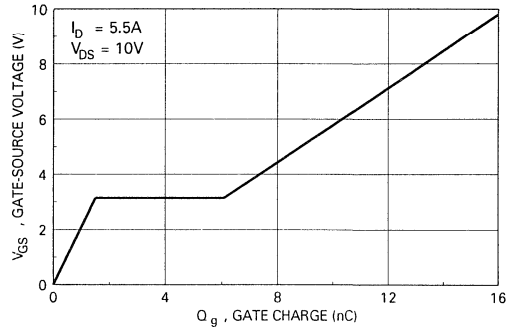


Figure 10. Gate Charge Characteristics

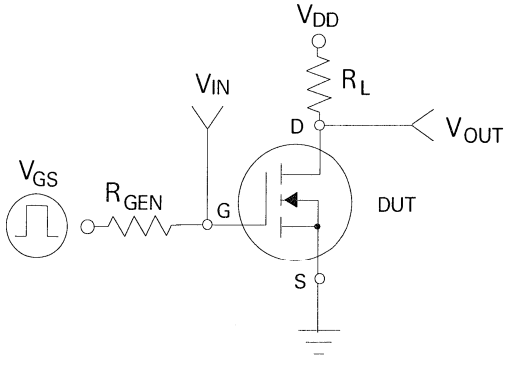


Figure 11. Switching Test Circuit

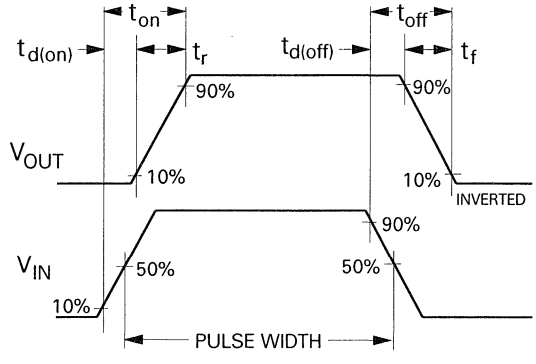


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

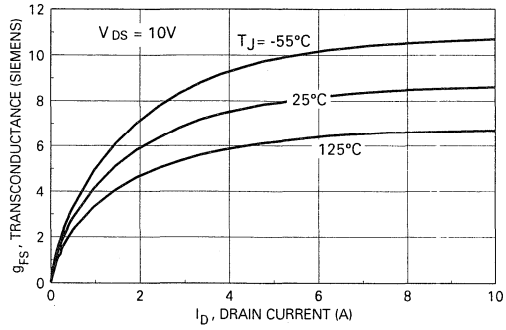


Figure 13. Transconductance Variation with Drain Current and Temperature

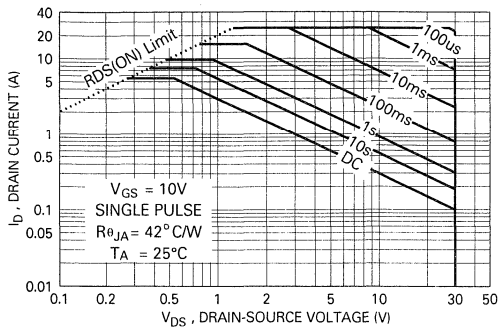


Figure 14. Maximum Safe Operating Area

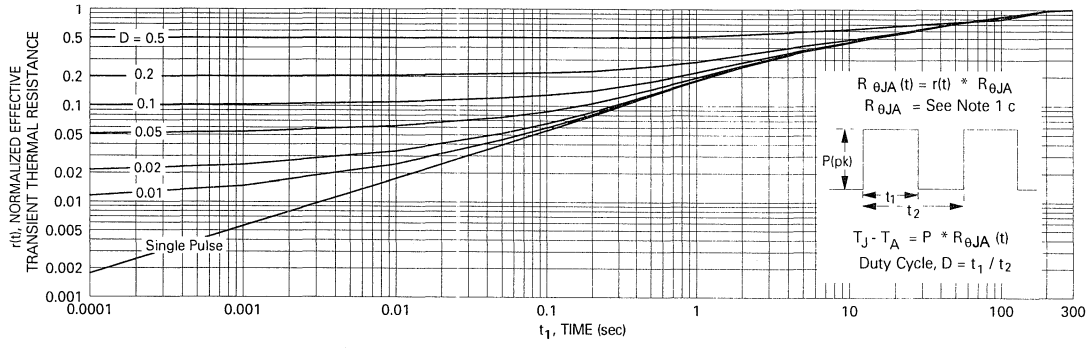


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

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National Semiconductor™

June 1996

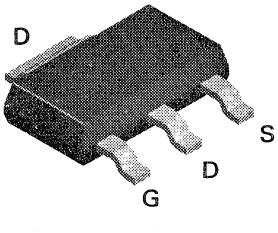
NDT452AP
P-Channel Enhancement Mode Field Effect Transistor

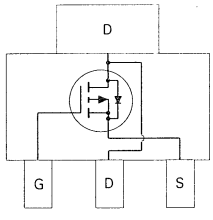
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and DC motor control.

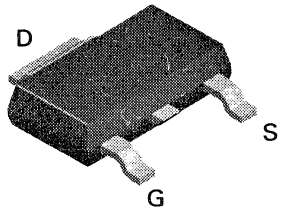
Features

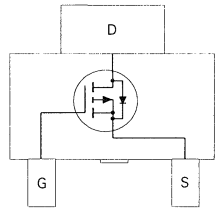
- -5A, -30V. $R_{DS(ON)}$ = 0.065Ω @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = -4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





SOT-223





SOT-223*
(J23Z)

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT452AP	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		-20	V
I_D	Drain Current - Continuous	(Note 1a)	-5	A
	- Pulsed		-15	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J,T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-1.6	-2.8	V
		T_J = 125°C	-0.7	-1.2	-2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.0 A		0.052	0.065	Ω
		T_J = 125°C		0.075	0.13	
		V_{GS} = -4.5 V, I_D = -4.3 A		0.085	0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-5			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -5.0 A		7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		690		pF
C_{oss}	Output Capacitance			430		pF
C_{rss}	Reverse Transfer Capacitance			160		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		9	20	ns
t_r	Turn - On Rise Time			20	30	ns
$t_{D(off)}$	Turn - Off Delay Time			40	50	ns
t_f	Turn - Off Fall Time			19	40	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -5.0 A, V_{GS} = -10 V		22	30	nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			5.2		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.5 A (Note 2)		-0.85	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = -2.5 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

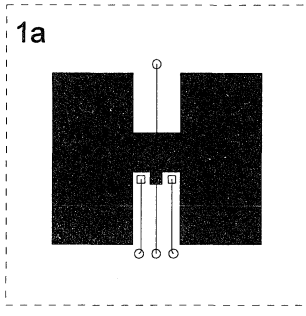
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

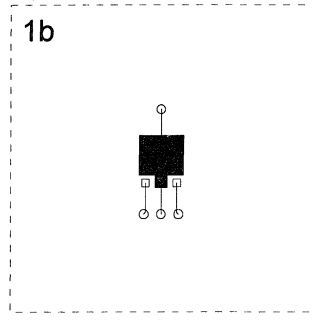
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

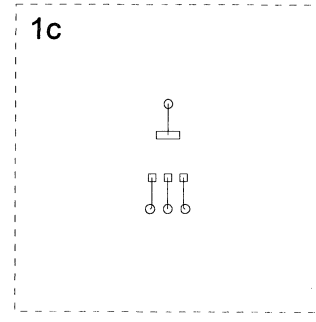
a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

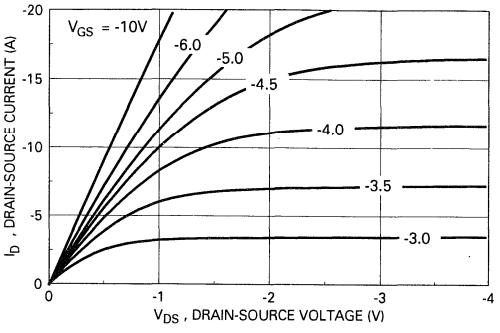


Figure 1. On-Region Characteristics.

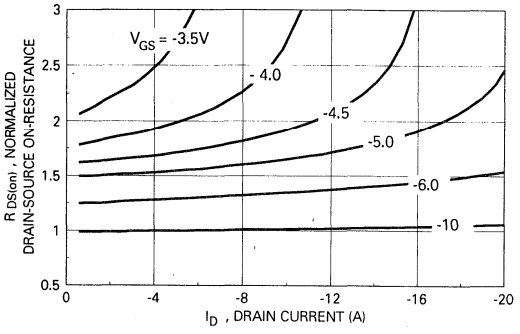


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

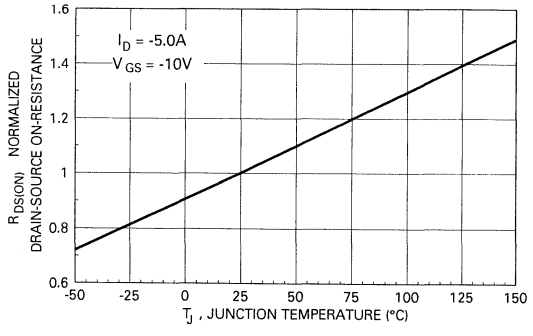


Figure 3. On-Resistance Variation with Temperature.

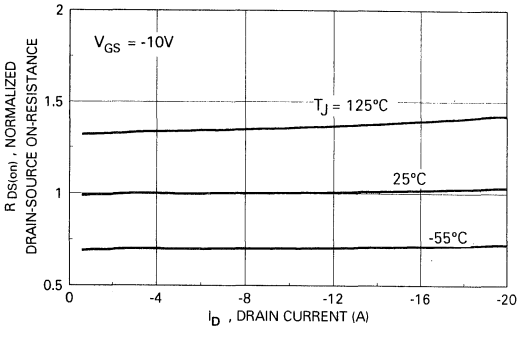


Figure 4. On-Resistance Variation with Drain Current and Temperature.

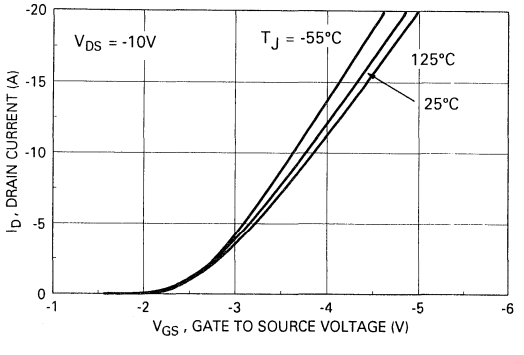


Figure 5. Transfer Characteristics.

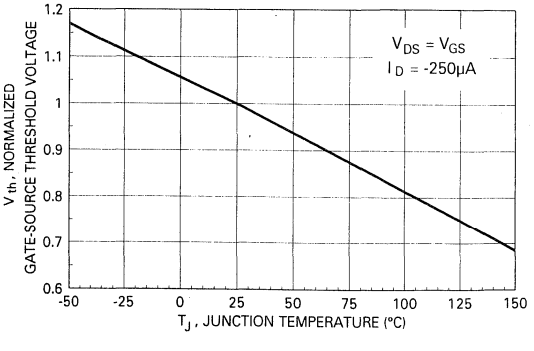


Figure 6. Gate Threshold Variation with Temperature.

5

Typical Electrical Characteristics

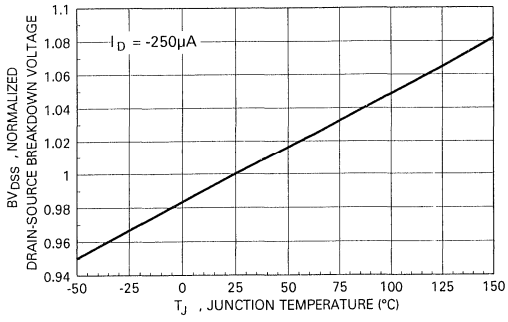


Figure 7. Breakdown Voltage Variation with Temperature.

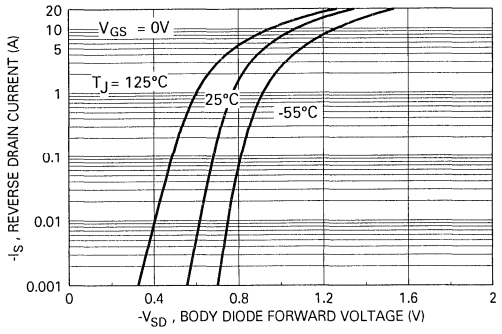


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

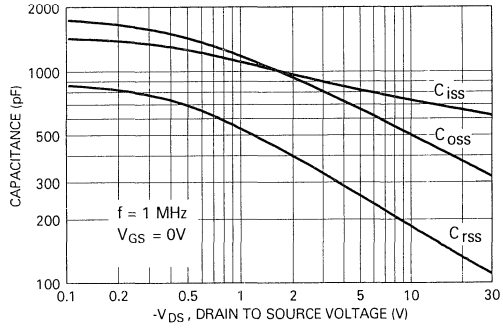


Figure 9. Capacitance Characteristics.

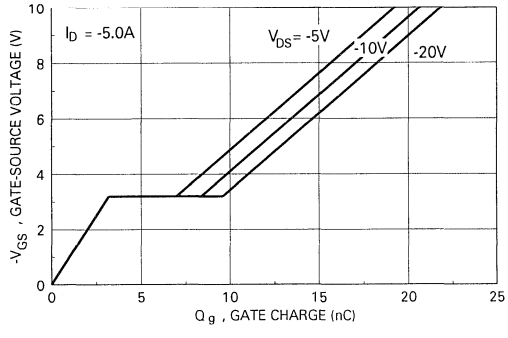


Figure 10. Gate Charge Characteristics.

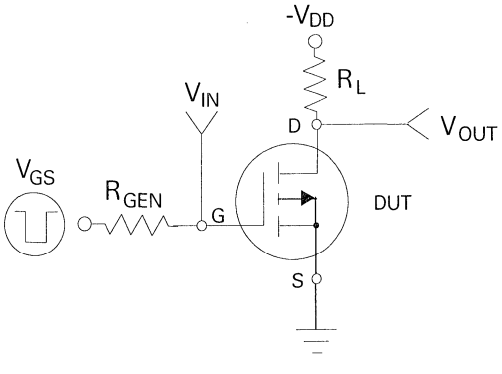


Figure 11. Switching Test Circuit

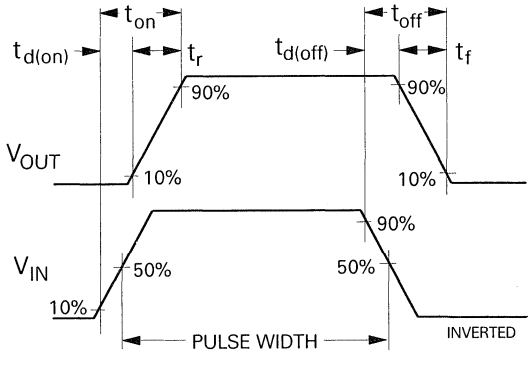


Figure 12. Switching Waveforms

Typical Thermal Characteristics

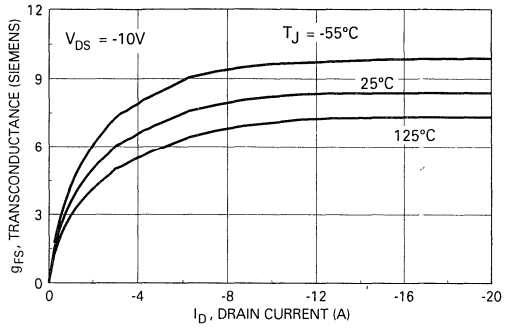


Figure 13. Transconductance Variation with Drain Current and Temperature.

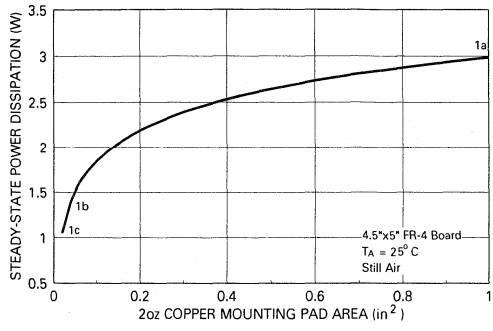


Figure 14. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

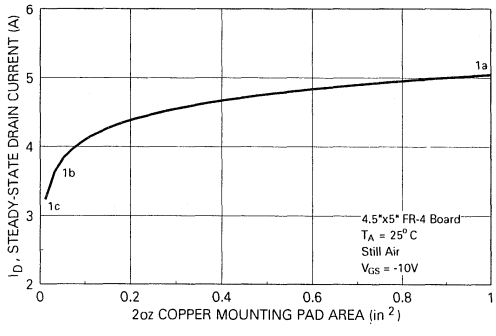


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

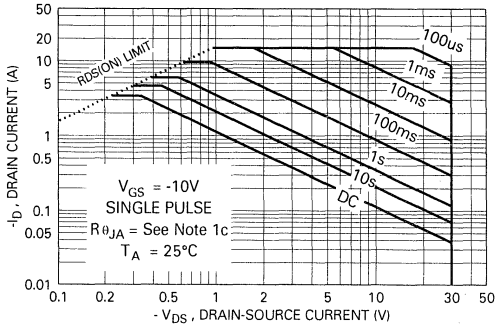


Figure 16. Maximum Safe Operating Area

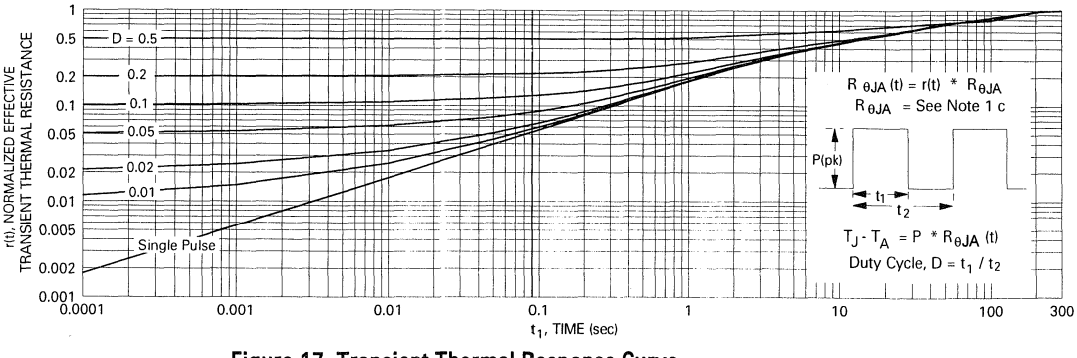


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

NDT452P

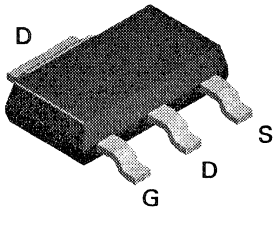
P-Channel Enhancement Mode Field Effect Transistor

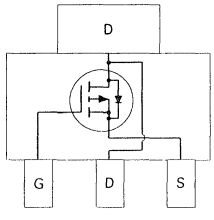
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and DC motor control.

Features

- -3A, -30V. $R_{DS(ON)}$ = 0.18Ω @ V_{GS} = -10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





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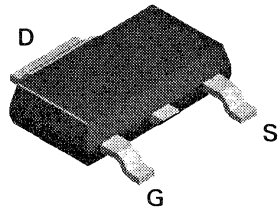
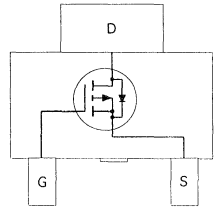




SOT-223* (J23Z)

Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT452P	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 3	A
	- Pulsed		± 20	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-2	µA
		T_J = 55°C			-25	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2	-3	V
		T_J=125°C	-0.85	-1.7	-2.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -3 A		0.15	0.18	Ω
		T_J=125°C		0.23	0.32	
		V_{GS} = -4.5 V, I_D = - 2.2 A		0.27	0.32	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5 V, V_{DS} = -5 V	-4.5			
g_{FS}	Forward Transconductance	V_{DS} = -15 V, I_D = -3 A		3.7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		525		pF
C_{oss}	Output Capacitance			300		pF
C_{rss}	Reverse Transfer Capacitance			130		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -10 V, I_D = -1.0 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		8	40	ns
t_r	Turn - On Rise Time			15	40	ns
$t_{D(off)}$	Turn - Off Delay Time			25	90	ns
t_f	Turn - Off Fall Time			8	50	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -3 A, V_{GS} = -10 V		15	25	nC
Q_{gs}	Gate-Source Charge			1.6	4	nC
Q_{gd}	Gate-Drain Charge			4.5	8	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -3 A (Note 2)			-1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

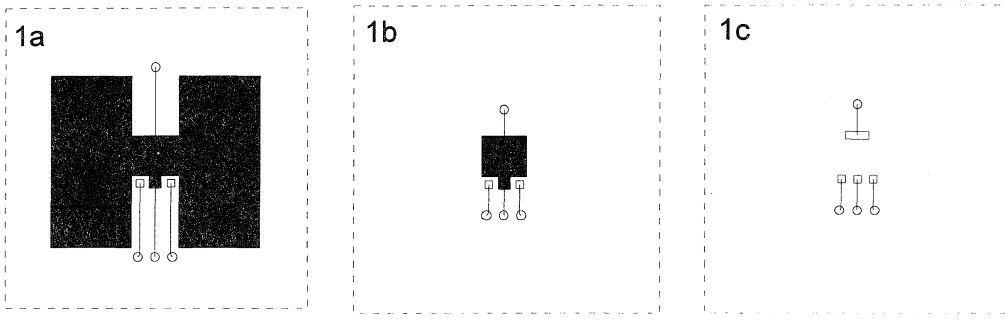
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

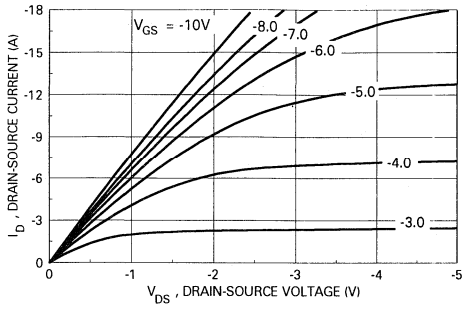


Figure 1. On-Region Characteristics.

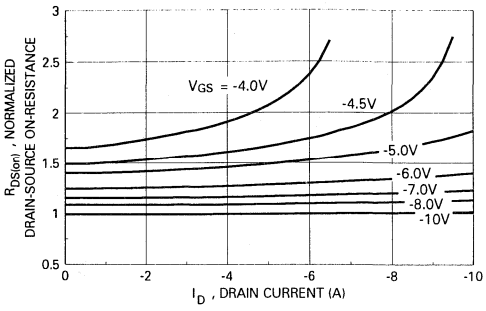


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

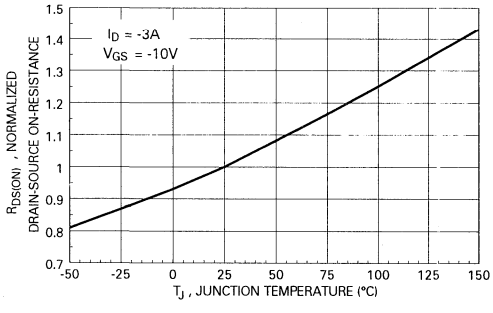


Figure 3. On-Resistance Variation with Temperature.

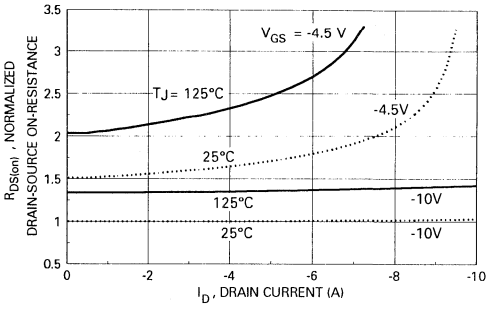


Figure 4. On-Resistance Variation with Drain Current and Temperature.

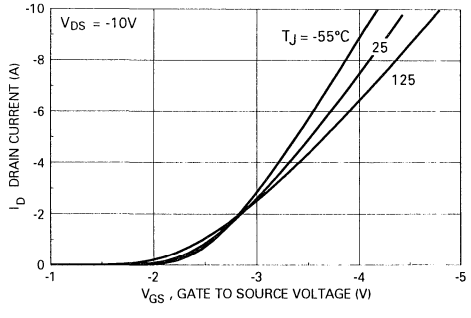


Figure 5. Transfer Characteristics

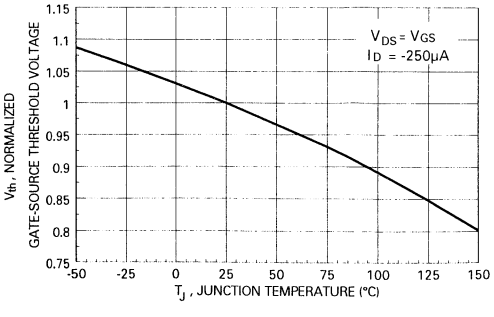


Figure 6. Gate Threshold Variation with Temperature.

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Typical Electrical Characteristics (continued)

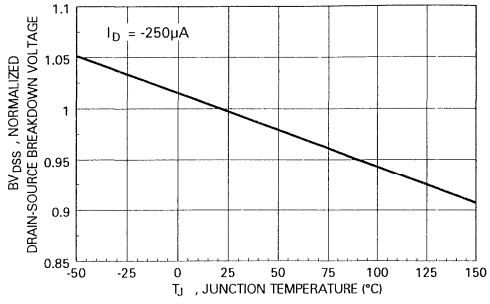


Figure 7. Breakdown Voltage Variation with Temperature.

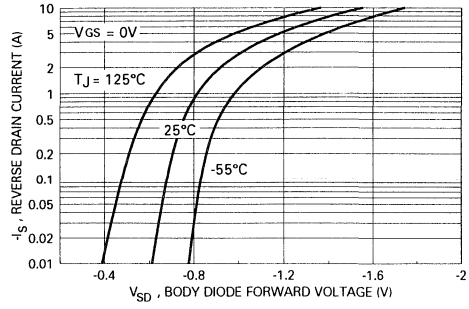


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

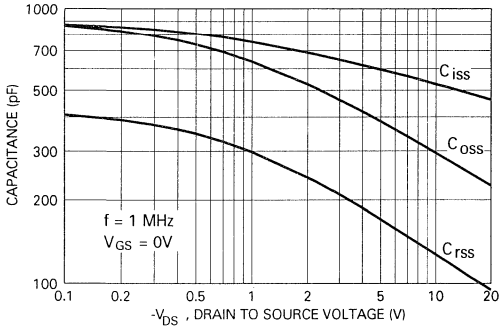


Figure 9. Capacitance Characteristics.

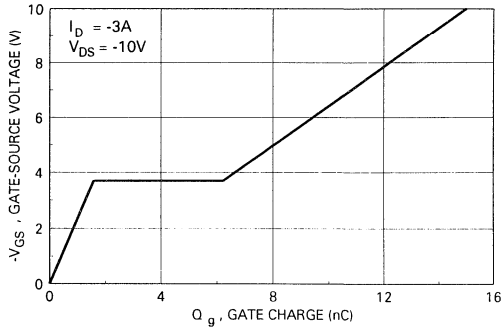


Figure 10. Gate Charge Characteristics.

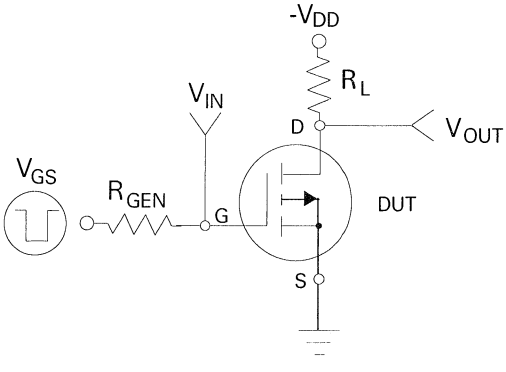


Figure 11. Switching Test Circuit

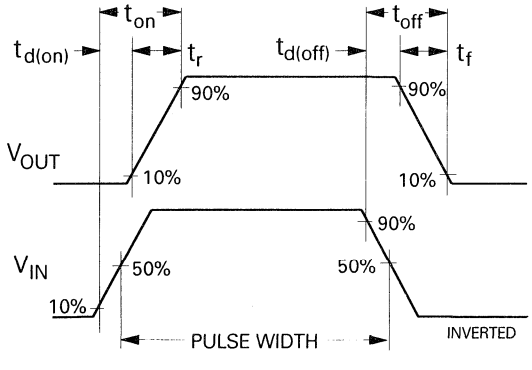


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

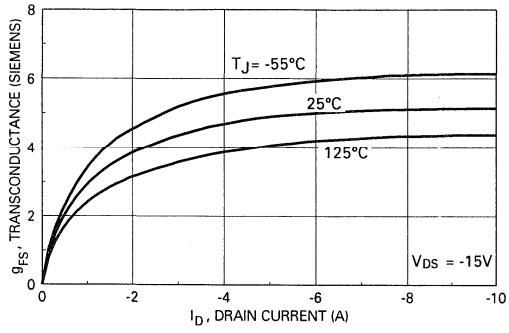


Figure 13. Transconductance Variation with Drain Current and Temperature

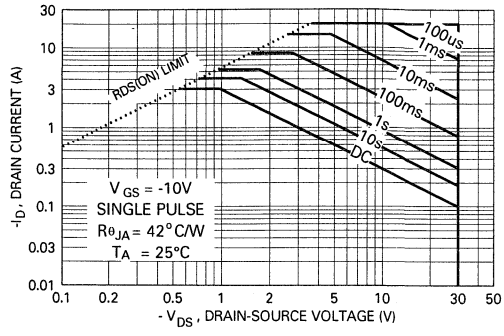


Figure 14. Maximum Safe Operating Area

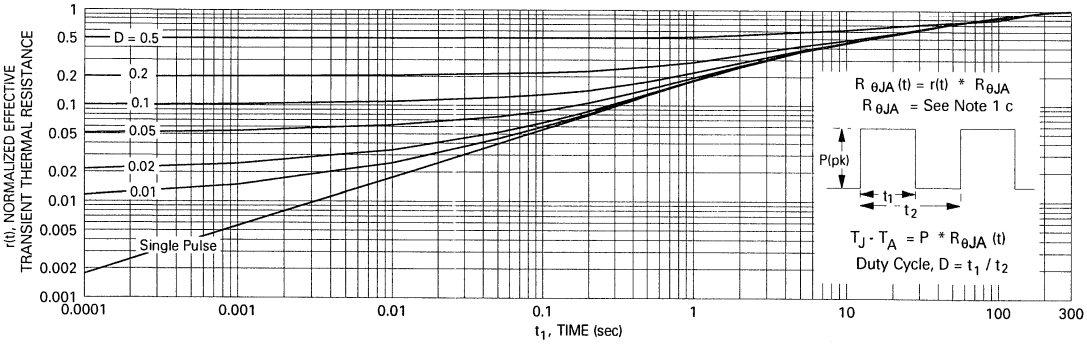


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

5

National Semiconductor™

June 1996

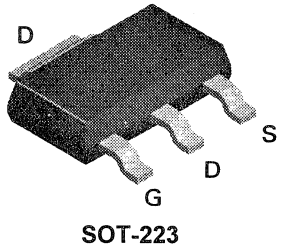
NDT453N
N-Channel Enhancement Mode Field Effect Transistor

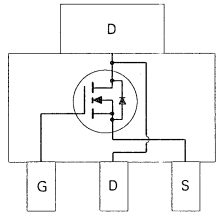
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

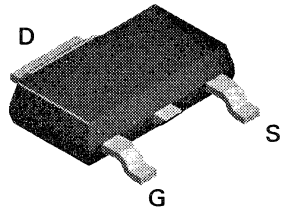
Features

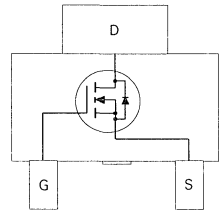
- 8A, 30V. $R_{DS(ON)}$ = 0.028Ω @ V_{GS} = 10V.
  $R_{DS(ON)}$ = 0.042Ω @ V_{GS} = 4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





SOT-223





SOT-223*
(J23Z)

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT453N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 8	A
	- Pulsed		± 15	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J,T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	2	3	V
		T_J = 125°C	0.7	1.5	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 8.0 A		0.022	0.028	Ω
		T_J = 125°C		0.03	0.045	
		V_{GS} = 4.5 V, I_D = 6.7 A		0.035	0.042	
		T_J = 125°C		0.047	0.075	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	15			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	10			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 8.0 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		890		pF
C_{oss}	Output Capacitance			560		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		10	15	ns
t_r	Turn - On Rise Time			20	35	ns
$t_{D(off)}$	Turn - Off Delay Time			40	50	ns
t_f	Turn - Off Fall Time			35	50	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 8.0 A, V_{GS} = 10 V		28	35	nC
Q_{gs}	Gate-Source Charge			4.5		nC
Q_{gd}	Gate-Drain Charge			9.5		nC

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A (Note 2)		0.8	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 2 A, dI_F/dt = 100A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

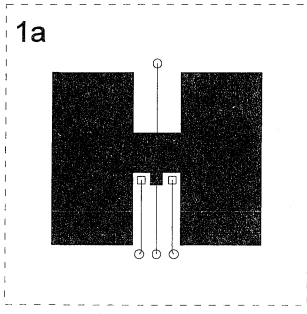
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

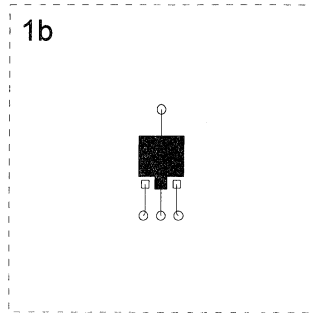
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

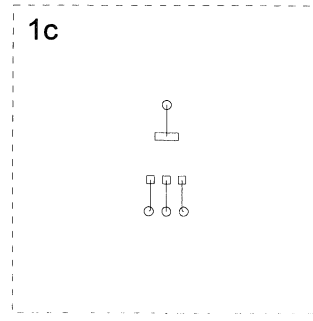
a. 42°C/W when mounted on a 1 in² pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in² pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in² pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

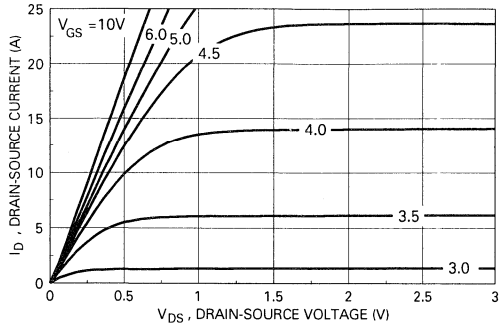


Figure 1. On-Region Characteristics.

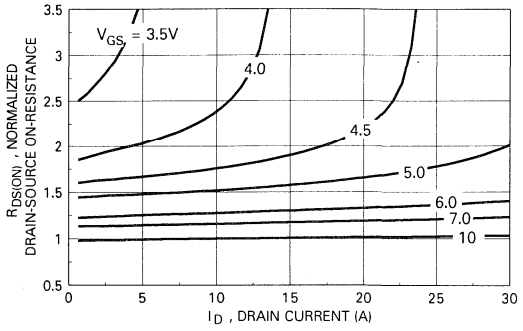


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

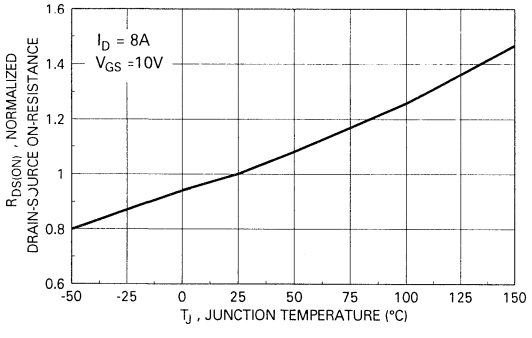


Figure 3. On-Resistance Variation with Temperature.

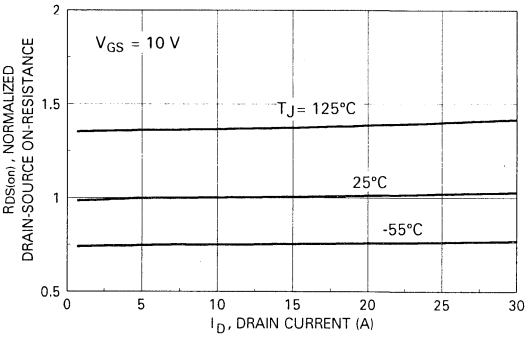


Figure 4. On-Resistance Variation with Drain Current and Temperature.

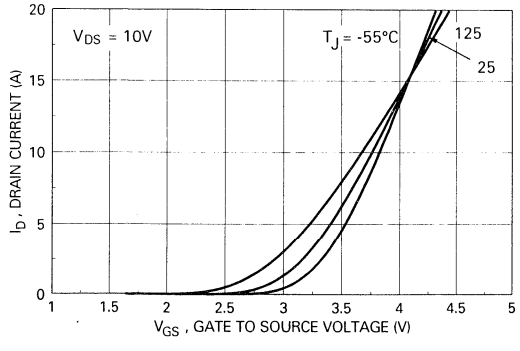


Figure 5. Transfer Characteristics.

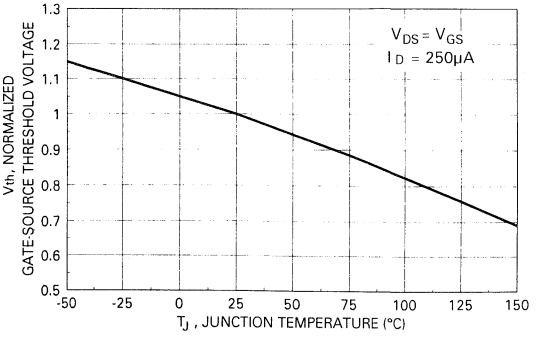


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

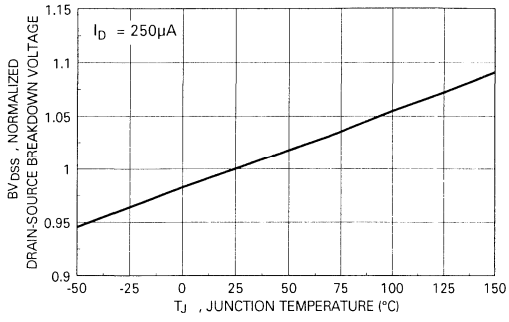


Figure 7. Breakdown Voltage Variation with Temperature.

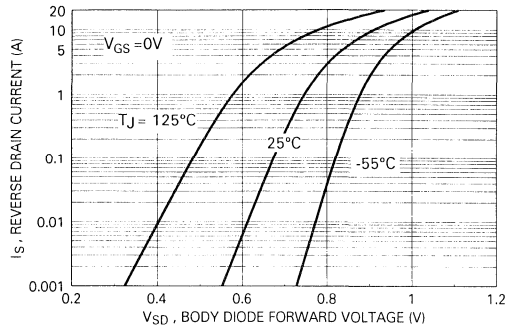


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

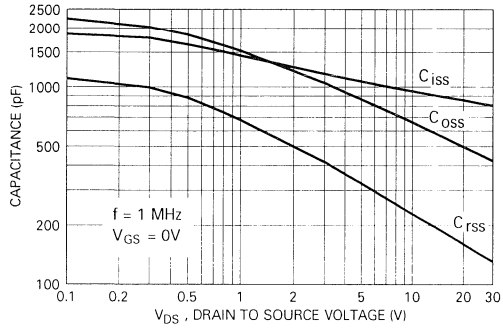


Figure 9. Capacitance Characteristics.

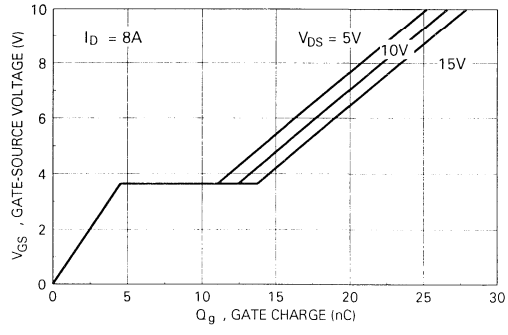


Figure 10. Gate Charge Characteristics.

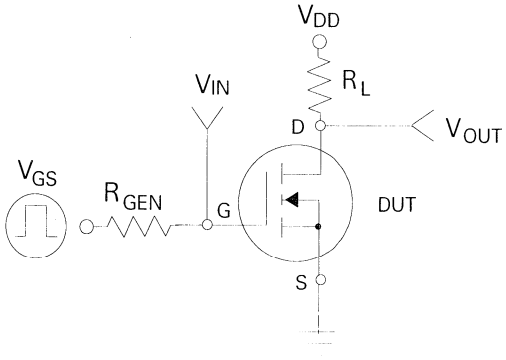


Figure 11. Switching Test Circuit

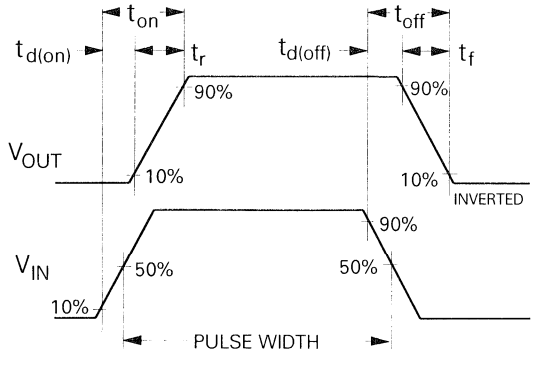


Figure 12. Switching Waveforms

Typical Electrical and Thermal Characteristics

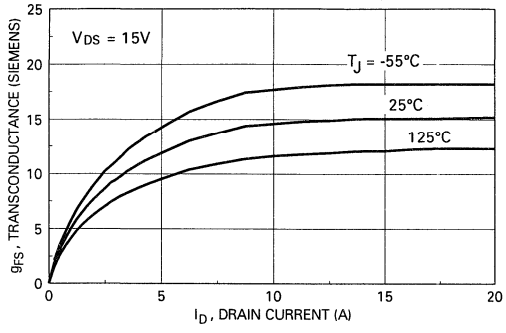


Figure 13. Transconductance Variation with Drain Current and Temperature.

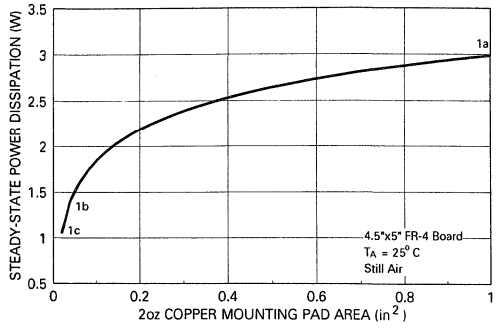


Figure 14. SOT-223 Maximum Steady- State Power Dissipation versus Copper Mounting Pad Area.

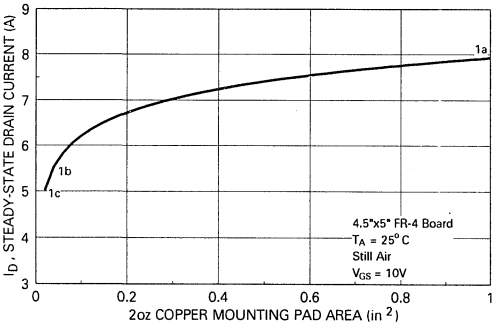


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

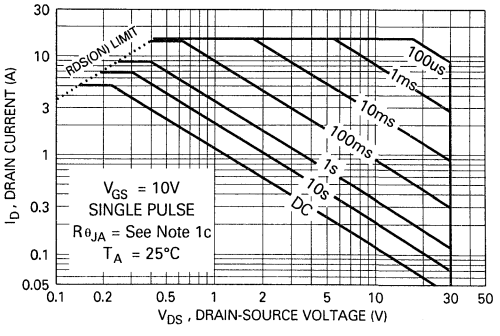


Figure 16. Maximum Safe Operating Area.

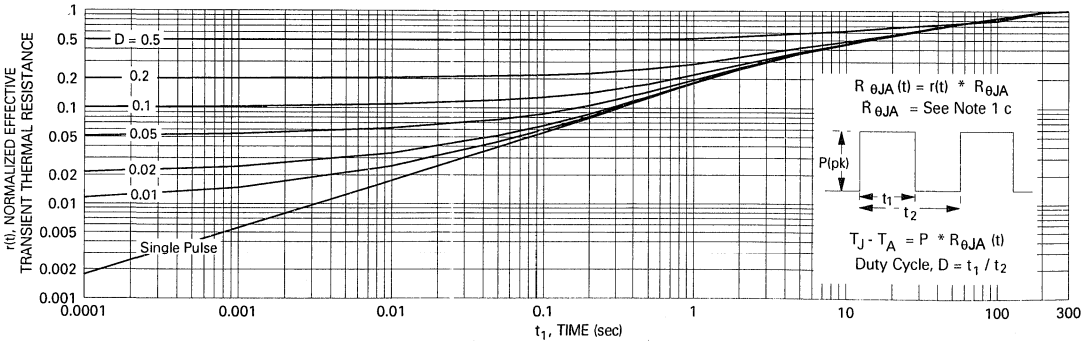


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

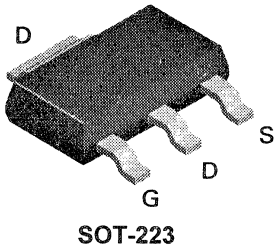
NDT454P
P-Channel Enhancement Mode Field Effect Transistor

General Description

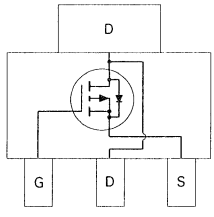
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

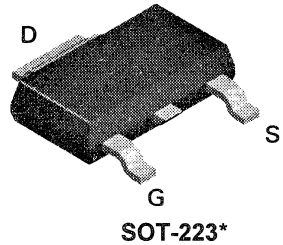
Features

- -5.9A, -30V. $R_{DS(ON)}$ = 0.05Ω @ V_{GS} = -10V
  $R_{DS(ON)}$ = 0.07Ω @ V_{GS} = -6V
  $R_{DS(ON)}$ = 0.09Ω @ V_{GS} = -4.5V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.

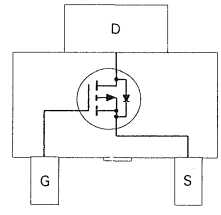


SOT-223





SOT-223*
(J23Z)



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT454P	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 5.9	A
	- Pulsed		± 15	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		V_{DS} = -15 V, V_{GS} = 0 V, T_J = 70°C			-5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1	-2.7		V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -5.9 A		0.038	0.05	Ω
		V_{GS} = -6 V, I_D = -5.2 A		0.046	0.07	
		V_{GS} = -4.5 V, I_D = -4.6 A		0.064	0.09	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-15			A
		V_{GS} = -4.5, V_{DS} = -5V	-5			
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 5.9 A		10		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		950		pF
C_{oss}	Output Capacitance			610		pF
C_{rss}	Reverse Transfer Capacitance			220		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		10	30	ns
t_r	Turn - On Rise Time			18	60	ns
$t_{D(off)}$	Turn - Off Delay Time			80	120	ns
t_f	Turn - Off Fall Time			45	100	ns
Q_g	Total Gate Charge	V_{DS} = -15 V, I_D = -5.9 A, V_{GS} = -10 V		29	40	nC
Q_{gs}	Gate-Source Charge			3		
Q_{gd}	Gate-Drain Charge			11		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.9	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -5.9 A (Note 2)		-0.85	-1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_F = -5.9 A, dI_F/dt = 100 A/µs			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

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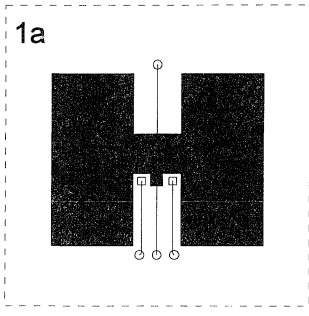
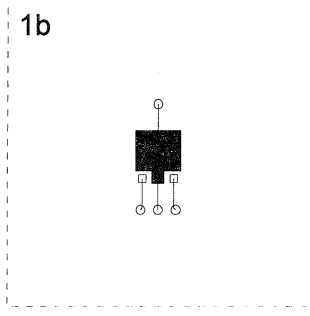
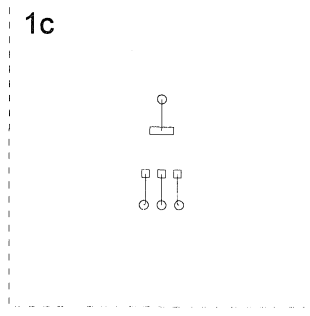
c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

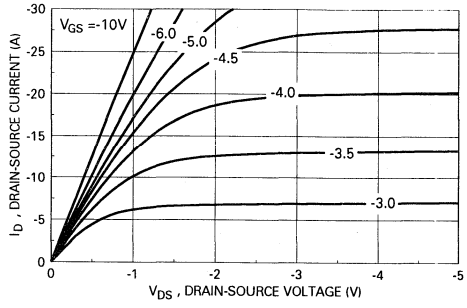


Figure 1. On-Region Characteristics

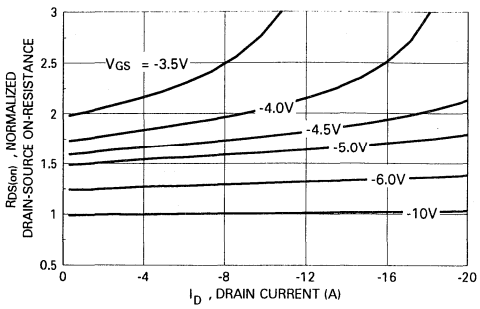


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

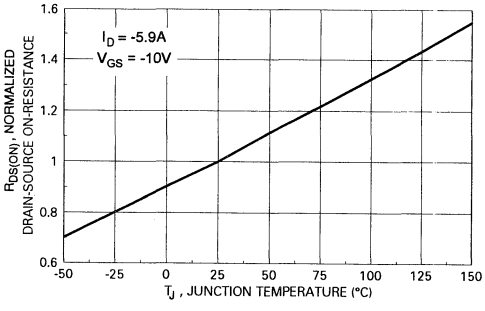


Figure 3. On-Resistance Variation with Temperature

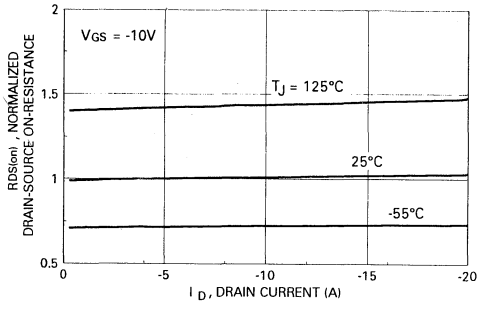


Figure 4. On-Resistance Variation with Drain Current and Temperature

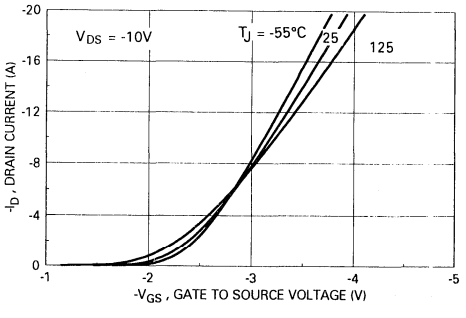


Figure 5. Transfer Characteristics

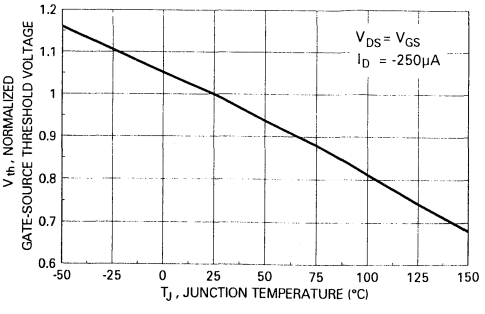


Figure 6. Gate Threshold Variation with Temperature

5

Typical Electrical Characteristics (continued)

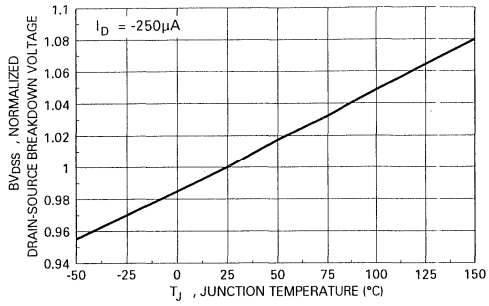


Figure 7. Breakdown Voltage Variation with Temperature

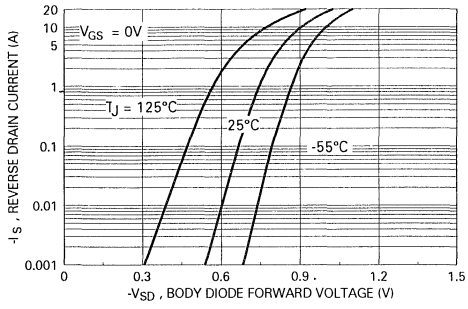


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

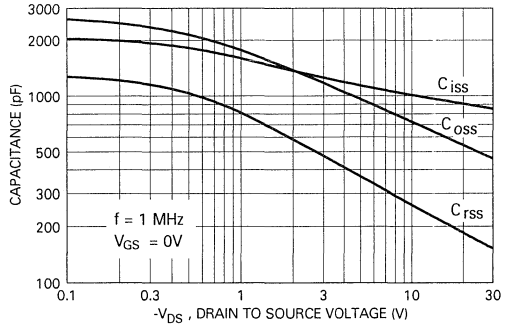


Figure 9. Capacitance Characteristics

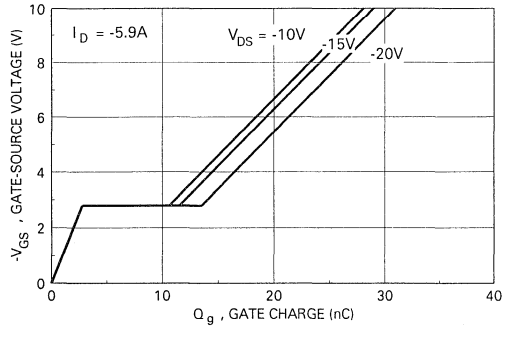


Figure 10. Gate Charge Characteristics

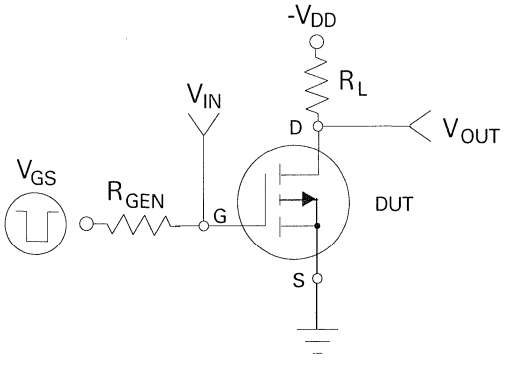


Figure 11. Switching Test Circuit

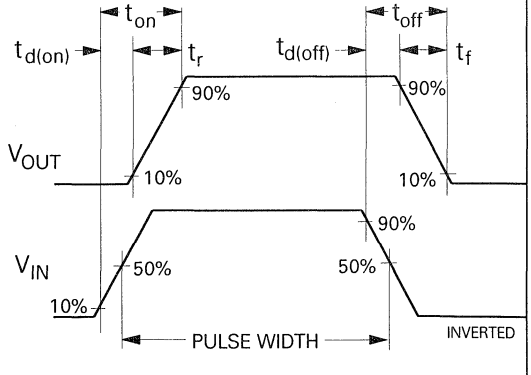


Figure 12. Switching Waveforms

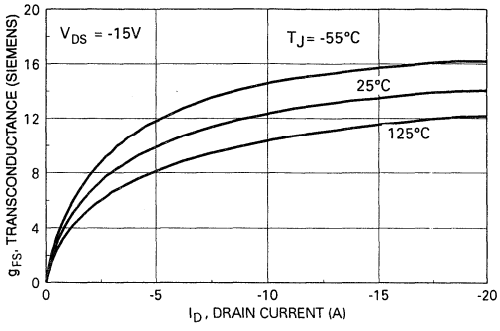


Figure 13. Transconductance Variation with Drain Current and Temperature

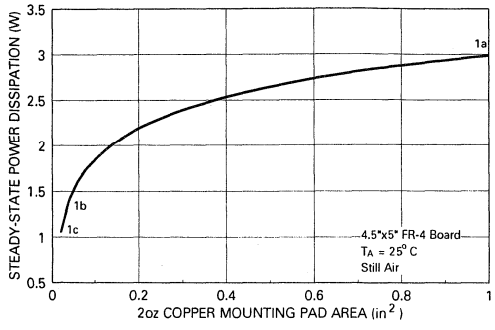


Figure 14. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

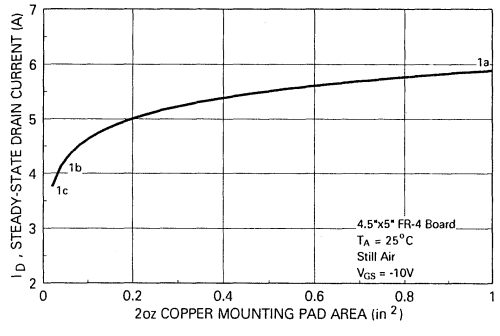


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

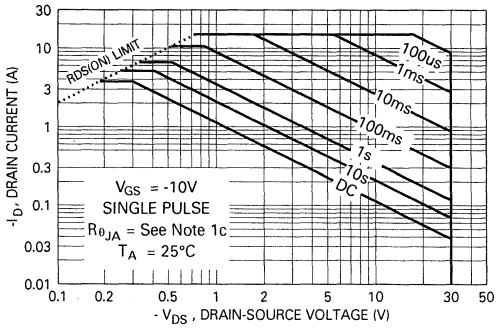


Figure 16. Maximum Safe Operating Area

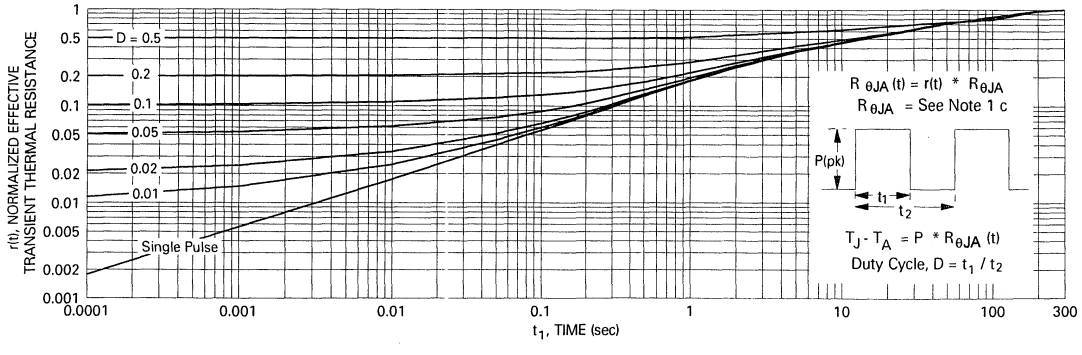


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

July 1996

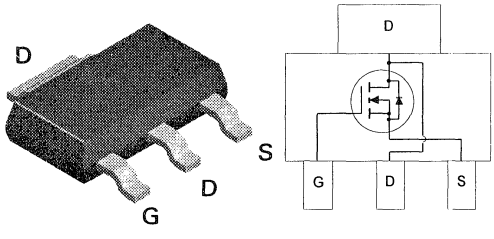
NDT455N
N-Channel Enhancement Mode Field Effect Transistor

General Description

These N-Channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 11.5 A, 30 V. $R_{DS(ON)}$ = 0.015 Ω @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 0.02 Ω @ V_{GS} = 4.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



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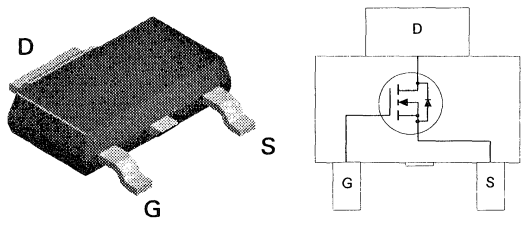


SOT-223*
(J23Z)

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT455N	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		20	V
I_D	Drain Current - Continuous	(Note 1a)	± 11.5	A
	- Pulsed		± 40	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			1	µA
		T_J = 55°C			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	3	V
		T_J = 125°C	0.7	0.9	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 11.5 A		0.013	0.015	Ω
		T_J = 125°C		0.019	0.03	
		V_{GS} = 4.5 V, I_D = 10 A		0.018	0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	30			A
		V_{GS} = 4.5 V, V_{DS} = 5 V	15			
G_{fs}	Forward Transconductance	V_{GS} = 10 V, I_D = 11.5 A		26		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15, V_{GS} = 0 V, f = 1.0 MHz		1220		pF
C_{oss}	Output Capacitance			715		pF
C_{rss}	Reverse Transfer Capacitance			280		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Turn - On Rise Time			16	30	ns
$t_{D(off)}$	Turn - Off Delay Time			48	80	ns
t_f	Turn - Off Fall Time			40	70	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 11.5 A, V_{GS} = 10 V		43	61	nC
Q_{gs}	Gate-Source Charge			4		nC
Q_{gd}	Gate-Drain Charge			11		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				2.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.5 A (Note 2)		0.845	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 2.5 A dI_F/dt = 100 A/µs			140	ns

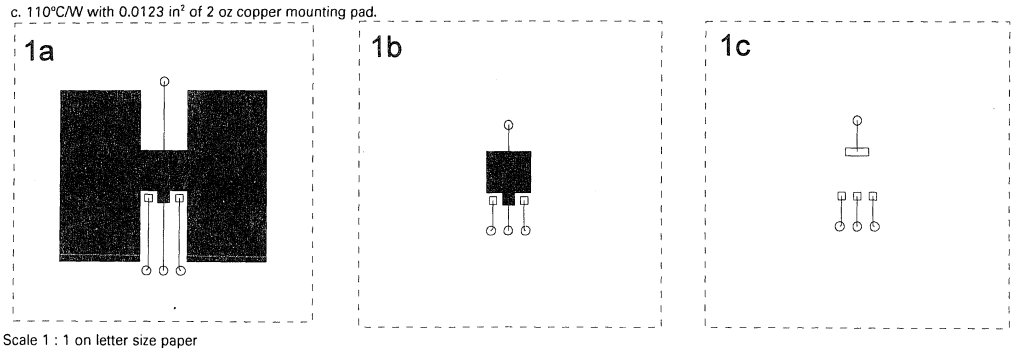
Notes:

1. $P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$ $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is defined by users. For general reference: Applications on 4.5"x5" FR-4 PCB under still air environment, typical $R_{\theta JA}$ is found to be:

   a. 42°C/W with 1 in^2 of 2 oz copper mounting pad.

   b. 95°C/W with 0.066 in^2 of 2 oz copper mounting pad.

   c. 110°C/W with 0.0123 in^2 of 2 oz copper mounting pad.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

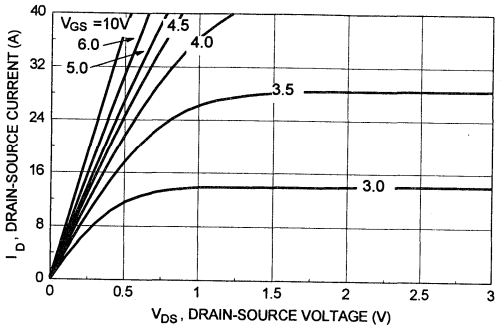


Figure 1. On-Region Characteristics.

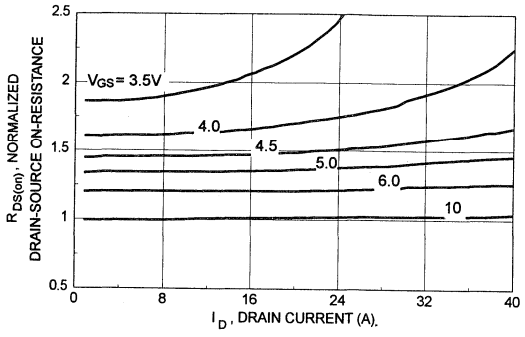


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

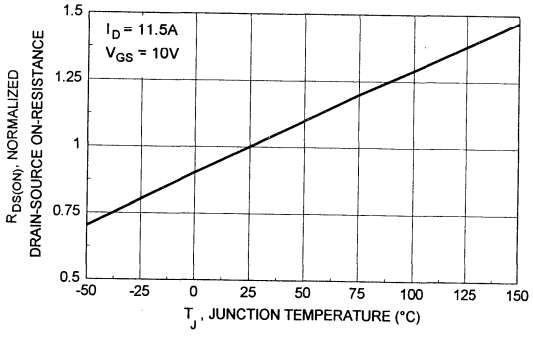


Figure 3. On-Resistance Variation with Temperature.

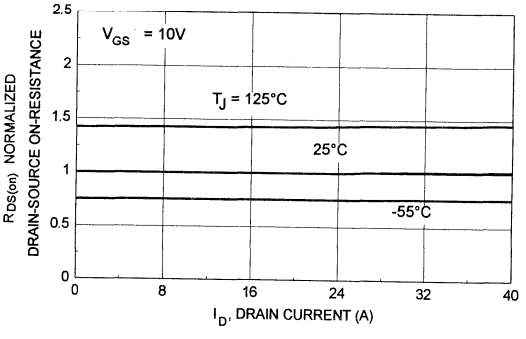


Figure 4. On-Resistance Variation with Drain Current and Temperature.

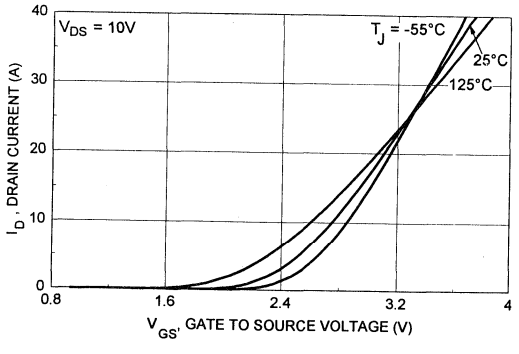


Figure 5. Transfer Characteristics.

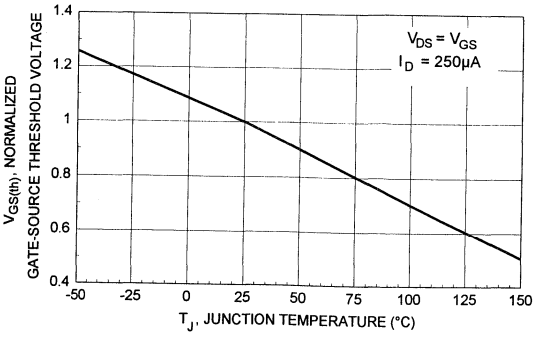


Figure 6. Gate Threshold Variation with Temperature.

5

Typical Electrical Characteristics

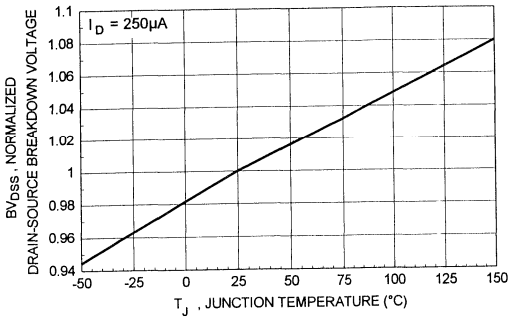


Figure 7. Breakdown Voltage Variation with Temperature.

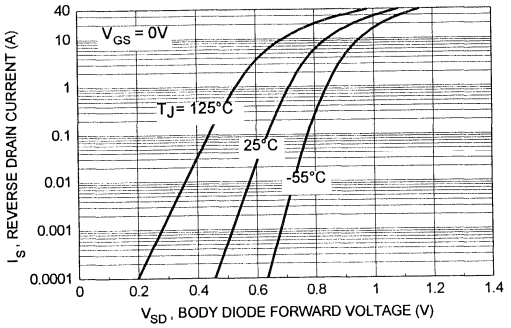


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

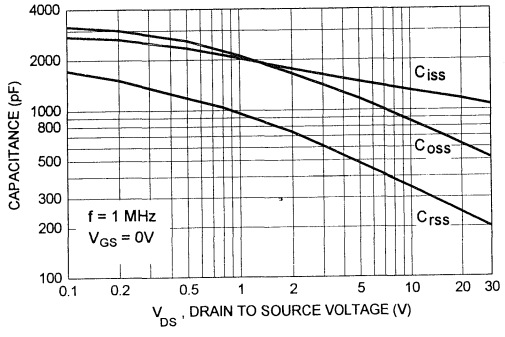


Figure 9. Capacitance Characteristics.

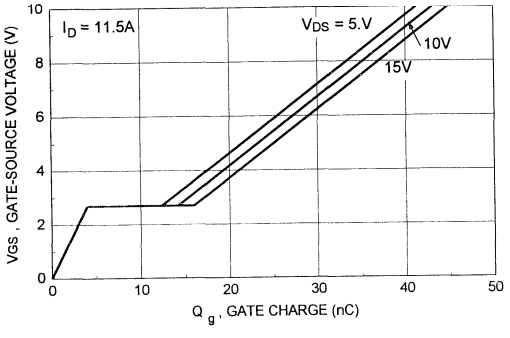


Figure 10. Gate Charge Characteristics.

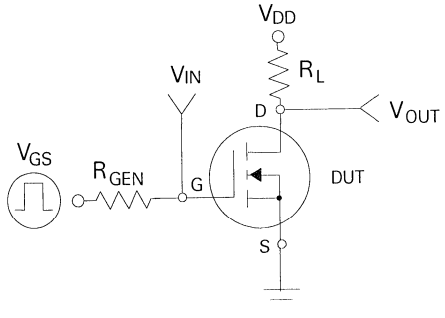


Figure 11. Switching Test Circuit

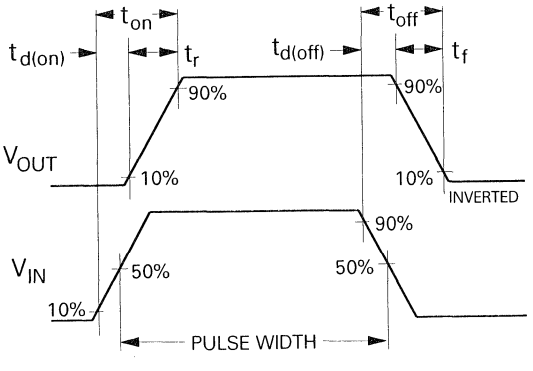


Figure 12. Switching Waveforms

Typical Thermal Characteristics

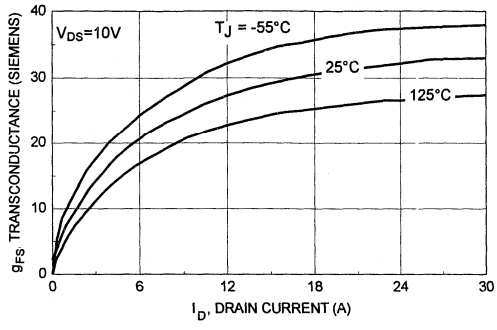


Figure 13. Transconductance Variation with Drain Current and Temperature.

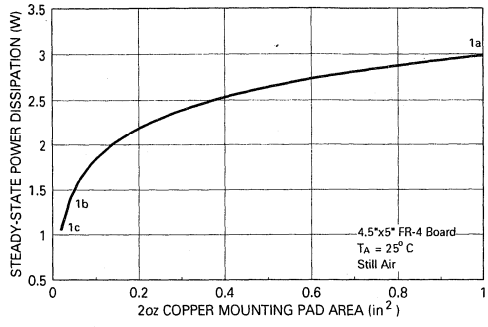


Figure 14. SOT-223 Maximum Steady- State Power Dissipation versus Copper Mounting Pad Area.

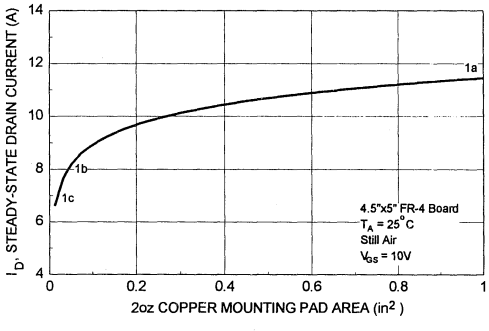


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

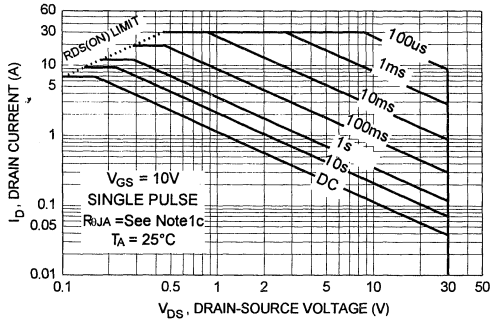


Figure 16. Maximum Safe Operating Area

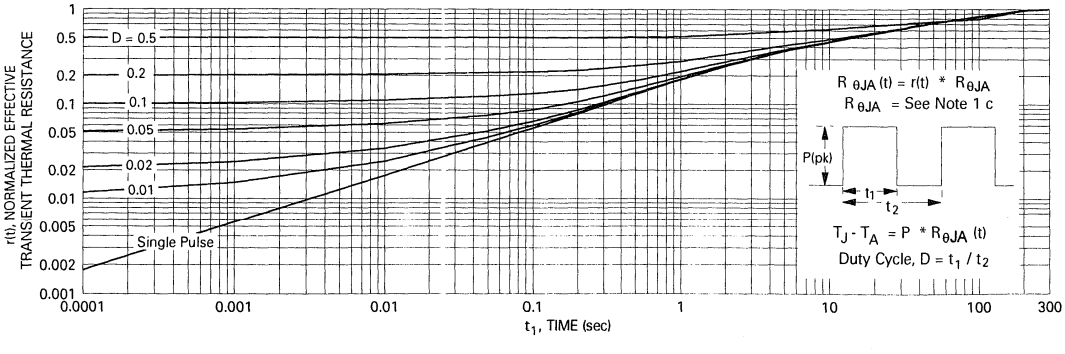


Figure 17. Typical Transient Thermal Impedance Curve.

Remark: Thermal characterization performed under the conditions of Note 1c. Should better thermal design employs, $R_{\theta JA}$ will be lower and reach thermal equivalent sooner.

National Semiconductor™

July 1996

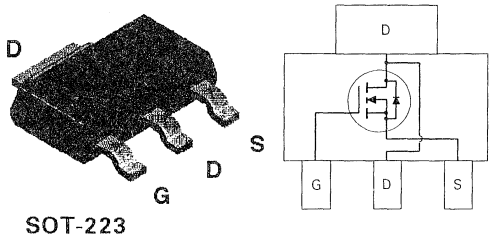
NDT456P
P-Channel Enhancement Mode Field Effect Transistor

General Description

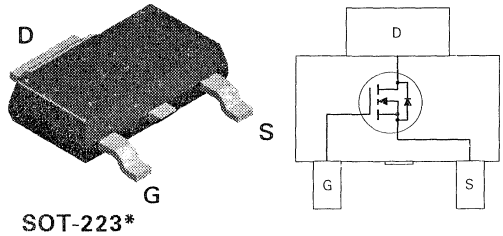
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance. And withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management, battery powered circuits, and DC motor control.

Features

- -7.5 A, -30 V. $R_{DS(ON)}$ = 0.03 Ω @ V_{GS} = -10 V
  $R_{DS(ON)}$ = 0.045 Ω @ V_{GS} = -4.5 V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.



SOT-223



SOT-223*
(J23Z)

Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT456P	Units
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current - Continuous	(Note 1a)	±7.5	A
	- Pulsed		±20	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = - 250 µA	-1	-1.5	-3	V
		T_J = 125°C	-0.5	-1.1	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -7.5 A		0.026	0.03	Ω
		T_J = 125°C		0.035	0.054	
		V_{GS} = - 4.5 V, I_D = -6 A		0.041	0.045	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V , V_{DS} = - 5 V	-20			A
		V_{GS} = -4.5 V, V_{DS} = - 5 V	-10			
G_{fs}	Forward Transconductance	V_{GS} = -10 V, I_D = -7.5 A		13		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1.0 MHz		1440		pF
C_{oss}	Output Capacitance			905		pF
C_{rss}	Reverse Transfer Capacitance			355		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -15 V, I_D = -7 A, V_{GEN} = -10 V, R_{GEN} = 12 Ω		10	20	ns
t_r	Turn - On Rise Time			65	120	ns
$t_{D(off)}$	Turn - Off Delay Time			70	130	ns
t_f	Turn - Off Fall Time			70	130	ns
Q_g	Total Gate Charge	V_{DS} = -10 V, I_D = -7.5 A, V_{GS} = -10 V		47	67	nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			12		nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.5	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = - 2.5 A (Note 2)		- 0.85	-1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = - 2.5 A dI_F/dt = 100 A/µs			140	ns

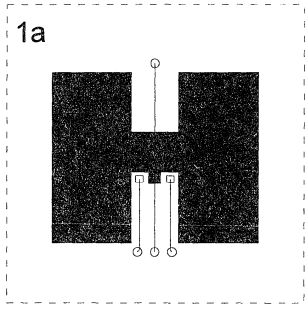
Notes:

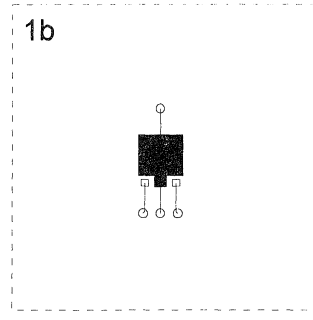
1. $P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$ $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is defined by users. For general reference: Applications on 4.5"x5" FR-4 PCB under still air environment, typical $R_{\theta JA}$ is found to be:

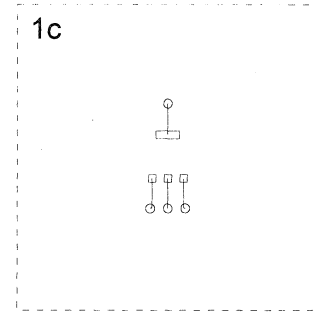
   a. 42°C when mounted on a 1 in^2 pad of 2oz copper.

   b. 95°C when mounted on a 0.066in^2 pad of 2oz copper.

   c. 110°C/W when mounted on a 0.00123in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

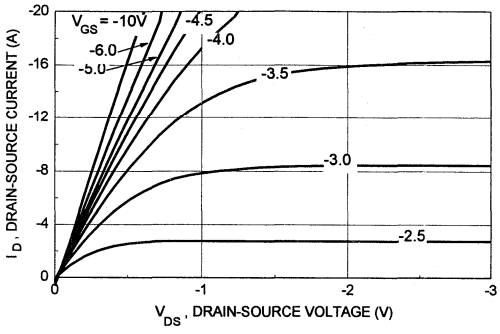


Figure 1. On-Region Characteristics.

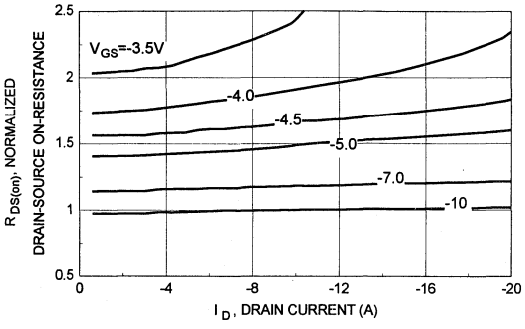


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

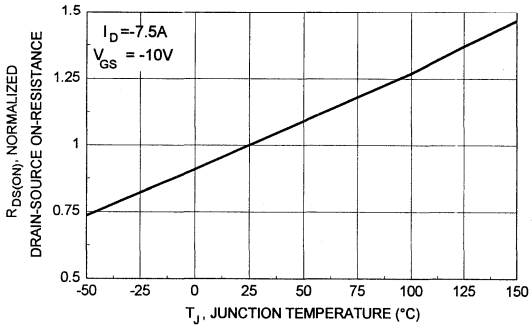


Figure 3. On-Resistance Variation with Temperature.

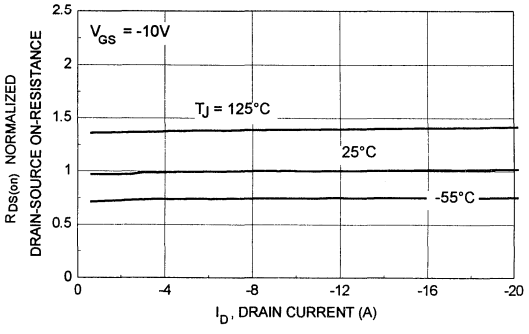


Figure 4. On-Resistance Variation with Drain Current and Temperature.

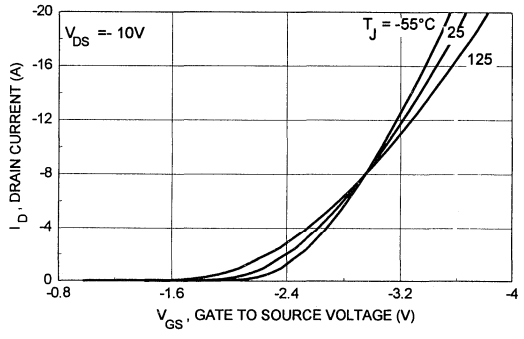


Figure 5. Transfer Characteristics.

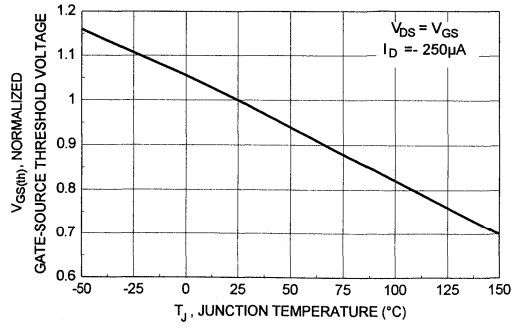


Figure 6. Gate Threshold Variation with Temperature.

5

Typical Electrical Characteristics

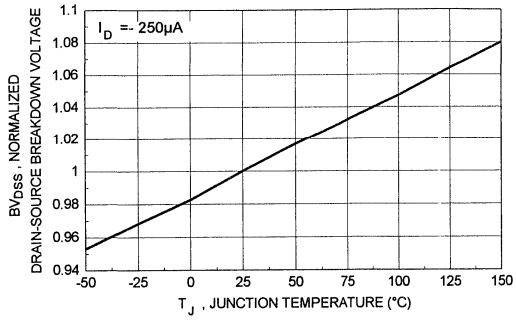


Figure 7. Breakdown Voltage Variation with Temperature.

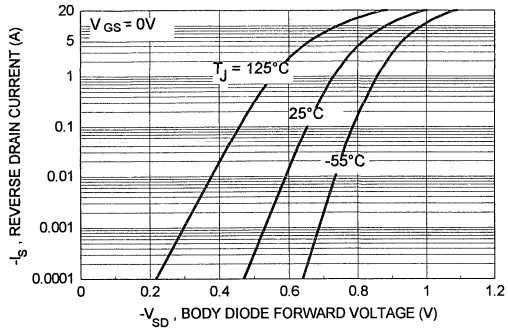


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

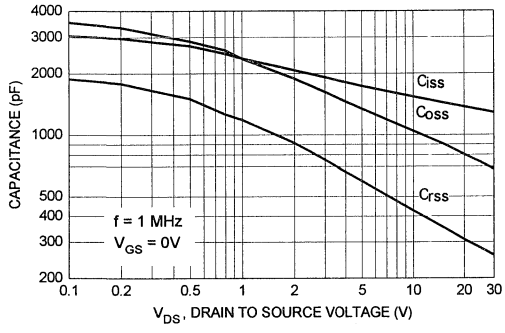


Figure 9. Capacitance Characteristics.

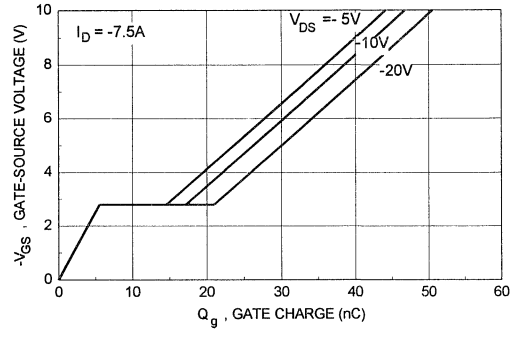


Figure 10. Gate Charge Characteristics.

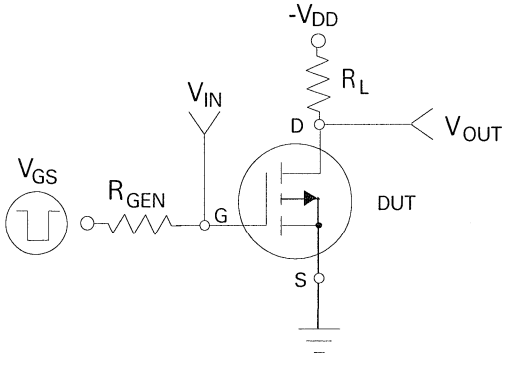


Figure 11. Switching Test Circuit

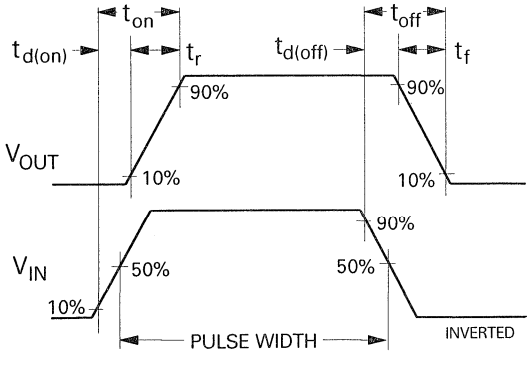


Figure 12. Switching Waveforms

Typical Thermal Characteristics

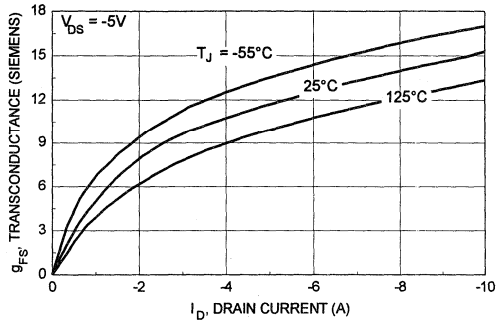


Figure 13. Transconductance Variation with Drain Current and Temperature.

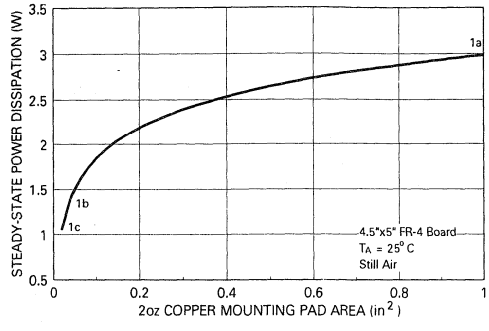


Figure 14. SOT-223 Maximum Steady-State Power Dissipation versus Copper Mounting Pad Area.

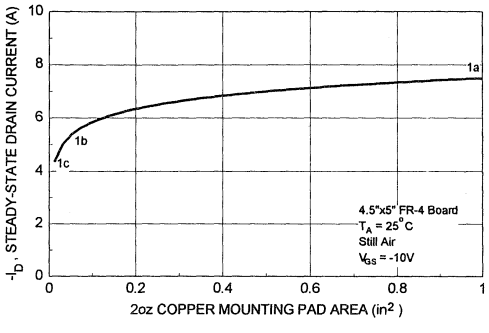


Figure 15. Maximum Steady-State Drain Current versus Copper Mounting Pad Area.

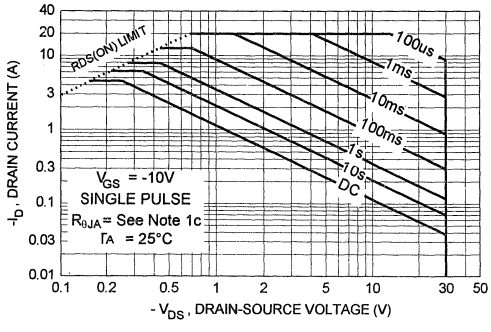


Figure 16. Maximum Safe Operating Area

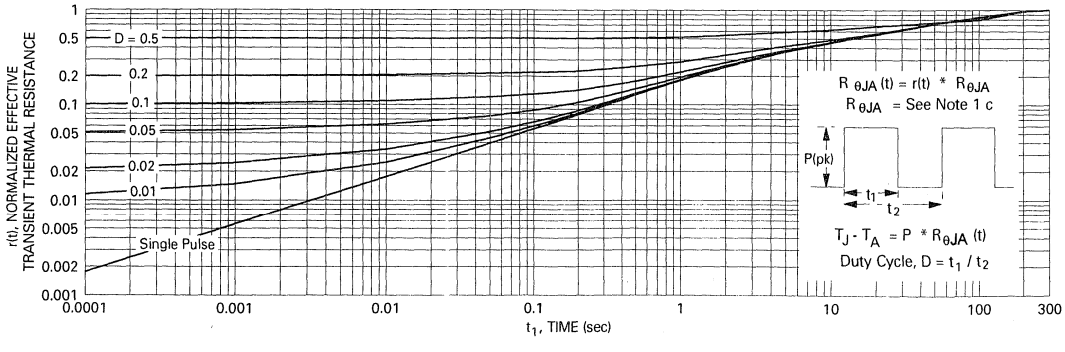


Figure 17. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

National Semiconductor™

June 1996

NDT2955

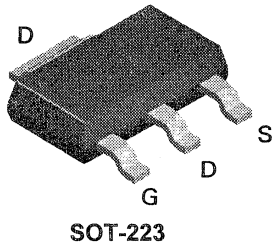
P-Channel Enhancement Mode Field Effect Transistor

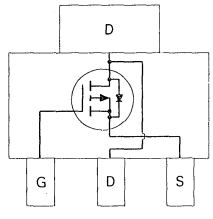
General Description

These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as notebook computer power management and DC motor control.

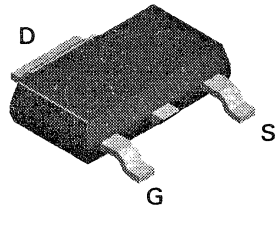
Features

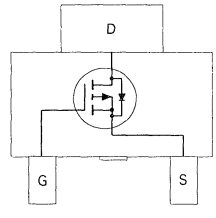
- -2.5A, -60V. $R_{DS(ON)}$ = 0.3Ω @ V_{GS} = -10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





SOT-223





SOT-223*
(J23Z)

Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT2955	Units
V_{DSS}	Drain-Source Voltage		-60	V
V_{GSS}	Gate-Source Voltage		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	-2.5	A
	- Pulsed		-15	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -60 V, V_{GS} = 0 V			-10	µA
		T_J = 125°C			-100	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2	-2.4	-4	V
		T_J = 125°C	-0.8	-2	-2.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.5 A		0.21	0.3	Ω
		T_J = 125°C		0.3	0.45	
		V_{GS} = -4.5 V, I_D = -2 A		0.36	0.5	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	-12			A
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -2.5 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		570		pF
C_{oss}	Output Capacitance			140		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -30 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω		8	15	ns
t_r	Turn - On Rise Time			20	40	ns
$t_{D(off)}$	Turn - Off Delay Time			20	40	ns
t_f	Turn - Off Fall Time			5	20	ns
Q_g	Total Gate Charge	V_{DS} = -30 V, I_D = -2.5 A, V_{GS} = -10 V		16	25	nC
Q_{gs}	Gate-Source Charge			2	5	nC
Q_{gd}	Gate-Drain Charge			4	8	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-2.3	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.5 A (Note2)			-1.3	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

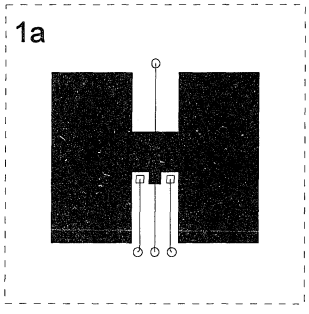
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

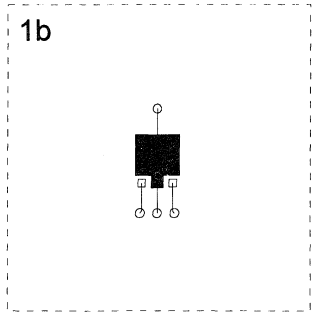
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

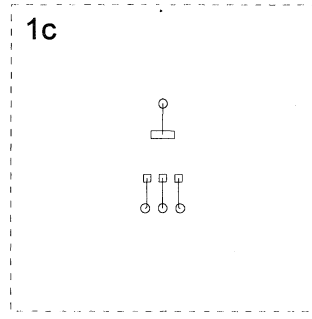
a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

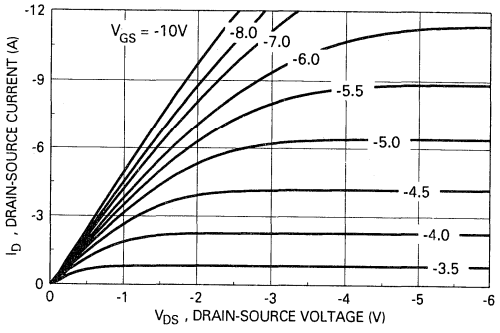


Figure 1. On-Region Characteristics.

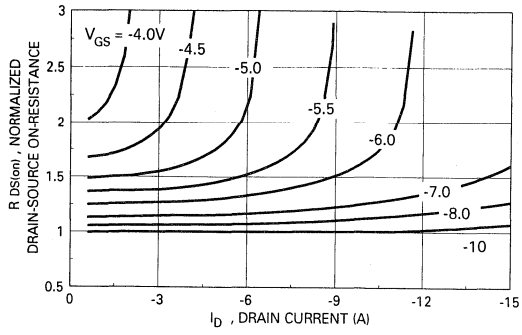


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

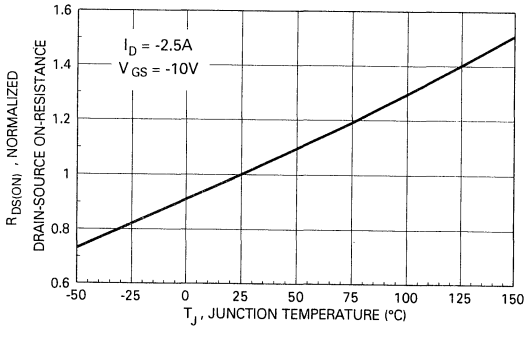


Figure 3. On-Resistance Variation with Temperature.

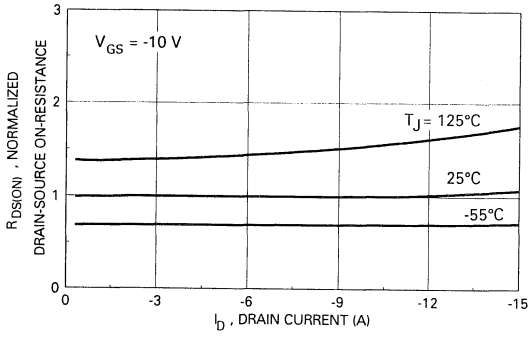


Figure 4. On-Resistance Variation with Drain Current and Temperature.

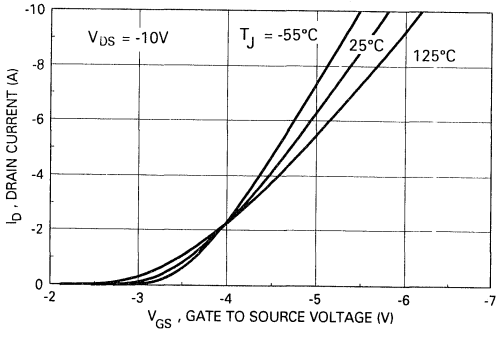


Figure 5. Transfer Characteristics

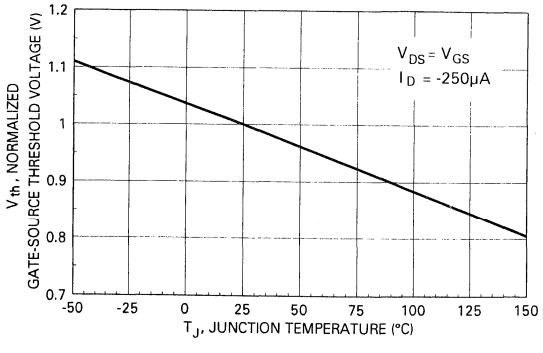


Figure 6. Gate Threshold Variation with Temperature.

5

Typical Electrical Characteristics (continued)

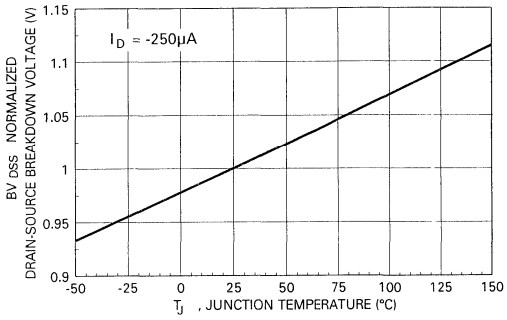


Figure 7. Breakdown Voltage Variation with Temperature.

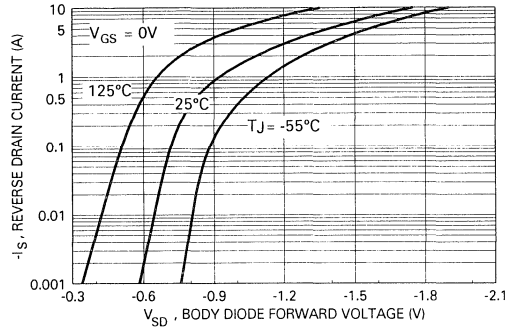


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

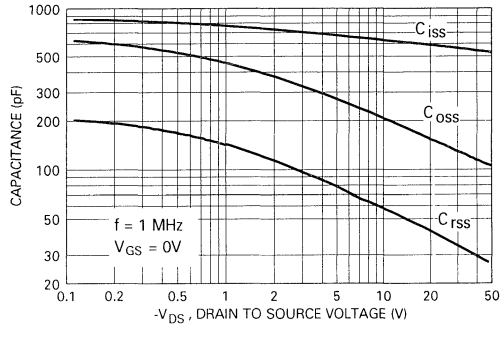


Figure 9. Capacitance Characteristics.

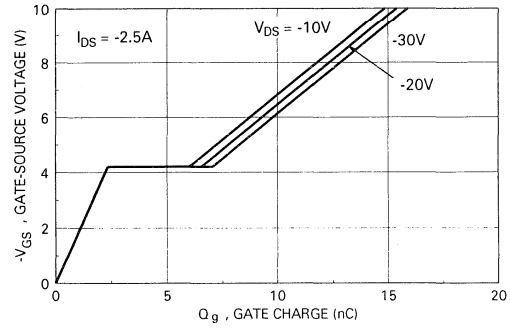


Figure 10. Gate Charge Characteristics

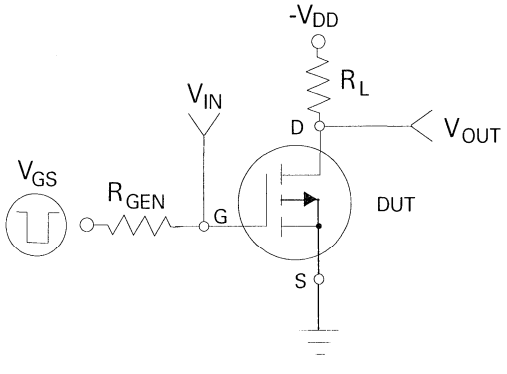


Figure 11. Switching Test Circuit

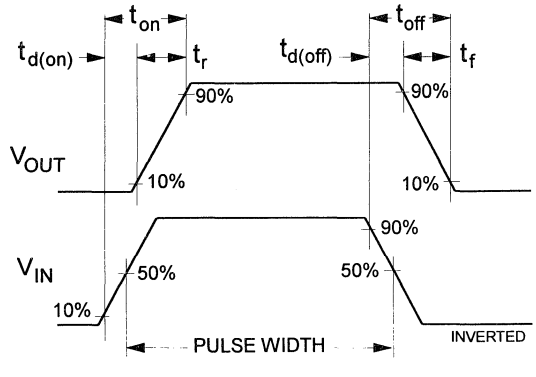


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

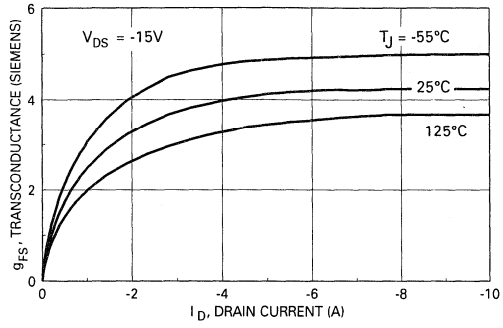


Figure 13. Transconductance Variation with Drain Current and Temperature.

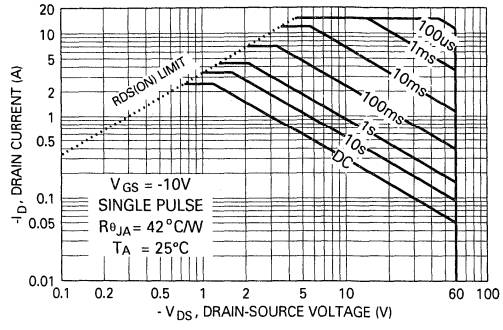


Figure 14. Maximum Safe Operating Area.

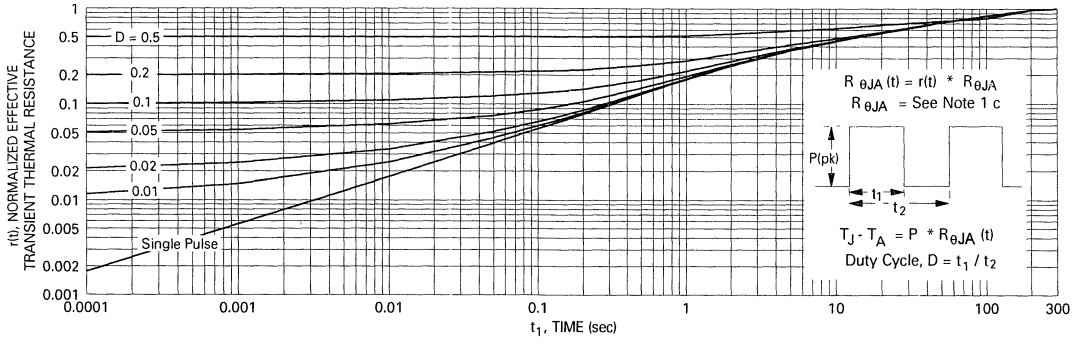


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

5

National Semiconductor™

June 1996

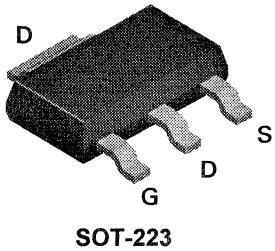
NDT3055
N-Channel Enhancement Mode Field Effect Transistor

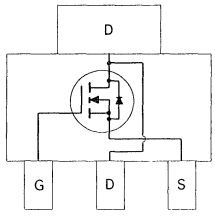
General Description

These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 4A, 60V. $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





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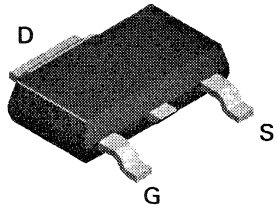
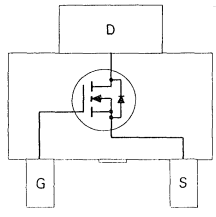




SOT-223*
(J23Z)

Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT3055	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage - Continuous		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 4	A
	- Pulsed		± 25	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J, T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			100	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.9	4	V
		T_J = 100°C	1.5	2.3	3	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4 A		0.075	0.1	Ω
		T_J = 125°C		0.13	0.22	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 4 A		3.5		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1.0 MHz		350		pF
C_{oss}	Output Capacitance			135		pF
C_{rss}	Reverse Transfer Capacitance			40		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1.2 A, V_{GS} = 10 V, R_{GEN} = 50 Ω		18	25	ns
t_r	Turn - On Rise Time			25	50	ns
$t_{D(off)}$	Turn - Off Delay Time			43	65	ns
t_f	Turn - Off Fall Time			34	60	ns
Q_g	Total Gate Charge	V_{DS} = 40 V, I_D = 4 A, V_{GS} = 10 V		10	15	nC
Q_{gs}	Gate-Source Charge			2	4	nC
Q_{gd}	Gate-Drain Charge			6	10	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Source-Drain Diode Forward Current				2.5	A
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 4 A (Note 2)			1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

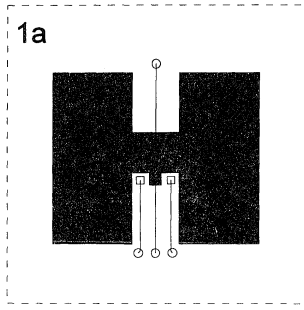
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

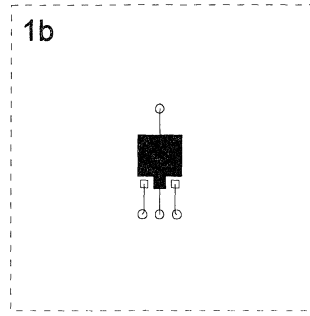
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

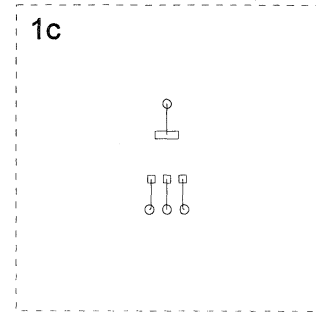
a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

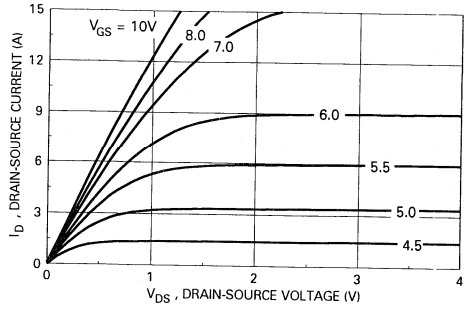


Figure 1. On-Region Characteristics.

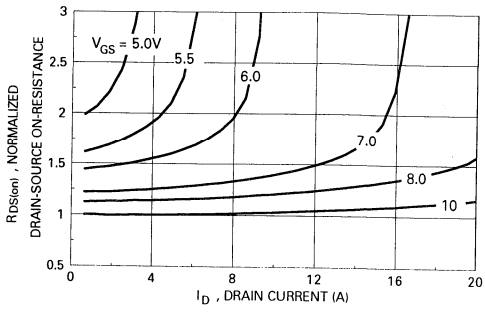


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

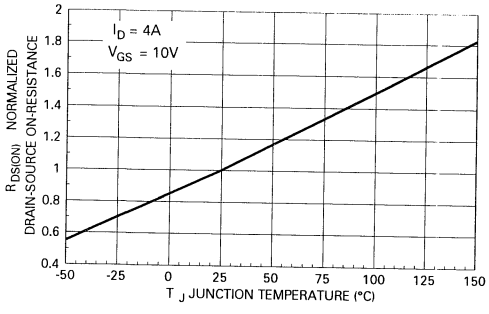


Figure 3. On-Resistance Variation with Temperature.

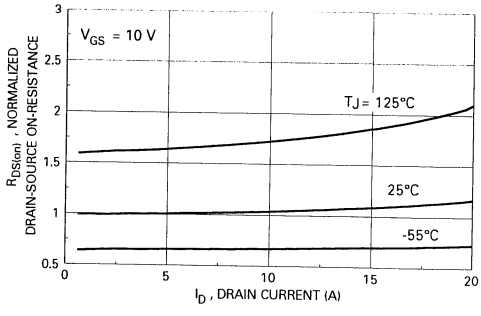


Figure 4. On-Resistance Variation with Drain Current and Temperature.

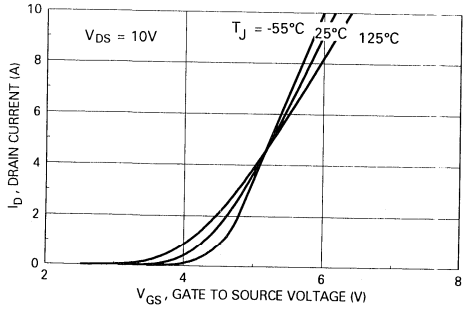


Figure 5. Transfer Characteristics

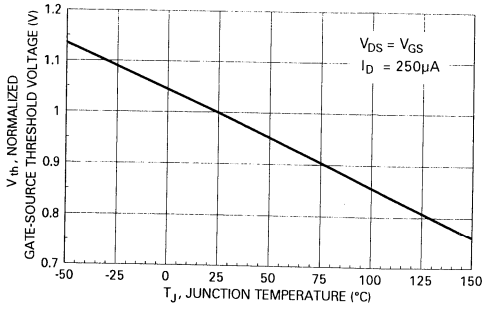


Figure 6. Gate Threshold Variation with Temperature.

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Typical Electrical Characteristics (continued)

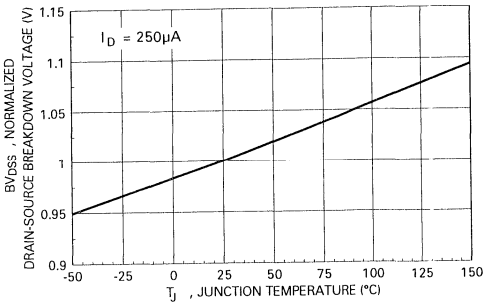


Figure 7. Breakdown Voltage Variation with Temperature.

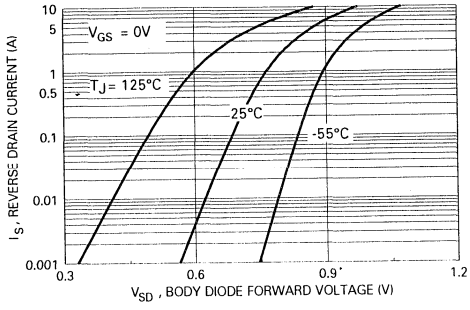


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

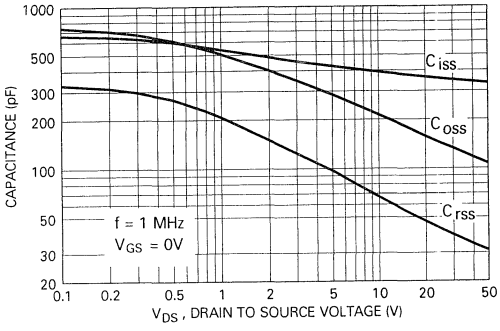


Figure 9. Capacitance Characteristics.

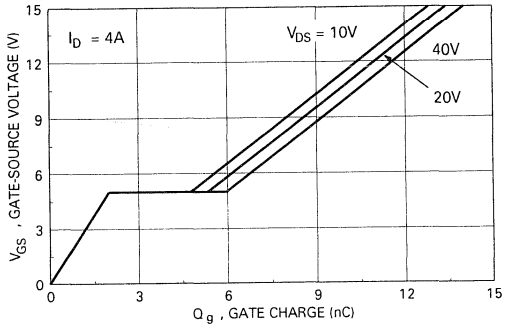


Figure 10. Gate Charge Characteristics.

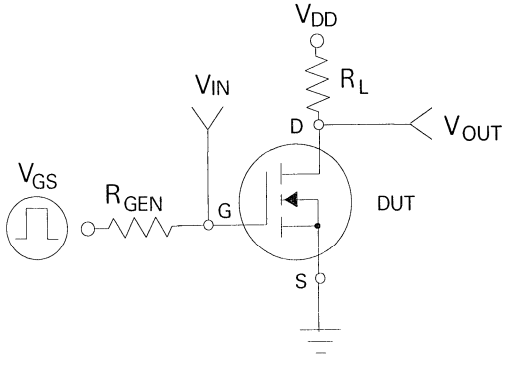


Figure 11. Switching Test Circuit

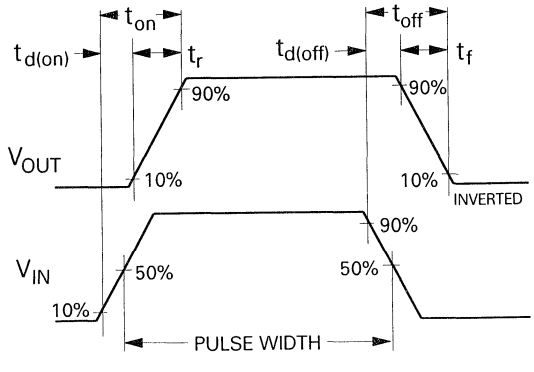


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

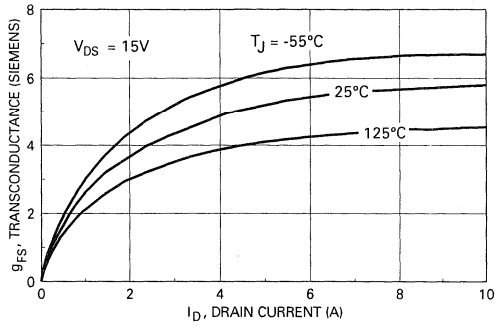


Figure 13. Transconductance Variation with Drain Current and Temperature

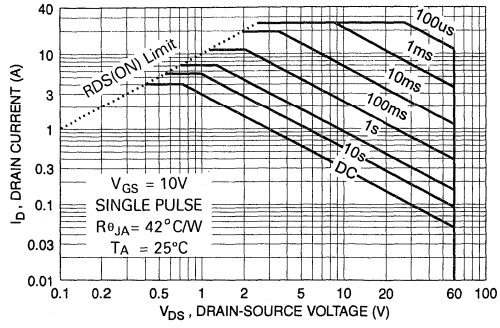


Figure 14. Maximum Safe Operating Area

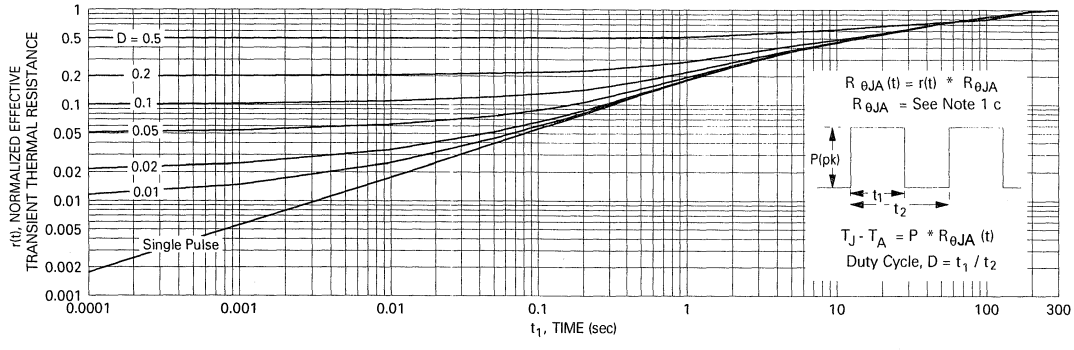


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

5

National Semiconductor™

March 1996

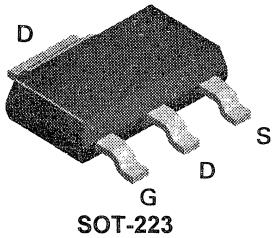
NDT3055L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

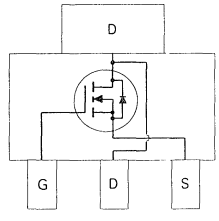
General Description

These logic level N-Channel enhancement mode field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as DC motor control and DC/DC conversion where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- 3.7A, 60V. $R_{DS(ON)}$ = 0.12Ω @ V_{GS} = 4.5V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.





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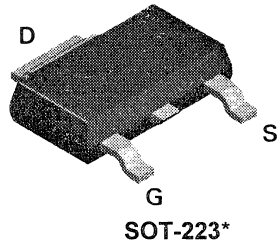

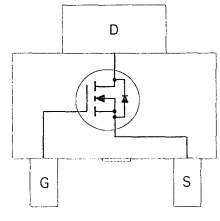

SOT-223*
(J23Z)

Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter		NDT3055L	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage - Continuous		± 20	V
I_D	Drain Current - Continuous	(Note 1a)	± 3.7	A
	- Pulsed		± 25	
P_D	Maximum Power Dissipation	(Note 1a)	3	W
		(Note 1b)	1.3	
		(Note 1c)	1.1	
T_J,T_{STG}	Operating and Storage Temperature Range		-65 to 150	°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
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* Order option J23Z for cropped center drain lead.

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			50	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.7	2	V
		T_J = 125°C	0.6	1.3	1.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 3.7 A		0.105	0.12	Ω
		T_J = 125°C		0.17	0.24	
		V_{GS} = 10 V, I_D = 3.9 A			0.1	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	10			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 3.7 A		6		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		435		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			30		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		8	20	ns
t_r	Turn - On Rise Time			4	20	ns
$t_{D(off)}$	Turn - Off Delay Time			24	50	ns
t_f	Turn - Off Fall Time			7	20	ns
Q_g	Total Gate Charge	V_{DS} = 40 V, I_D = 3.7 A, V_{GS} = 10 V		13.5	20	nC
Q_{gs}	Gate-Source Charge			1.5	3	nC
Q_{gd}	Gate-Drain Charge			4	8	nC

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Source-Drain Diode Forward Current				2.5	A
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.86	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

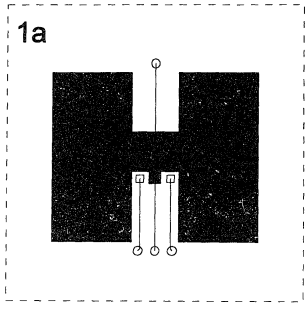
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

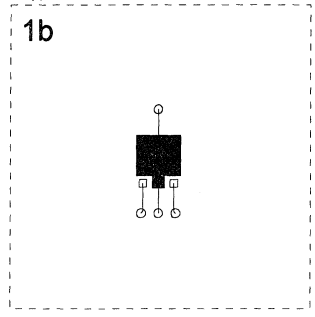
Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

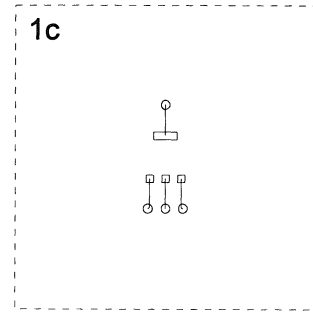
a. 42°C/W when mounted on a 1 in^2 pad of 2oz copper.

b. 95°C/W when mounted on a 0.066 in^2 pad of 2oz copper.

c. 110°C/W when mounted on a 0.0123 in^2 pad of 2oz copper.







Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics (continued)

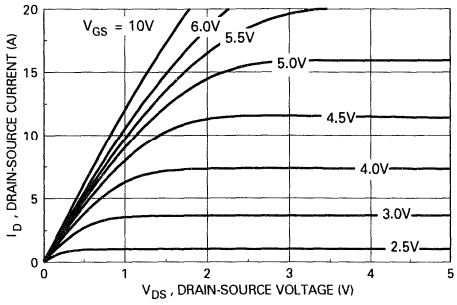


Figure 1. On-Region Characteristics.

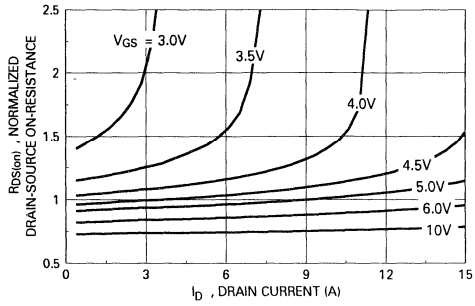


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

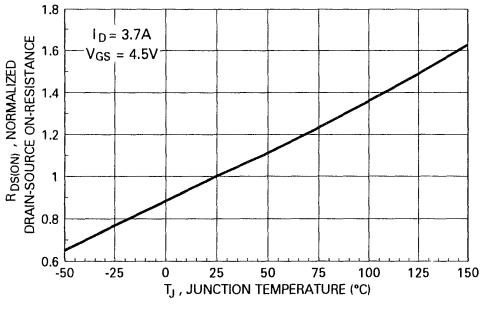


Figure 3. On-Resistance Variation with Temperature.

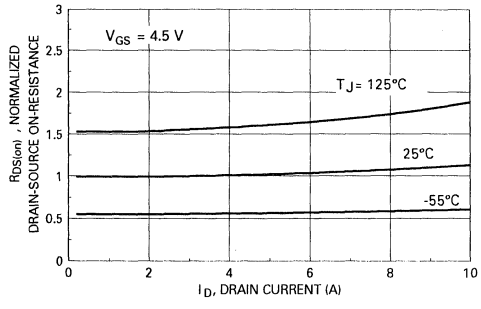


Figure 4. On-Resistance Variation with Drain Current and Temperature.

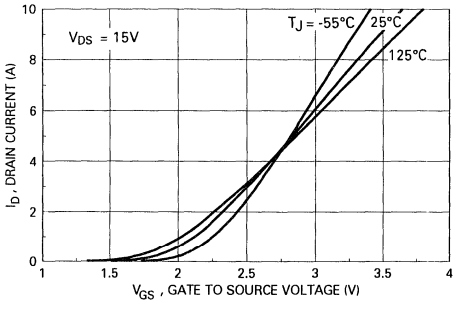


Figure 5. Transfer Characteristics

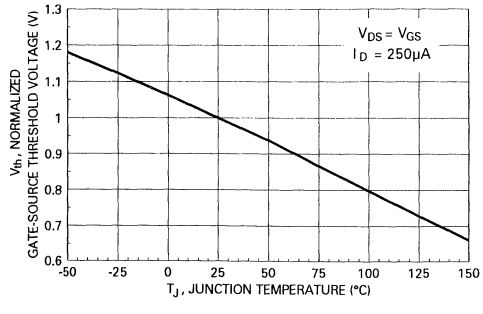


Figure 6. Gate Threshold Variation with Temperature.

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Typical Electrical Characteristics (continued)

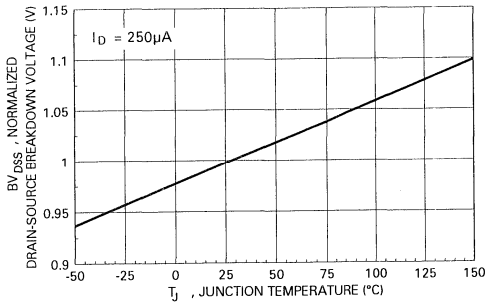


Figure 7. Breakdown Voltage Variation with Temperature.

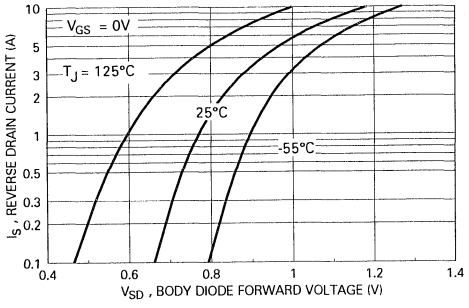


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

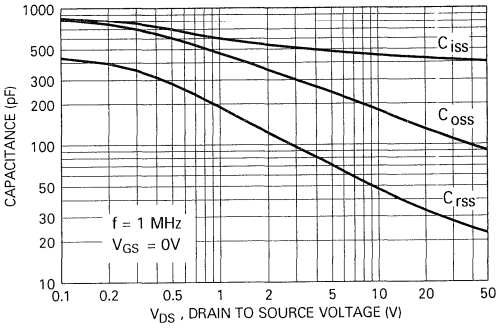


Figure 9. Capacitance Characteristics.

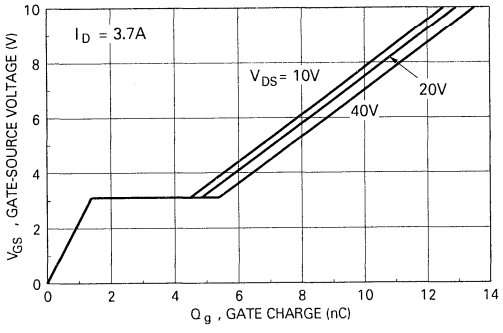


Figure 10. Gate Charge Characteristics.

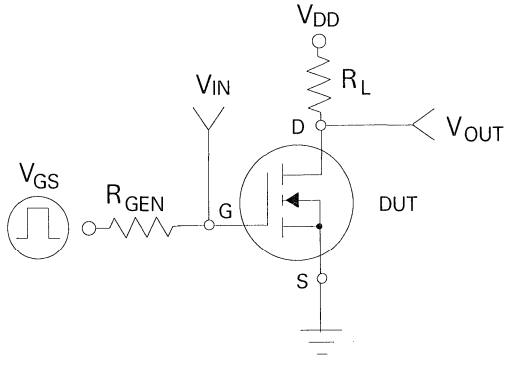


Figure 11. Switching Test Circuit

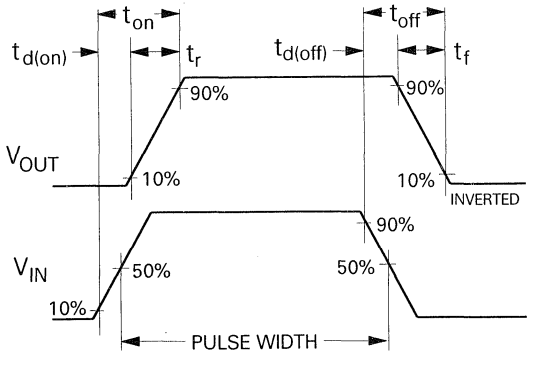


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

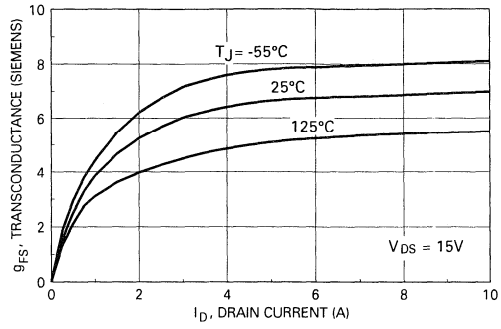


Figure 13. Transconductance Variation with Drain Current and Temperature

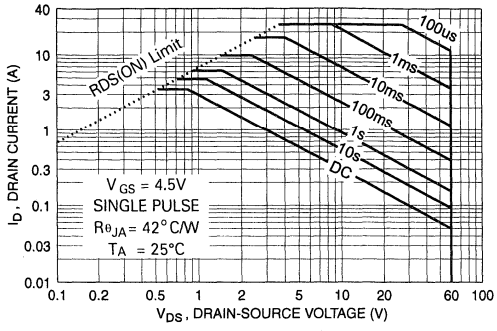


Figure 14. Maximum Safe Operating Area

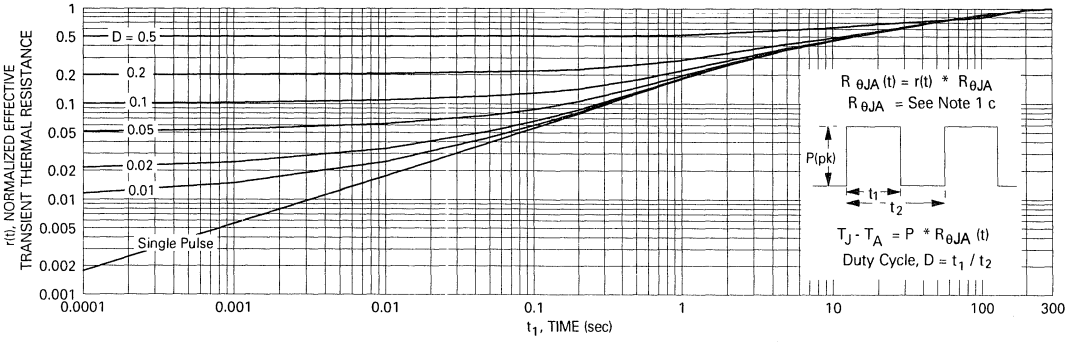


Figure 15. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

5

Section 6

SO-16 Data Sheets

National Semiconductor™

May 1996

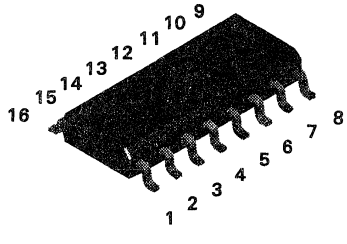
NDM3000
3 Phase Brushless Motor Driver

General Description

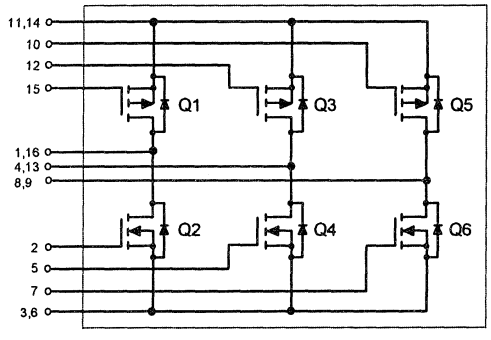
The NDM3000 three phase brushless motor driver consists of three N-Channel and P-Channel MOSFETs in a half bridge configuration. These devices are produced using National's proprietary, high cell density DMOS technology. This very high density process is tailored to minimize on-state resistance which reduces power loss, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage 3 phase motor driver such as disk drive spindle motor control and other half bridge applications.

Features

- ±3.0A, ±30V, 2.5W
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability.
- Industry standard SOIC-16 surface mount package.



SOIC-16



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	NDM3000	Units
V_{DSS}	Drain-Source Voltage (All Types)	± 30	V
V_{GSS}	Gate-Source Voltage (All Types)	± 20	V
I_D	Drain Current Q1+Q4 or Q1+Q6 or Q3+Q2 - Continuous Q3+Q6 or Q5+Q2 or Q5+Q4	± 3.0	A
	- Pulsed (Note 1a & 2)	± 10	
P_D	Total Power Dissipation (Note 1a) Q1+Q4 or Q1+Q6 or Q3+Q2 or (Note 1b) Q3+Q6 or Q5+Q2 or Q5+Q4	2.5	W
		1.6	
	(Note 1c)	1.4	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C

THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient Q1+Q4 or Q1+Q6 or Q3+Q2 or Q3+Q6 or Q5+Q2 or Q5+Q4 (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case Q1+Q4 or Q1+Q6 or Q3+Q2 or Q3+Q6 or Q5+Q2 or Q5+Q4 (Note 1)	20	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = ± 250 µA	All	±30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = ±20 V, V_{GS} = 0 V	All			±1	µA
		T_J=55°C				±25	µA
I_{GSS}	Gate - Body Leakage, Forward	V_{GS} = ±20 V, V_{DS} = 0 V	All			±100	nA
ON CHARACTERISTICS (Note 3)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	Q1, Q3, Q5	-1	-1.6	-3	V
		T_J=125°C		-0.7	-1.25	-2.2	
		V_{DS} = V_{GS}, I_D = 250 µA	Q2, Q4, Q6	1	1.7	3	
		T_J=125°C		0.7	1.2	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -3.0 A	Q1, Q3, Q5		0.125	0.16	Ω
		T_J=125°C			0.18	0.29	
		V_{GS} = -4.5 V, I_D = -1.0 A			0.16	0.25	
		V_{GS} = 10 V, I_D = 3.0 A	Q2, Q4, Q6		0.07	0.09	
		T_J=125°C			0.1	0.16	
		V_{GS} = 4.5 V, I_D = 1.0 A			0.09	0.13	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -5 V	Q1, Q3, Q5	-10			A
		V_{GS} = 10 V, V_{DS} = 5 V	Q2, Q4, Q6	10			
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1, Q3, Q5 V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1, Q3, Q5		375		pF
			Q2, Q4, Q6		360		
C_{oss}	Output Capacitance	Q2, Q4, Q6 V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	Q1, Q3, Q5		245		pF
			Q2, Q4, Q6		260		
C_{rss}	Reverse Transfer Capacitance		Q1, Q3, Q5		130		pF
			Q2, Q4, Q6		105		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 3)							
$t_{D(on)}$	Turn - On Delay Time	Q1, Q3, Q5 V_{DD} = -15 V, I_D = -1 A, V_{GEN} = -10 V, R_{GEN} = 6 Ω	Q1, Q3, Q5		10	40	ns
			Q2, Q4, Q6		9	40	
t_r	Turn - On Rise Time		Q1, Q3, Q5		13	40	ns
			Q2, Q4, Q6		21	40	
$t_{D(off)}$	Turn - Off Delay Time	Q2, Q4, Q6 V_{DD} = 15 V, I_D = 1 A, V_{GEN} = 10 V, R_{GEN} = 6 Ω	Q1, Q3, Q5		21	90	ns
			Q2, Q4, Q6		21	90	
t_f	Turn - Off Fall Time		Q1, Q3, Q5		5	50	ns
			Q2, Q4, Q6		8	50	
Q_g	Total Gate Charge	Q1, Q3, Q5 V_{DS} = -10 V, I_D = -3.0 A, V_{GS} = -10 V	Q1, Q3, Q5		10	25	nC
			Q2, Q4, Q6		9.5	25	
Q_{gs}	Gate-Source Charge	Q2, Q4, Q6 V_{DS} = 10 V, I_D = 3.0 A, V_{GS} = 10 V	Q1, Q3, Q5		1.6		nC
			Q2, Q4, Q6		1.5		
Q_{gd}	Gate-Drain Charge		Q1, Q3, Q5		3		nC
			Q2, Q4, Q6		2.5		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1, Q3, Q5			-1.2	A
			Q2, Q4, Q6			1.2	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -3.0 A (Note 3)	Q1, Q3, Q5		-0.8	-1.3	V
		V_{GS} = 0 V, I_S = 3.0 A (Note 3)	Q2, Q4, Q6		0.8	1.3	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = ±3.0 A, dI_F/dt = 100 A/µs	All			100	ns

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

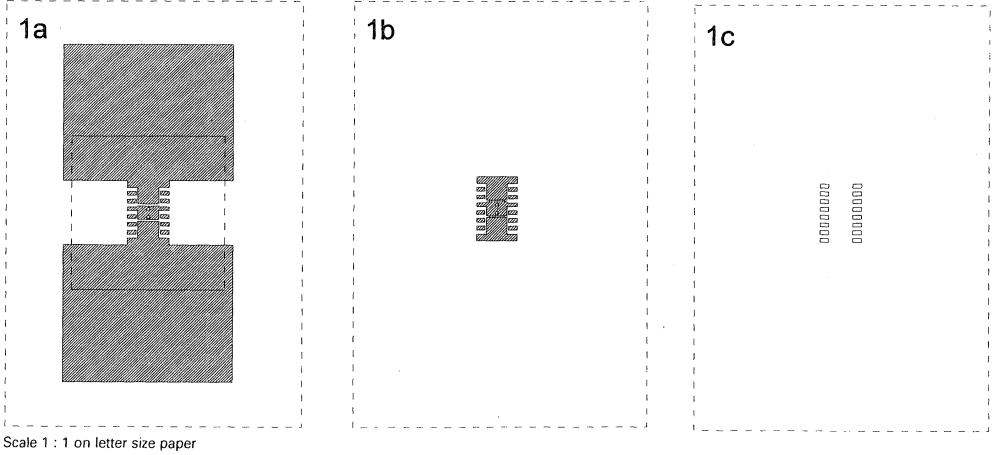
$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ using the board layouts shown below on 4.5"x5" FR-4 PCB in a still air environment:

a. 50°C/W when mounted on a 1 in^2 pad of 2oz cpper.

b. 80°C/W when mounted on a 0.027 in^2 pad of 2oz cpper.

c. 90°C/W when mounted on a 0.0028 in^2 pad of 2oz cpper.



Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

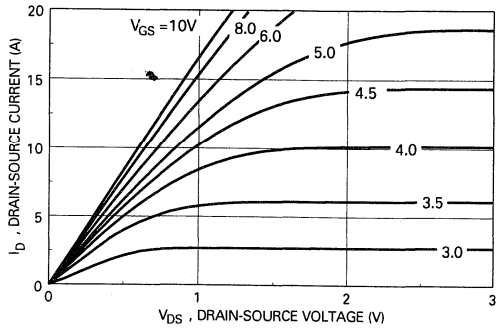


Figure 1. N-Channel On-Region Characteristic.

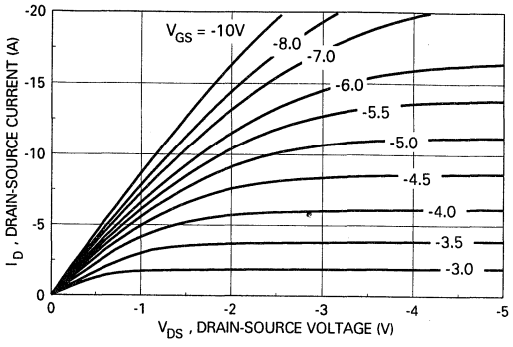


Figure 2. P-Channel On-Region Characteristics.

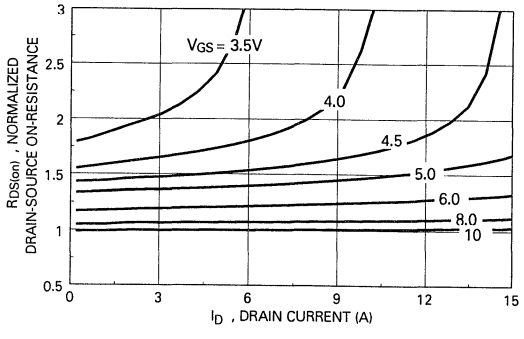


Figure 3. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

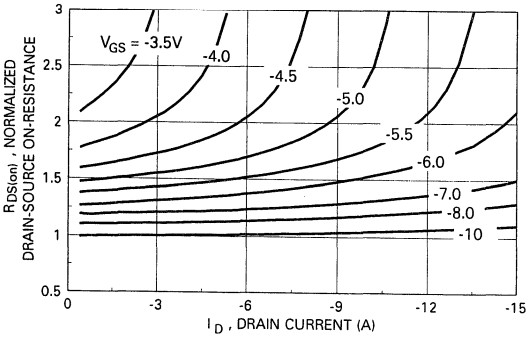


Figure 4. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

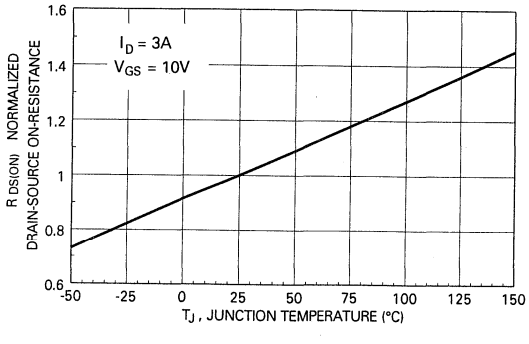


Figure 5. N-Channel On-Resistance Variation with Temperature.

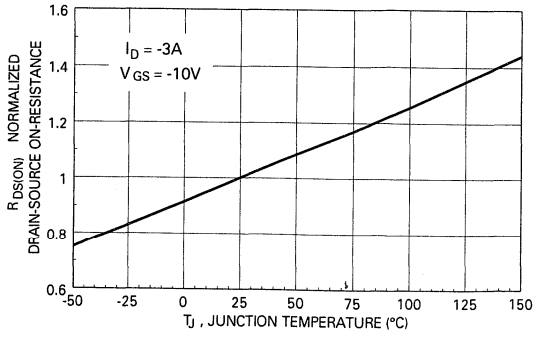


Figure 6. P-Channel On-Resistance Variation with Temperature.

Typical Electrical Characteristics

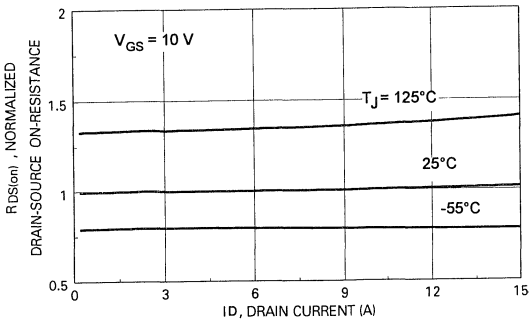


Figure 7. N-Channel On-Resistance Variation with Drain Current and Temperature.

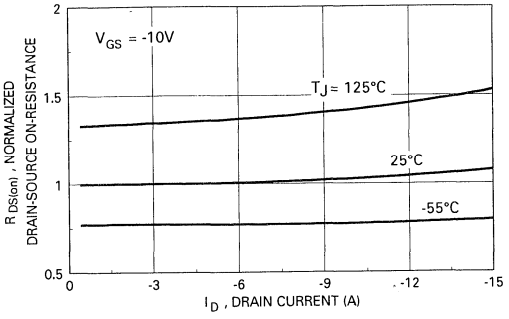


Figure 8. P-Channel On-Resistance Variation with Drain Current and Temperature.

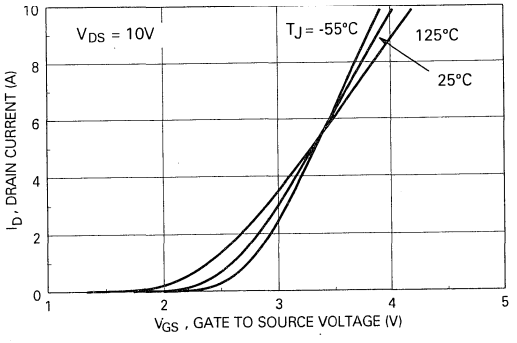


Figure 9. N-Channel Transfer Characteristics.

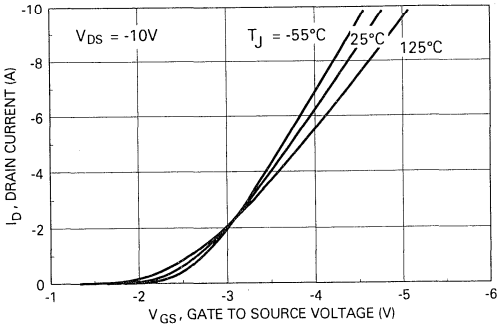


Figure 10. P-Channel Transfer Characteristics.

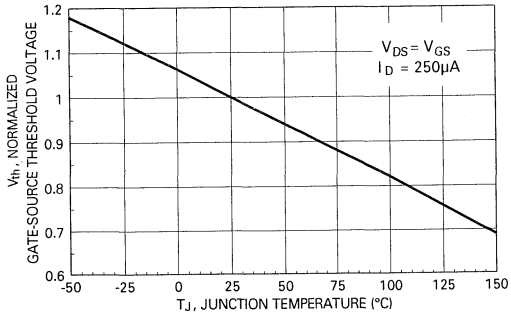


Figure 11. N-Channel Gate Threshold Variation with Temperature.

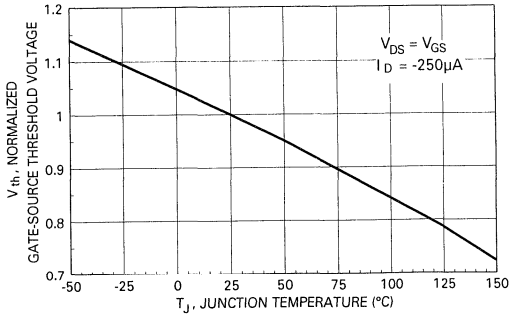


Figure 12. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics

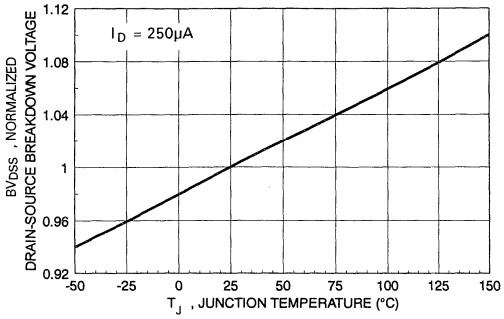


Figure 13. N-Channel Breakdown Voltage Variation with Temperature.

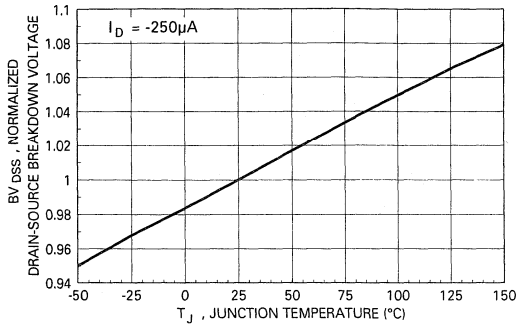


Figure 14. P-Channel Breakdown Voltage Variation with Temperature.

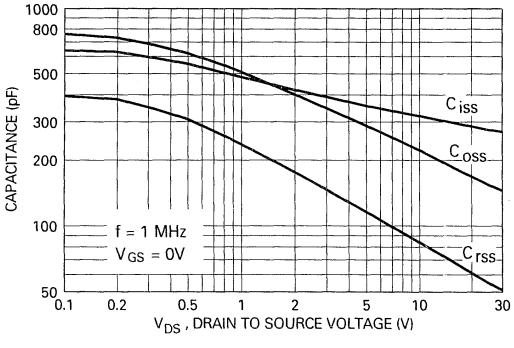


Figure 15. N-Channel Capacitance Characteristics.

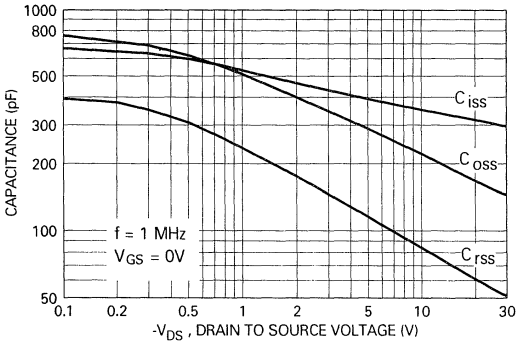


Figure 16. P-Channel Capacitance Characteristics.

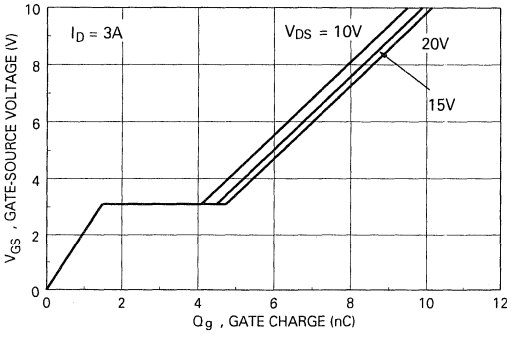


Figure 17. N-Channel Gate Charge Characteristics.

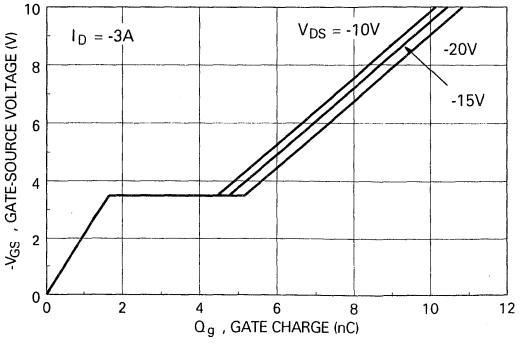


Figure 18. P-Channel Gate Charge Characteristics.

6

Typical Electrical Characteristics

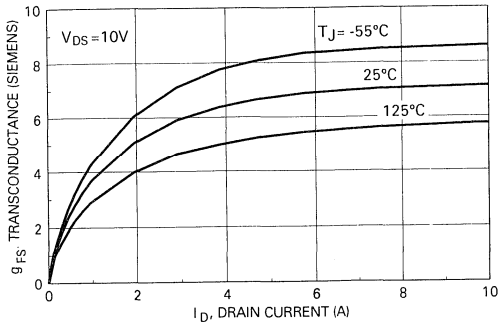


Figure 19. N-Channel Transconductance Variation with Drain Current and Temperature.

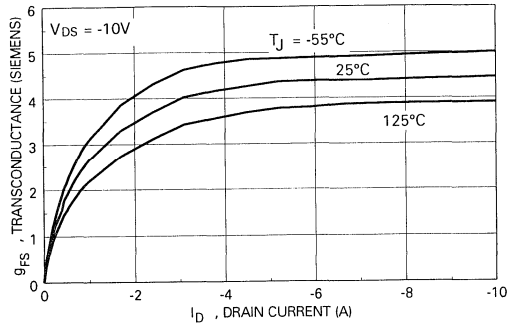


Figure 20. P-Channel Transconductance Variation with Drain Current and Temperature.

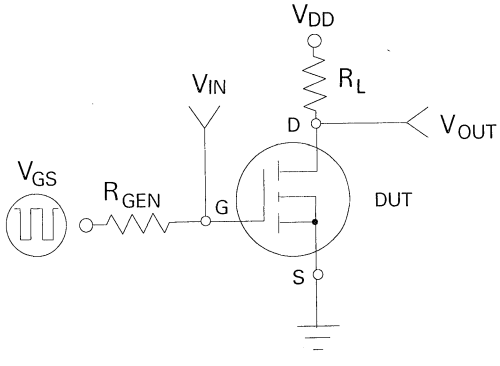


Figure 21. N or P-Channel Switching Test Circuit.

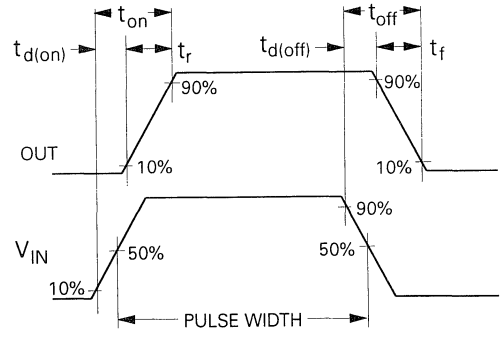


Figure 22. N or P-Channel Switching Waveforms.

Typical Thermal and Electrical Characteristics

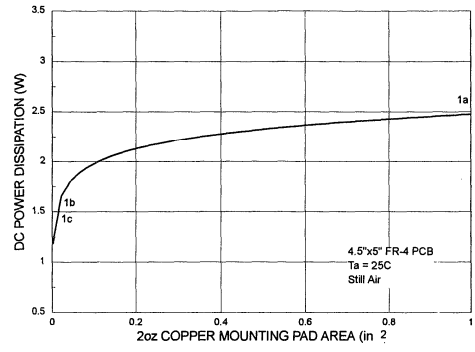


Figure 23. SOIC-16 3 Leadframe Device DC Power Dissipation versus Copper Mounting Pad Area

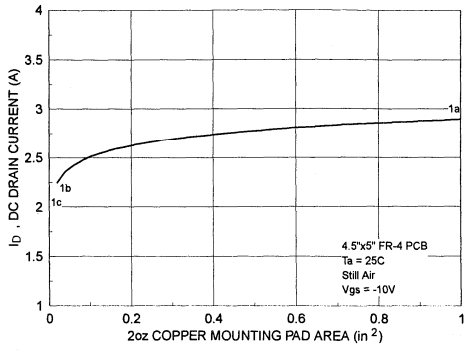


Figure 24. P-Ch DC Drain Current Capability versus Copper Mounting Pad Area.

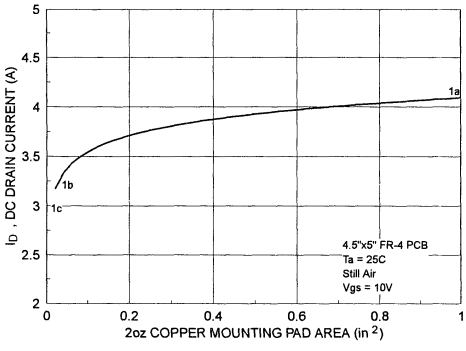


Figure 25. N-Ch DC Drain Current Capability versus Copper Mounting Pad Area.

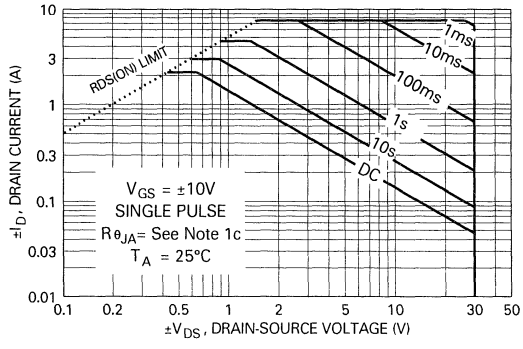


Figure 26. P-Ch Typical Safe Operating Area

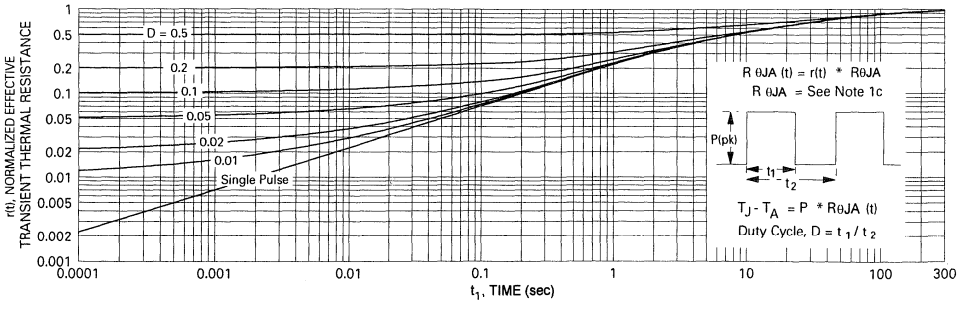


Figure 27. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note 1c. Transient thermal response will change depending on the circuit board design.

Section 7

SOT-23 / TO-92 Data Sheets

National Semiconductor™

November 1995

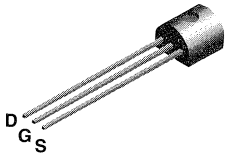
2N7000 / 2N7002 / NDS7002A
N-Channel Enhancement Mode Field Effect Transistor

General Description

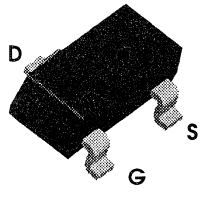
These N-Channel enhancement mode field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 400mA DC and can deliver pulsed currents up to 2A. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

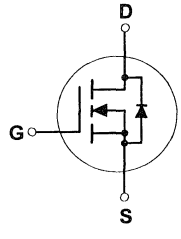
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



TO-92
2N7000



SOT-23
(TO-236AB)
2N7002 / NDS7002A



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	2N7000	2N7002	NDS7002A	Units
V_{DSS}	Drain-Source Voltage		60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)		60		V
V_{GSS}	Gate-Source Voltage - Continuous		±20		V
	- Non Repetitive (tp < 50μs)		±40		
I_D	Maximum Drain Current - Continuous	200	115	280	mA
	- Pulsed	500	800	1500	
P_D	Maximum Power Dissipation	400	200	300	mW
	Derated above 25°C	3.2	1.6	2.4	mW/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		-65 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds		300		°C
THERMAL CHARACTERISTICS					
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	312.5	625	417	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	2N7000			1	µA
		T_J=125°C				1	mA
		V_{DS} = 60 V, V_{GS} = 0 V	2N7002 NDS7002			1	µA
		T_J=125°C				0.5	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15 V, V_{DS} = 0 V	2N7000			10	nA
		V_{GS} = 20 V, V_{DS} = 0 V	2N7002 NDS7002			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -15 V, V_{DS} = 0 V	2N7000			-10	nA
		V_{GS} = -20 V, V_{DS} = 0 V	2N7002 NDS7002			-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	2N7000	0.8	2.1	3	V
		V_{DS} = V_{GS}, I_D = 250 µA	2N7002 NDS7002	1	2.1	2.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA	2N7000		1.2	5	Ω
		T_J =125°C			1.9	9	
		V_{GS} = 4.5 V, I_D = 75 mA			1.8	5.3	
		V_{GS} = 10 V, I_D = 500 mA	2N7002		1.2	7.5	
		T_J =100°C			1.7	13.5	
		V_{GS} = 5.0 V, I_D = 50 mA			1.7	7.5	
		T_J =100C			2.4	13.5	
		V_{GS} = 10 V, I_D = 500 mA	NDS7002		1.2	2	
		T_J =125°C			2	3.5	
		V_{GS} = 5.0 V, I_D = 50 mA			1.7	3	
		T_J =125°C			2.8	5	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA	2N7000		0.6	2.5	V
		V_{GS} = 4.5 V, I_D = 75 mA			0.14	0.4	
		V_{GS} = 10 V, I_D = 500mA	2N7002		0.6	3.75	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	1.5	
		V_{GS} = 10 V, I_D = 500mA	NDS7002		0.6	1	
		V_{GS} = 5.0 V, I_D = 50 mA			0.09	0.15	

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
ON CHARACTERISTICS Continued (Note 1)							
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V	2N7000	75	600		mA
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	2N7002	500	2700		
		V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	NDS7002	500	2700		
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	2N7000	100	320		mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	2N7002	80	320		
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	NDS7002	80	320		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All		20	50	pF
C_{oss}	Output Capacitance		All		11	25	pF
C_{rss}	Reverse Transfer Capacitance		All		4	5	pF
t_{on}	Turn-On Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 25	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	2N700 NDS7002			20	
t_{off}	Turn-Off Time	V_{DD} = 15 V, R_L = 25 Ω, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 25	2N7000			10	ns
		V_{DD} = 30 V, R_L = 150 Ω, I_D = 200 mA, V_{GS} = 10 V, R_{GEN} = 25 Ω	2N700 NDS7002			20	
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		2N7002			115	mA
			NDS7002			280	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		2N7002			0.8	A
			NDS7002			1.5	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 11.5 mA (Note 1)	2N7002		0.88	1.5	V
		V_{GS} = 0 V, I_S = 400 mA (Note 1)	NDS7002		0.88	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

2N7000 / 2N7002 / NDS7002A

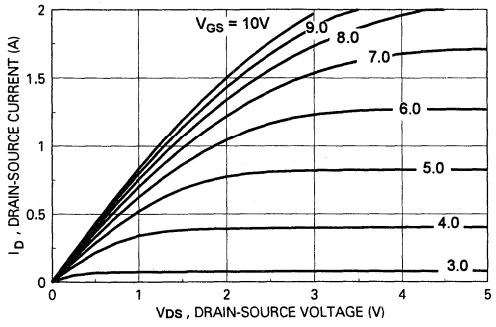


Figure 1. On-Region Characteristics

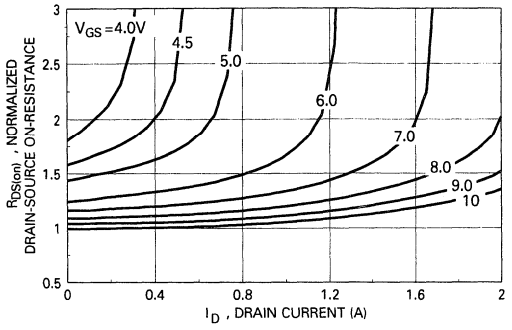


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

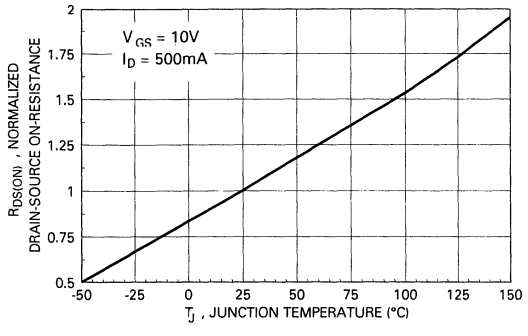


Figure 3. On-Resistance Variation with Temperature

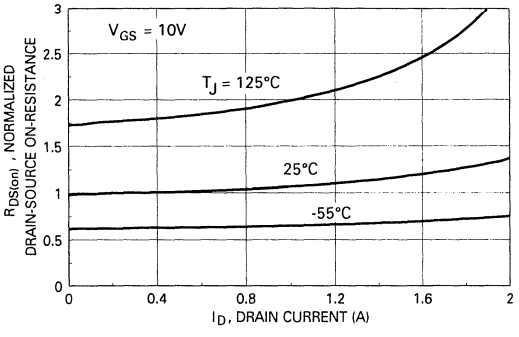


Figure 4. On-Resistance Variation with Drain

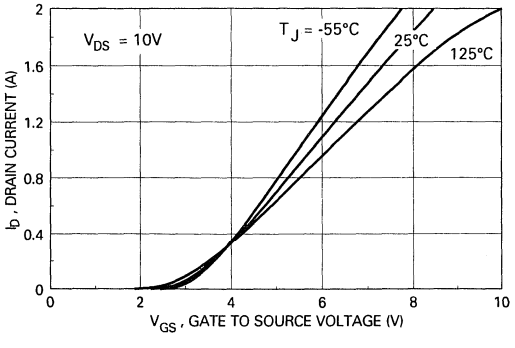


Figure 5. Transfer Characteristics

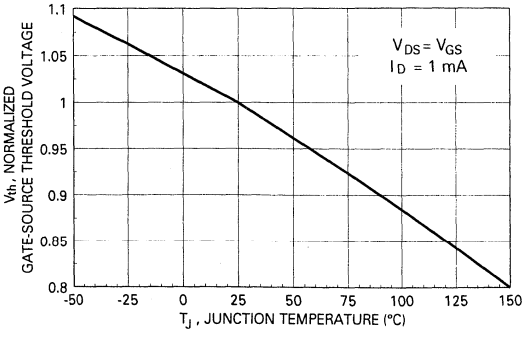


Figure 6. Gate Threshold Variation with Temperature

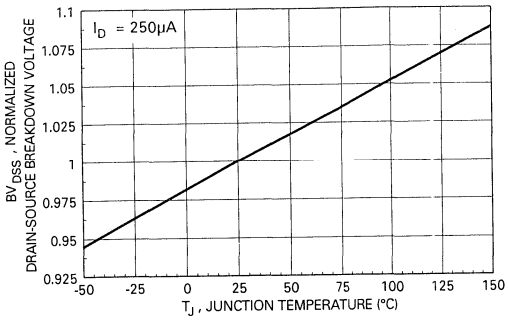


Figure 7. Breakdown Voltage Variation with Temperature

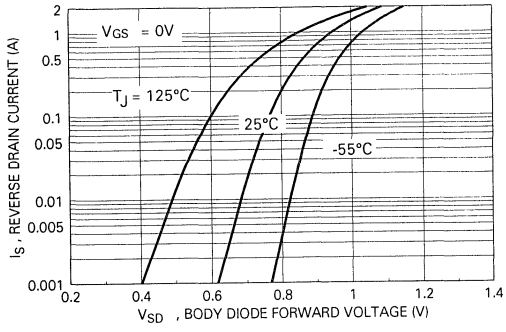


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

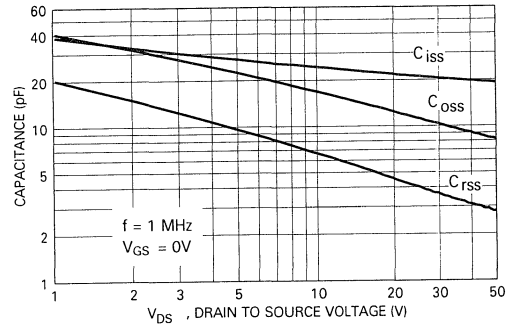


Figure 9. Capacitance Characteristics

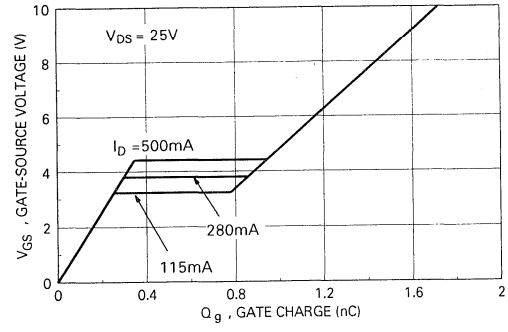


Figure 10. Gate Charge Characteristics

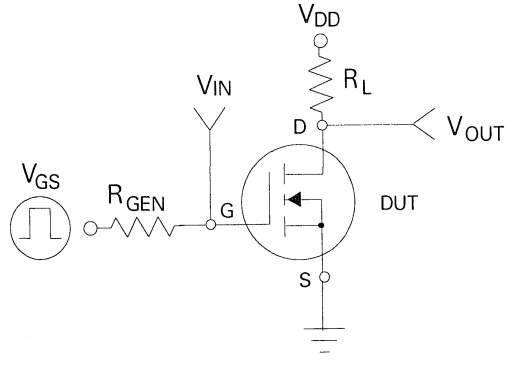


Figure 11. Switching Test Circuit

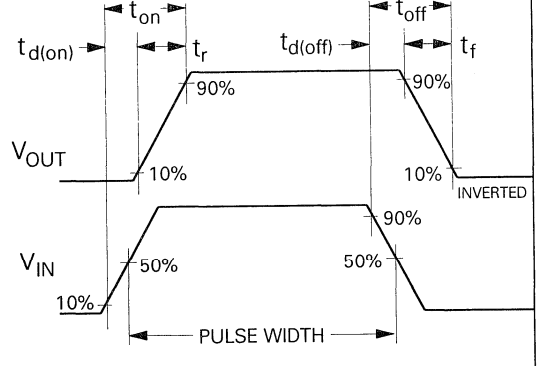


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

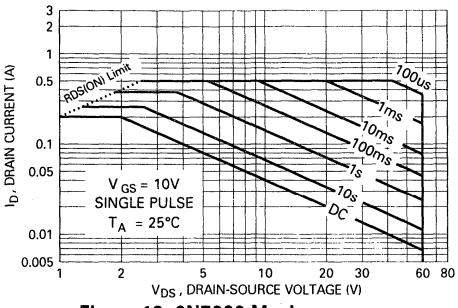


Figure 13. 2N7000 Maximum Safe Operating Area

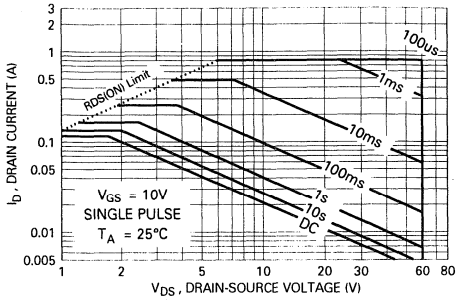


Figure 14. 2N7002 Maximum Safe Operating Area

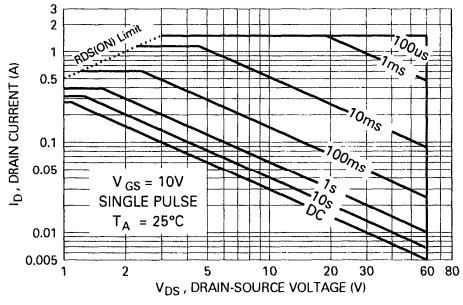


Figure 15. NDS7000A Maximum Safe Operating Area

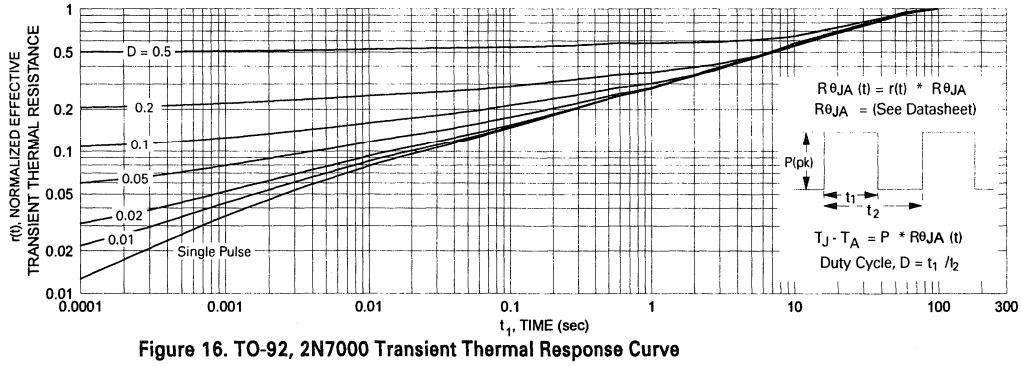


Figure 16. TO-92, 2N7000 Transient Thermal Response Curve

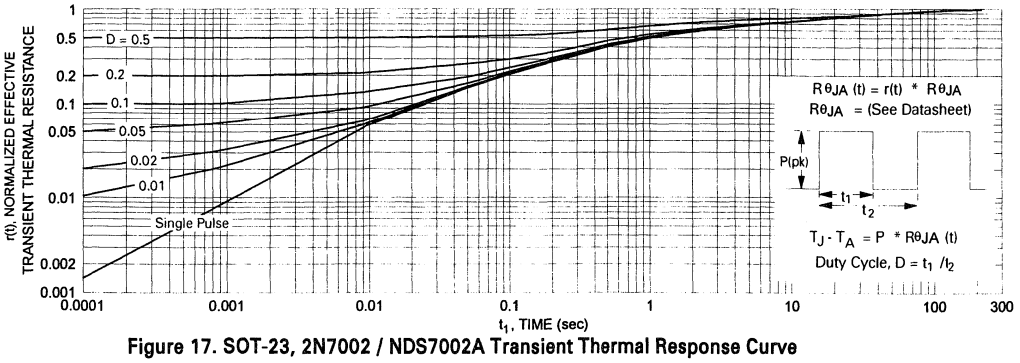


Figure 17. SOT-23, 2N7002 / NDS7002A Transient Thermal Response Curve

7

National Semiconductor™

April 1995

BS170 / MMBF170

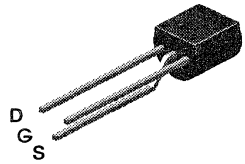
N-Channel Enhancement Mode Field Effect Transistor

General Description

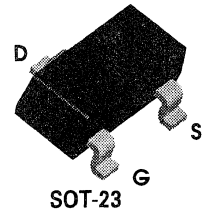
These N-Channel enhancement mode field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

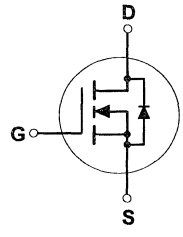
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



TO-92 (97)
BS170



SOT-23
(TO-236AB)
MMBF170



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	BS170	MMBF170	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$)	60		V
V_{GSS}	Gate-Source Voltage	± 20		V
I_D	Drain Current - Continuous	500	500	mA
	- Pulsed	1200	800	
P_D	Maximum Power Dissipation	830	300	mW
	Derate Above 25°C	6.6	2.4	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistacne, Junction-to-Ambient	150	417	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 100 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 25 V, V_{GS} = 0 V	All			0.5	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 15 V, V_{DS} = 0 V	All			10	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	All	0.8	2.1	3	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 200 mA	All		1.2	5	Ω
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 200 mA	BS170		320		mS
		$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	MMBF170		320		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	All		24	40	pF
C_{oss}	Output Capacitance		All		17	30	pF
C_{rss}	Reverse Transfer Capacitance		All		7	10	pF
SWITCHING CHARACTERISTICS (Note 1)							
t_{on}	Turn-On Time	V_{DD} = 25 V, I_D = 200 m A, V_{GS} = 10 V, R_{GEN} = 25 Ω	BS170			10	ns
		V_{DD} = 25 V, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 50 Ω	MMBF170			10	
t_{off}	Turn-Off Time	V_{DD} = 25 V, I_D = 200 m A, V_{GS} = 10 V, R_{GEN} = 25 Ω	BS170			10	ns
		V_{DD} = 25 V, I_D = 500 mA, V_{GS} = 10 V, R_{GEN} = 50 Ω	MMBF170			10	

Note:
1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

BS170 / MMBF170

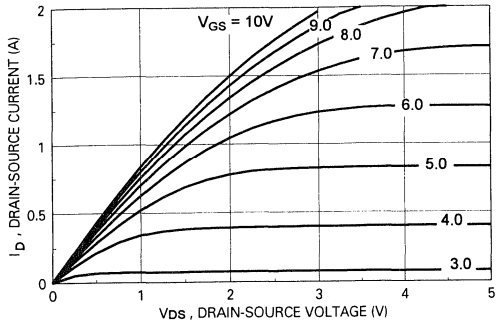


Figure 1. On-Region Characteristics

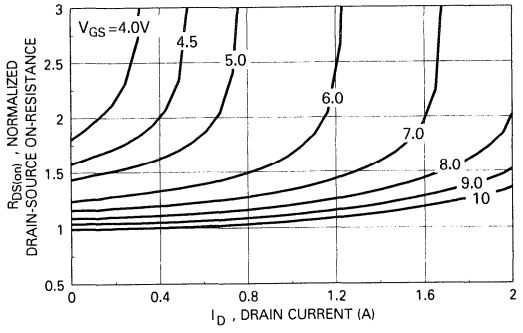


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

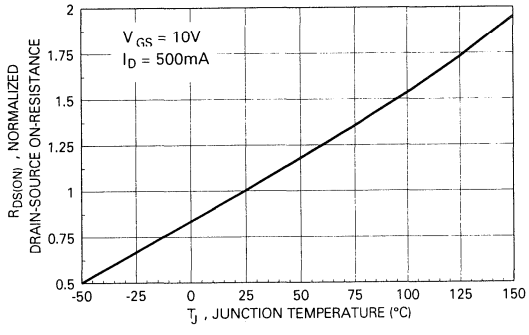


Figure 3. On-Resistance Variation with Temperature

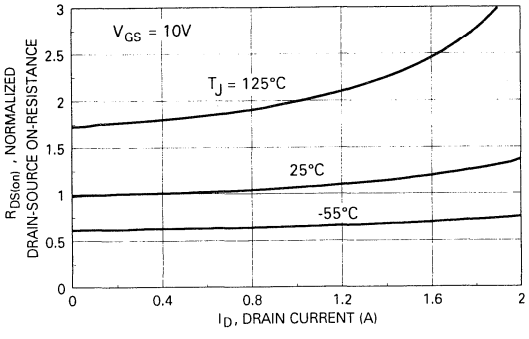


Figure 4. On-Resistance Variation with Drain Current and Temperature

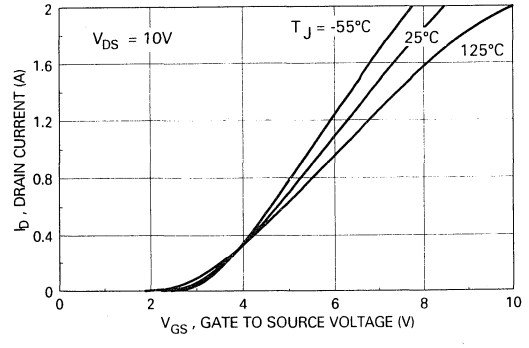


Figure 5. Transfer Characteristics

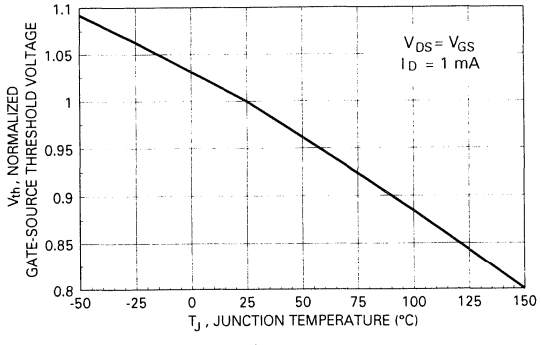


Figure 6. Gate Threshold Variation with Temperature

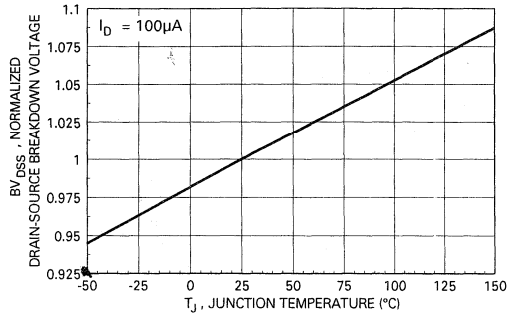


Figure 7. Breakdown Voltage Variation with Temperature

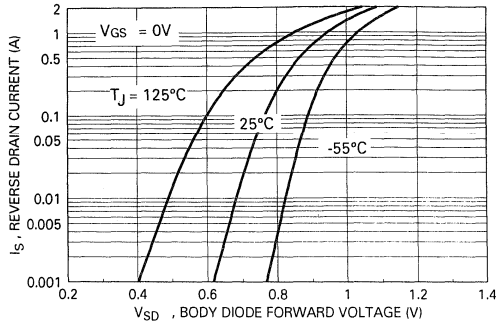


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

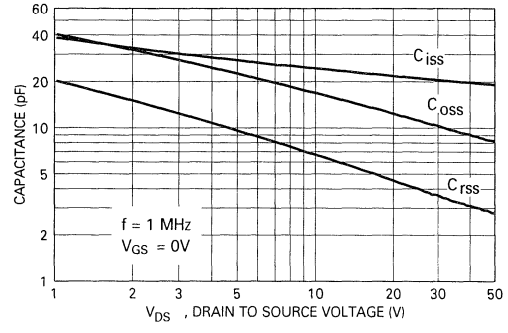


Figure 9. Capacitance Characteristics

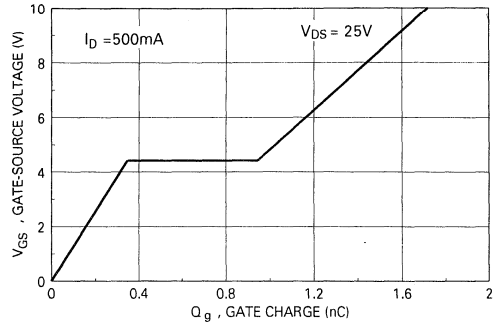


Figure 10. Gate Charge Characteristics

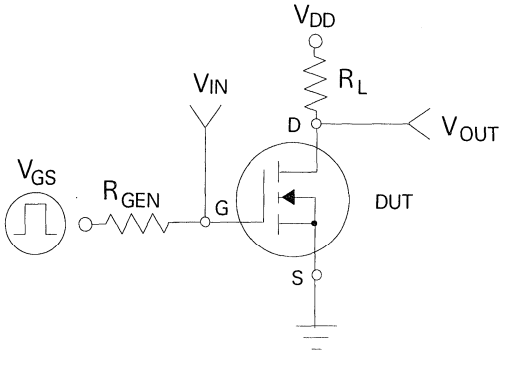


Figure 11. Switching Test Circuit

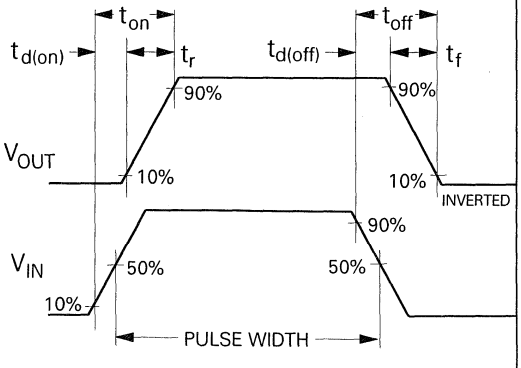


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

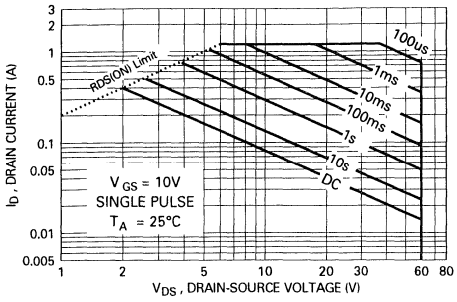


Figure 13. BS170 Maximum Safe Operating Area

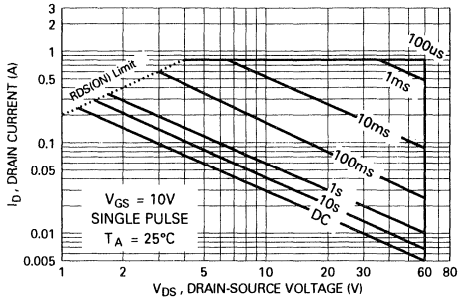


Figure 14. MMBF170 Maximum Safe Operating Area

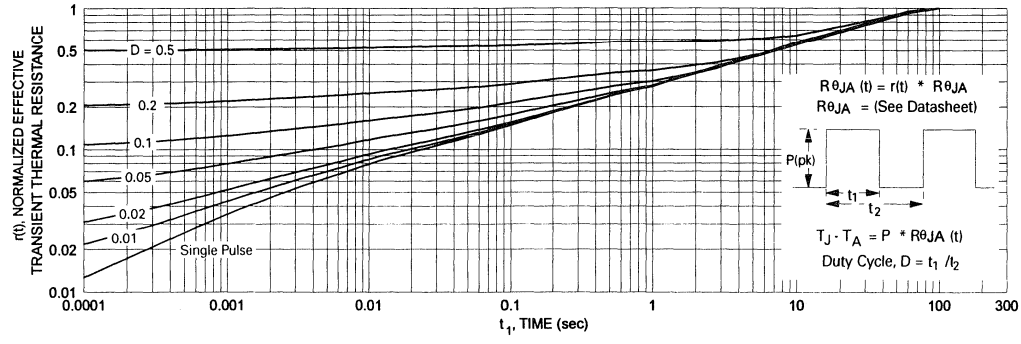


Figure 15. TO-92, BS170 Transient Thermal Response Curve

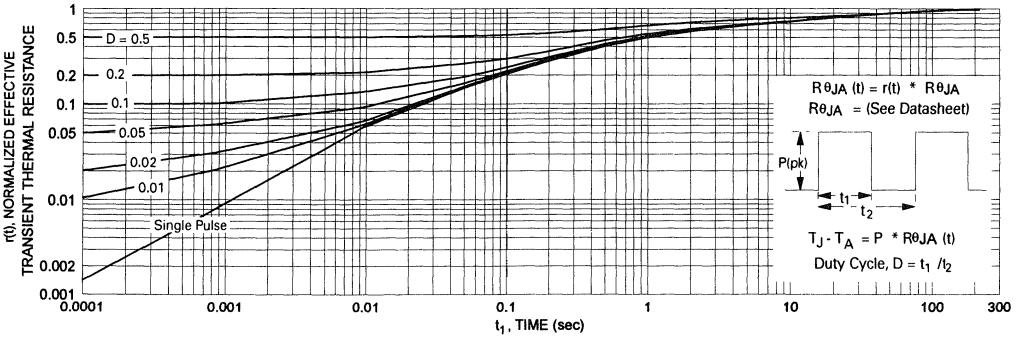


Figure 16. SOT-23, MMBF170 Transient Thermal Response Curve

National Semiconductor™

April 1995

BS270

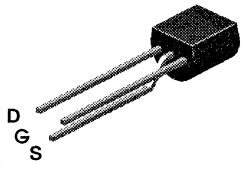
N-Channel Enhancement Mode Field Effect Transistor

General Description

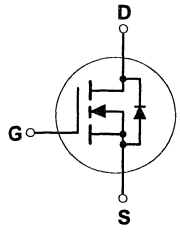
These N-Channel enhancement mode field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. They can be used in most applications requiring up to 500mA DC. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- 400mA, 60V. $R_{DS(ON)}$ = 2Ω @ V_{GS} = 10V.
- High density cell design for low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.
- High saturation current capability.



TO-92 (97)
BS270



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	BS270	Units
V_{DSS}	Drain-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1M\Omega$)	60	V
V_{GSS}	Gate-Source Voltage - Continuous	±20	V
	- Non Repetitive (tp < 50μs)	±40	
I_D	Drain Current - Continuous	400	mA
	- Pulsed	2000	
P_D	Maximum Power Dissipation	625	mW
	Derate Above 25°C	5	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistacne, Junction-to-Ambient	200	°C/W

7

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 10 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		T_J = 125°C			500	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			10	nA
I_{GSSF}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-10	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	2.1	2.5	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 500 mA		1.2	2	Ω
		T_J = 125°C		2	3.5	
		V_{GS} = 4.5 V, I_D = 75 mA		1.8	3	
$V_{DS(ON)}$	Drain-Source On-Voltage	V_{GS} = 10 V, I_D = 500 mA		0.6	1	V
		V_{GS} = 4.5 V, I_D = 75 mA		0.14	0.225	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = 10 V, $V_{DS} \geq 2\ V_{DS(on)}$	2000	2700		mA
		V_{GS} = 4.5 V, $V_{DS} \geq 2\ V_{DS(on)}$	400	600		
g_{FS}	Forward Transconductance	$V_{DS} \geq 2\ V_{DS(on)}$, I_D = 200 mA	100	320		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		20	50	pF
C_{oss}	Output Capacitance			11	25	pF
C_{rss}	Reverse Transfer Capacitance			4	5	pF
SWITCHING CHARACTERISTICS (Note 1)						
t_{on}	Turn-On Time	V_{DD} = 30 V, I_D = 500 m A, V_{GS} = 10 V, R_{GEN} = 25 Ω			10	ns
t_{off}	Turn-Off Time				10	ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				400	mA
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				2000	mA
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 400 mA (Note 1)		0.88	1.2	V

Note:
1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

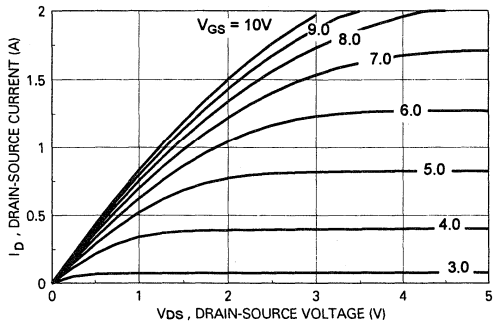


Figure 1. On-Region Characteristics

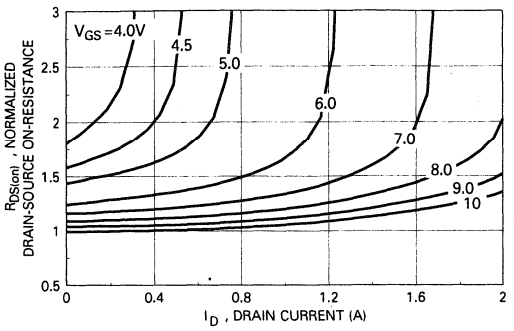


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

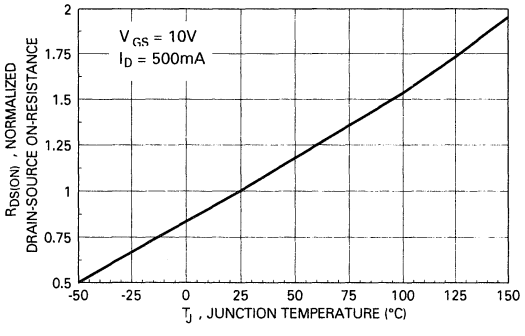


Figure 3. On-Resistance Variation with Temperature

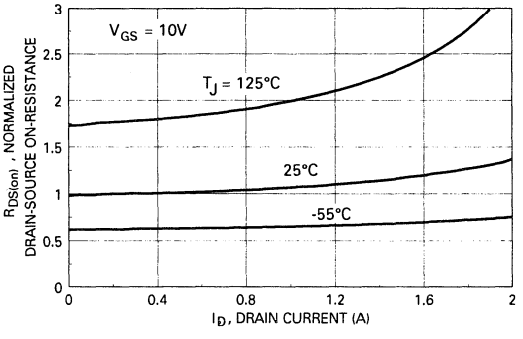


Figure 4. On-Resistance Variation with Drain

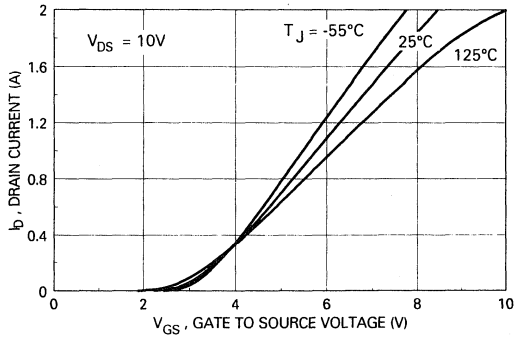


Figure 5. Transfer Characteristics

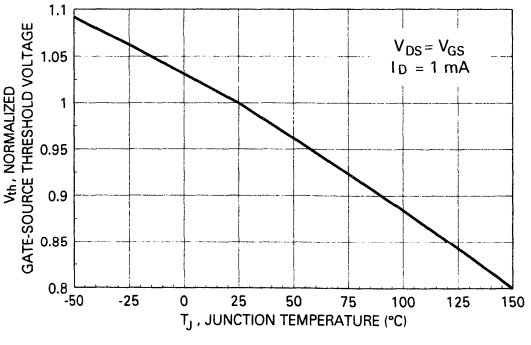


Figure 6. Gate Threshold Variation with Temperature

7

Typical Electrical Characteristics (continued)

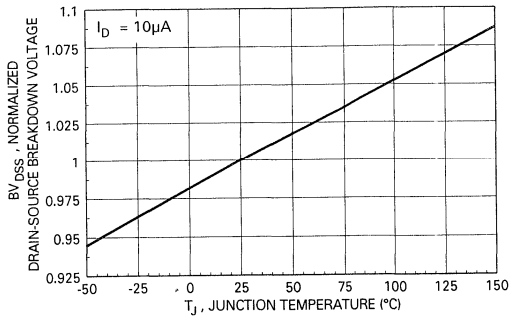


Figure 7. Breakdown Voltage Variation with Temperature

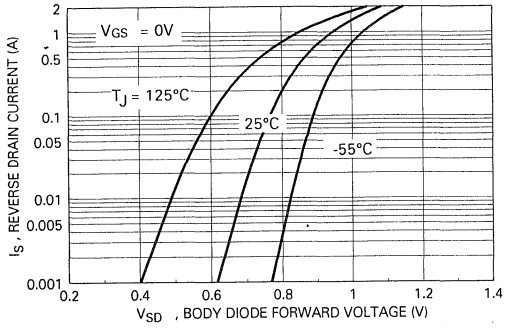


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

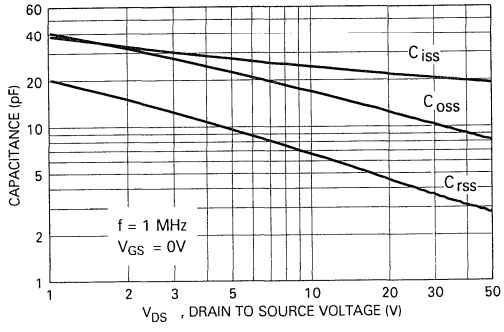


Figure 9. Capacitance Characteristics

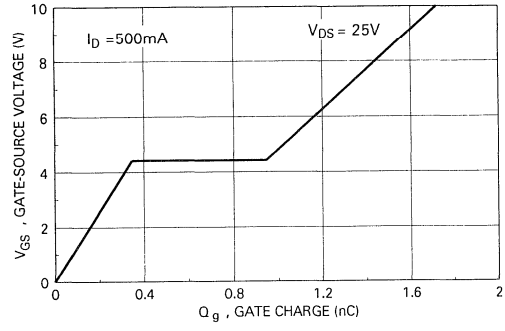


Figure 10. Gate Charge Characteristics

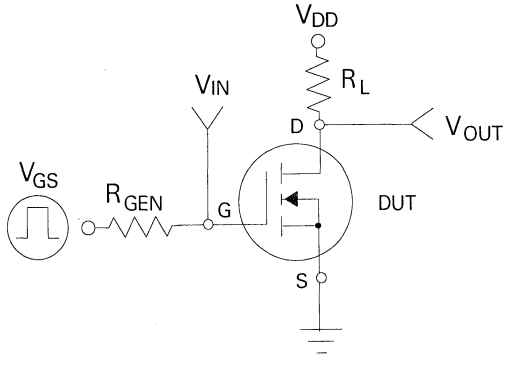


Figure 11. Switching Test Circuit

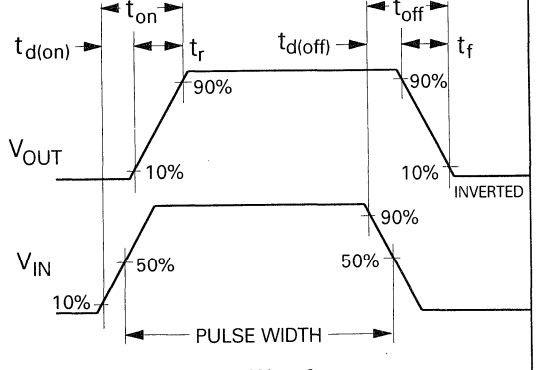


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

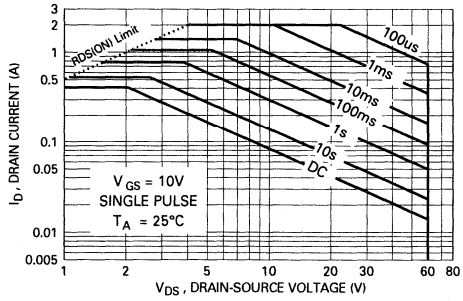


Figure 13. Maximum Safe Operating Area

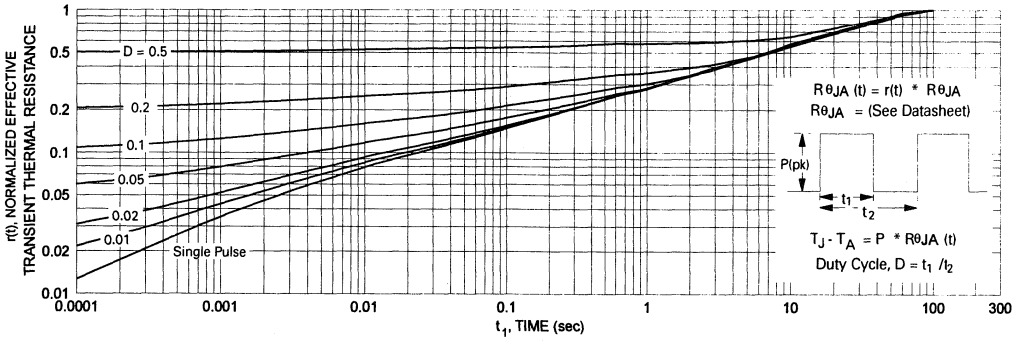


Figure 14. Transient Thermal Response Curve

7

National Semiconductor™

June 1995

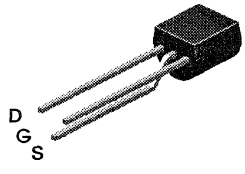
BSS84 / BSS110
P-Channel Enhancement Mode Field Effect Transistor

General Description

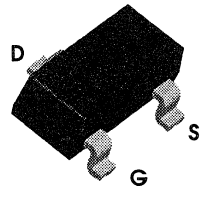
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 0.17A DC and can deliver pulsed currents up to 0.68A. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

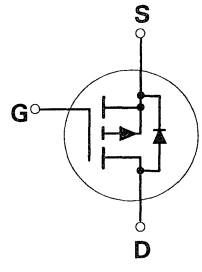
- BSS84: -0.13A, -50V. $R_{DS(ON)}$ = 10Ω @ V_{GS} = -10V.
  BSS110: -0.17A, -50V. $R_{DS(ON)}$ = 10Ω @ V_{GS} = -10V
- Voltage controlled p-channel small signal switch.
- High density cell design for low $R_{DS(ON)}$.
- High saturation current.



TO-92 (97)
BSS110



SOT-23
(TO-236AB)
BSS84



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	BSS84	BSS110	Units
V_{DSS}	Drain-Source Voltage	-50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq$ 20 KΩ)	-50		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
I_D	Drain Current - Continuous @ T_A = 30/35°C	-0.13	-0.17	A
	- Pulsed @ T_A = 25°C	-0.52	-0.68	
P_D	Maximum Power Dissipation T_A = 25°C	0.36	0.63	mW
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
T_L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	300		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	350	200	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	All	-50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -50 V, V_{GS} = 0 V	All			-15	µA
		V_{DS} = -50 V, V_{GS} = 0 V, T_J = 125°C				-60	µA
		V_{DS} = -25 V, V_{GS} = 0 V				-0.1	µA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-10	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -1 mA	All	-0.8	-1.75	-2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.13 A	BSS84		2.3	10	Ω
		V_{GS} = -10 V, I_D = -0.17 A	BSS110		2.2	10	
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -0.13 A	BSS84	0.05	0.27		S
		V_{DS} = -10 V, I_D = -0.17 A	BSS110	0.05	0.29		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	BSS84		37	45	pF
			BSS110		37	40	
C_{oss}	Output Capacitance		All		16	25	pF
C_{rss}	Reverse Transfer Capacitance		All		5	12	pF
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -30 V, I_D = -0.27 A, V_{GS} = -10 V, R_{GEN} = 50 Ω	All			12	nS
t_r	Turn - On Rise Time		All			50	nS
$t_{D(off)}$	Turn - Off Delay Time		All			10	nS
t_f	Turn - Off Fall Time		All			25	nS
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Continuous Source Diode Current		BSS84			-0.13	A
			BSS110			-0.17	
I_{SM}	Maximum Pulsed Source Diode Current (Note 1)		BSS84			-0.52	A
			BSS110			-0.68	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.26 A (Note 1)	BSS84		-0.95	-1.2	V
		V_{GS} = 0 V, I_S = -0.34 A (Note 1)	BSS110		-1	-1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

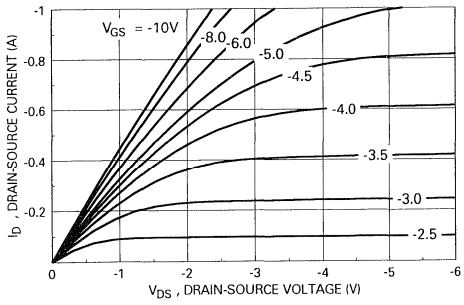


Figure 1. On-Region Characteristics

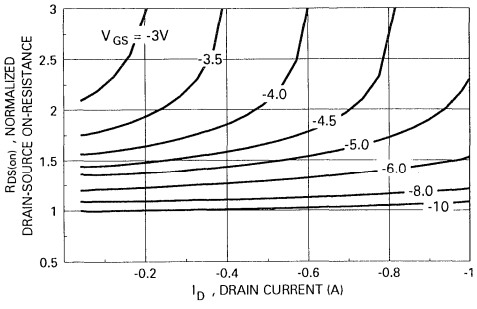


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

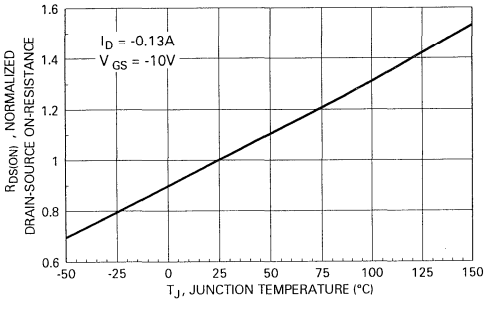


Figure 3. On-Resistance Variation with Temperature

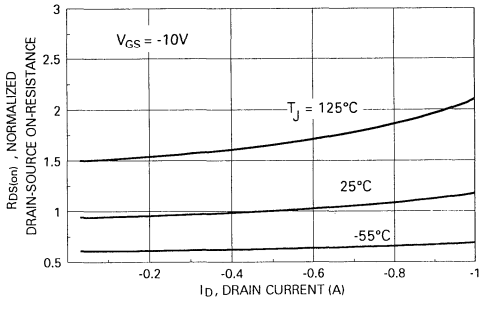


Figure 4. On-Resistance Variation with Drain Current and Temperature

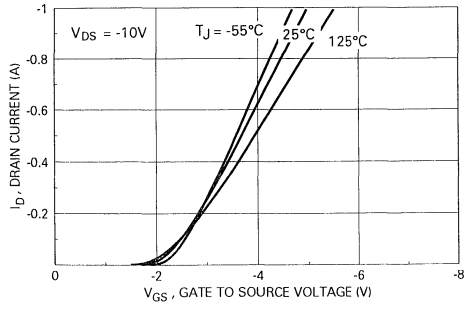


Figure 5. Transfer Characteristics

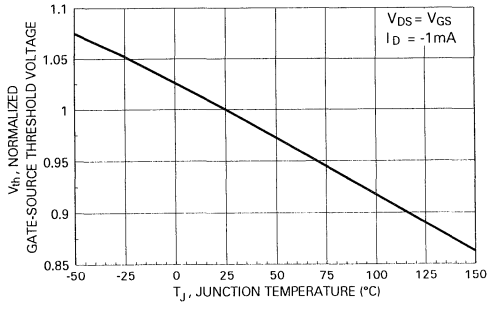


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

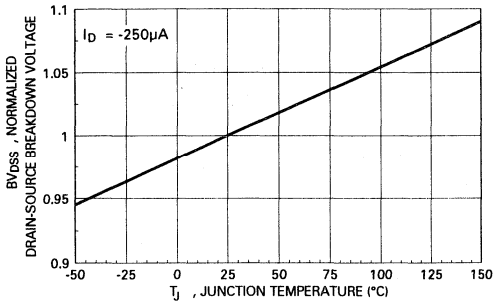


Figure 7. Breakdown Voltage Variation with Temperature

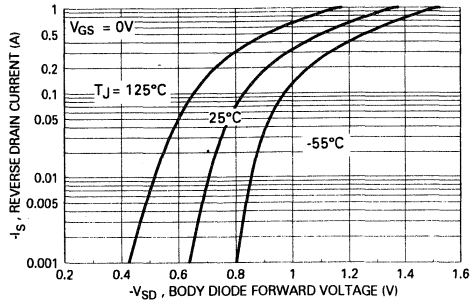


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

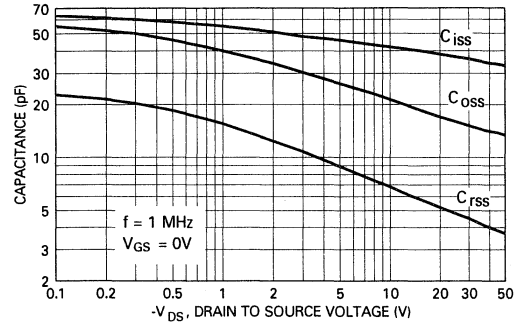


Figure 9. Capacitance Characteristics

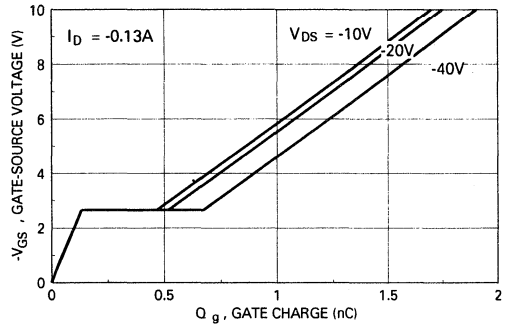


Figure 10. Gate Charge Characteristics

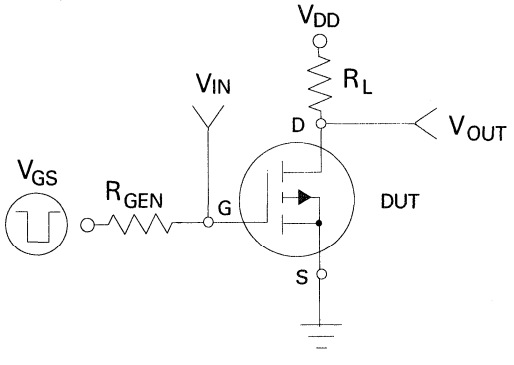


Figure 11. Switching Test Circuit

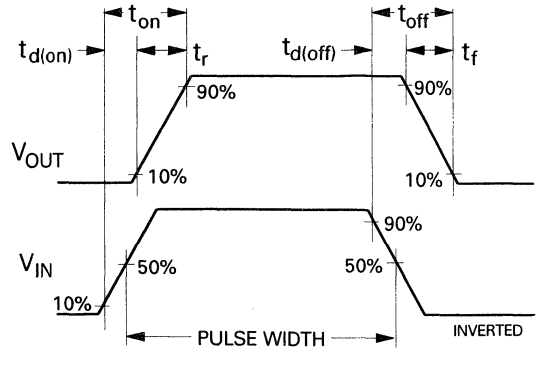


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

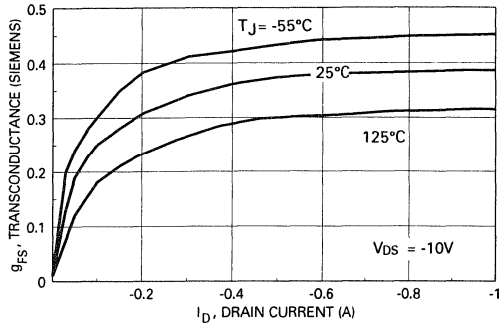


Figure 13. Transconductance Variation with Drain Current and Temperature

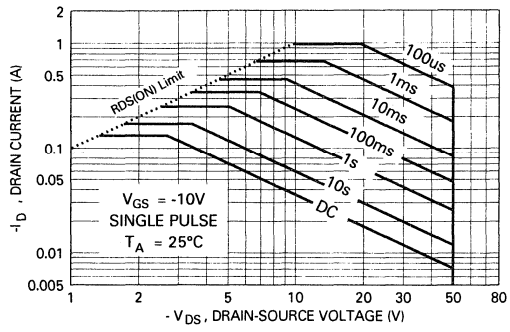


Figure 14. Maximum Safe Operating Area

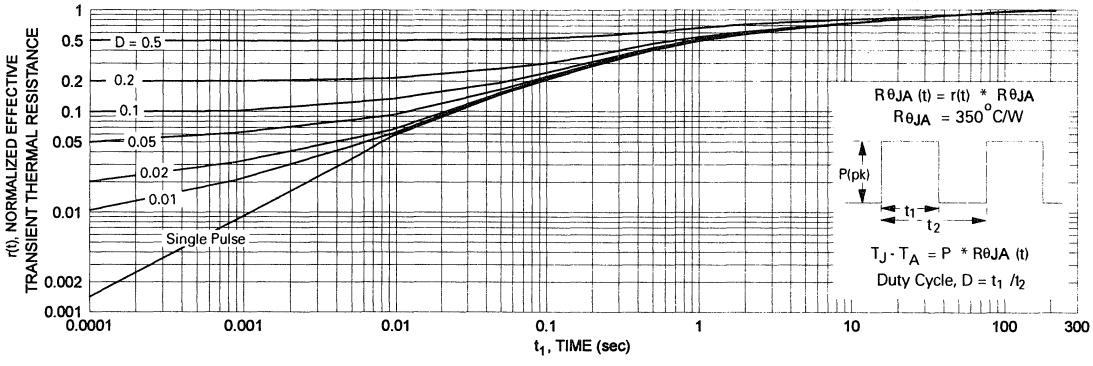


Figure 15. Transient Thermal Response Curve

Note : Characterization performed using a circuit board with 175°C/W typical case-to-ambient thermal resistance.

National Semiconductor™

July 1996

BSS100 / BSS123

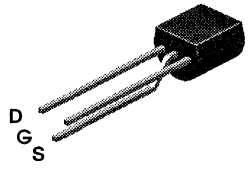
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

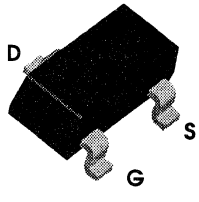
These N-Channel logic level enhancement mode power field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance. This product is particularly suited to low voltage, low current applications, such as small servo motor controls, power MOSFET gate drivers, and other switching applications.

Features

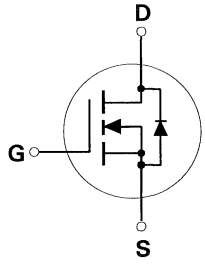
- BSS100: 0.22A, 100V. $R_{DS(ON)}$ = 6Ω @ V_{GS} = 10V.
  BSS123: 0.17A, 100V. $R_{DS(ON)}$ = 6Ω @ V_{GS} = 10V
- High density cell design for extremely low $R_{DS(ON)}$.
- Voltage controlled small signal switch.
- Rugged and reliable.



TO-97
BSS100



SOT-23
BSS123



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	BSS100	BSS123	Units
V_{DSS}	Drain-Source Voltage	100		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 20K\Omega$)	100		V
V_{GSS}	Gate-Source Voltage - Continuous	± 10		V
	- Non Repetitive ($T_P < 50\ \mu S$)	± 20		
I_D	Drain Current - Continuous	0.22	0.17	A
	- Pulsed	0.9	0.68	
P_D	Total Power Dissipation @ T_A = 25°C	0.63	0.36	mW
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistacne, Junction-to-Ambient	200	350	°C/W

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Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	All	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 100 V, V_{GS} = 0 V	BSS100			15	µA
		V_{DS} = 100 V, V_{GS} = 0 V	BSS123			1	µA
		V_{DS} = 100 V, V_{GS} = 0 V, T_J=125°C	All			60	µA
		V_{DS} = 60 V, V_{GS} = 0 V	BSS100			10	nA
		V_{DS} = 20 V, V_{GS} = 0 V	BSS123			10	nA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	BSS100			10	nA
		V_{GS} = 20 V, V_{DS} = 0 V	BSS123			50	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	All	0.8		2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.22 A	BSS100			6	Ω
		V_{GS} = 10 V, I_D = 0.17 A	BSS123			6	
		V_{GS} = 4.5 V, I_D = 0.22 A	BSS100			10	
		V_{GS} = 4.5 V, I_D = 0.17 A	BSS123			10	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.22 A	BSS100	0.08			S
		V_{DS} = 10 V, I_D = 0.17 A	BSS123	0.08			
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All			60	pF
C_{oss}	Output Capacitance		All			15	pF
C_{rss}	Reverse Transfer Capacitance		All			6	pF
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 0.28 A, V_{GS} = 10 V, R_{GEN} = 50 Ω	All			8	ns
t_r	Turn - On Rise Time		All			12	ns
$t_{D(off)}$	Turn - Off Delay Time		All			16	ns
t_f	Turn - Off Fall Time		All			22	ns
Q_g	Totall Gate Charge	V_{DS} = 10 V, I_D = 0.22 A, V_{GS} = 10 V,	All			2	nC
Q_{gs}	Gate-Source Charge		All			0.25	nC
Q_{gd}	Gate-Drain Charge		All			0.4	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Source Current		BSS100			0.22	A
			BSS123			0.17	
I_{SM}	Maximum Pulse Source Current (Note 1)		BSS100			0.9	A
			BSS123			0.68	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.44 A	BSS100			1.3	V
		V_{GS} = 0 V, I_S = 0.34 A	BSS123			1.3	

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

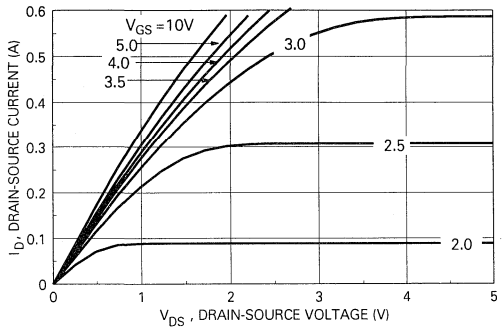


Figure 1. On-Region Characteristics.

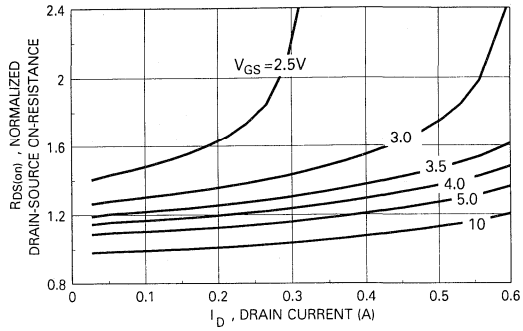


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

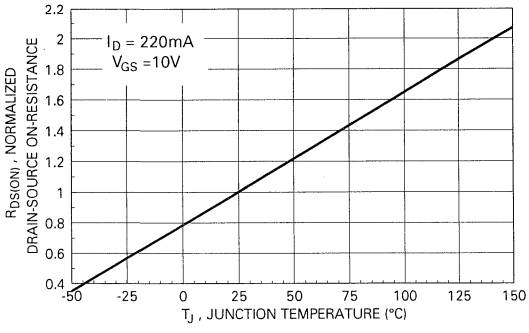


Figure 3. On-Resistance Variation with Temperature.

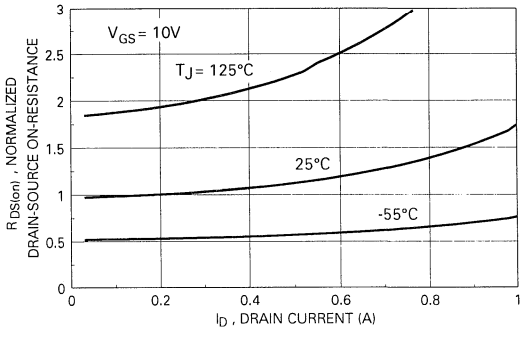


Figure 4. On-Resistance Variation with Drain Current and Temperature.

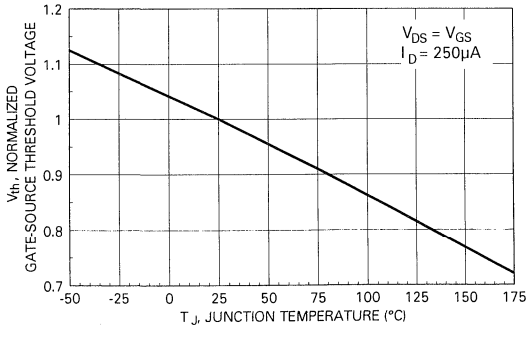


Figure 5. Gate Threshold Variation with Temperature

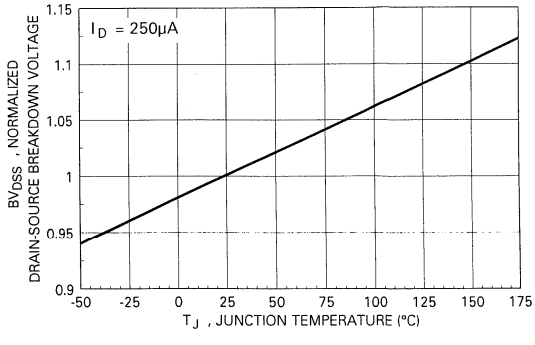


Figure 6. Breakdown Voltage Variation with Temperature.

Typical Electrical Characteristics (continued)

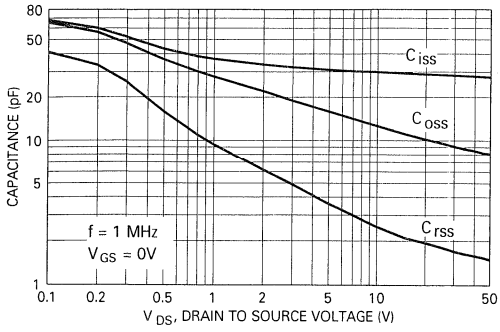


Figure 7. Capacitance Characteristics.

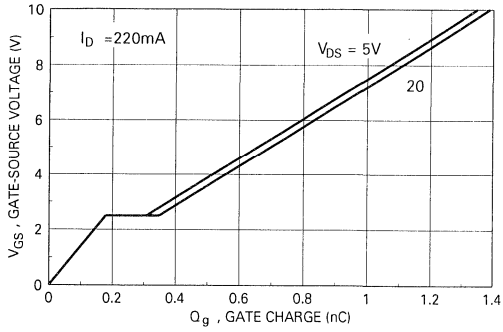


Figure 8. Gate Charge Characteristics.

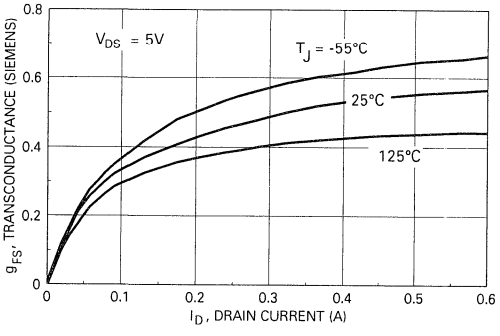


Figure 9. Transconductance Variation with Drain Current and Temperature.

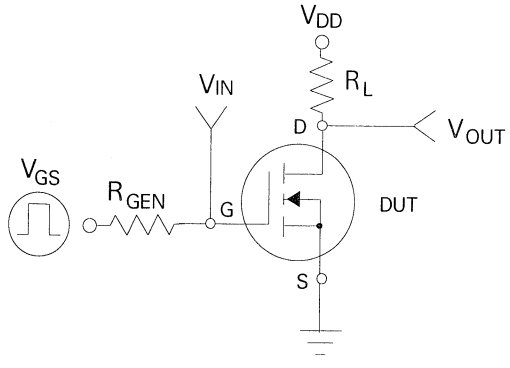


Figure 10. Switching Test Circuit

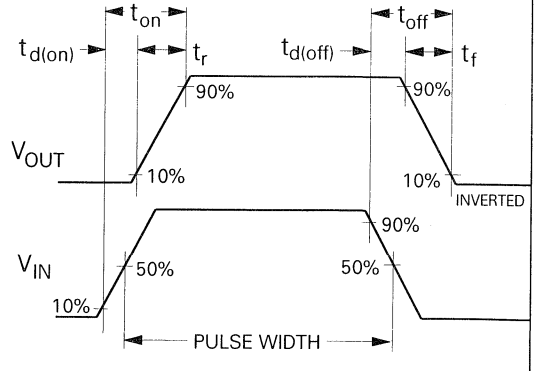


Figure 11. Switching Waveforms

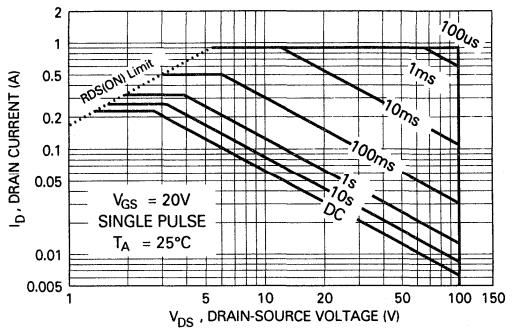


Figure 12. BSS100 Maximum Safe Operating Area.

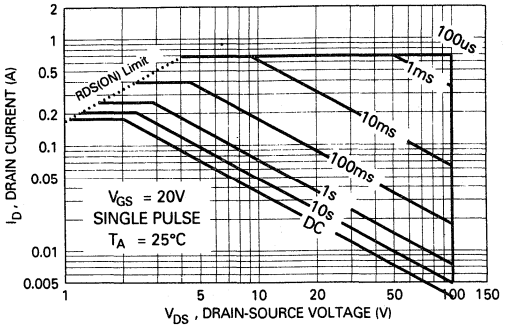


Figure 13. BSS123 Maximum Safe Operating Area.

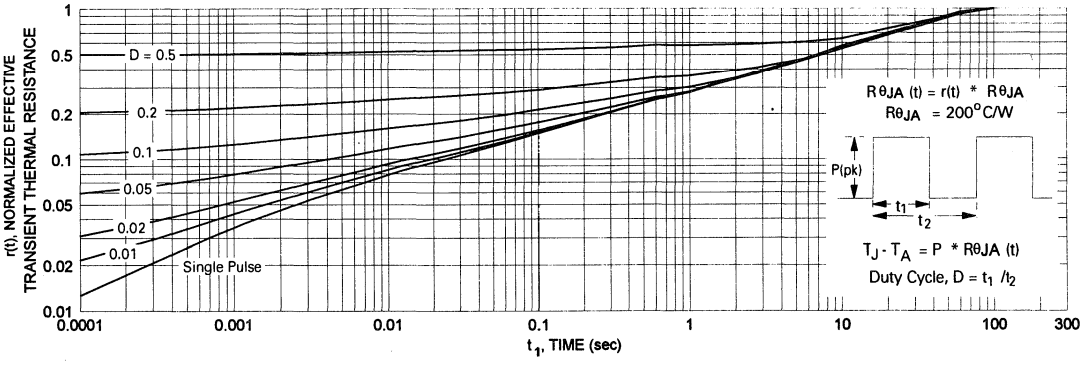


Figure 14. BSS100 Transient Thermal Response Curve

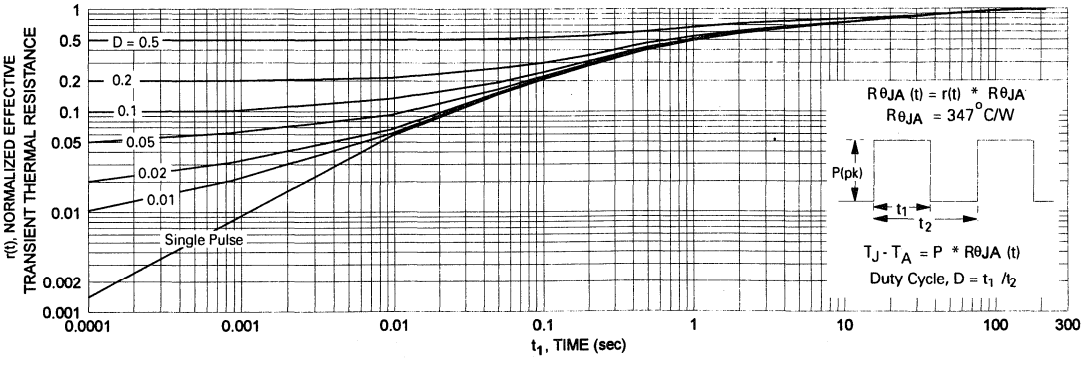


Figure 15. BSS123 Transient Thermal Response Curve

National Semiconductor™

May 1995

BSS138

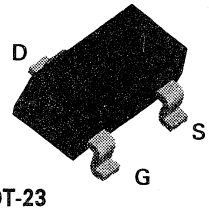
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

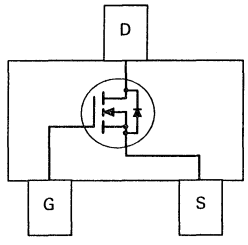
These N-Channel enhancement mode field effect transistors are produced using Nationals proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

Features

- 0.22 A, 50V. $R_{DS(ON)}$ = 3.5Ω @ V_{GS} = 10V.
- High density cell design for extremely low $R_{DS(ON)}$.
- Rugged and Relaible
- Compact industry standard SOT-23 surface mount package.



SOT-23
(TO-236AB)



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	BSS138	Units
V_{DSS}	Drain-Source Voltage	50	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 20K\Omega$)	50	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
	- Non Repetitive ($T_P < 50\ \mu S$)	± 40	
I_D	Drain Current - Continuous	0.22	A
	- Pulsed	0.88	
P_D	Maximum Power Dissipation	0.36	W
	Derate Above 25°C	2.8	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 Seconds	300	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	350	°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			0.5	µA
		T_J =125°C			5	µA
		V_{DS} = 30 V, V_{GS} = 0 V			100	nA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.8	1.3	1.6	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 0.22 A		0.81	3.5	Ω
		V_{GS} = 4.5 V, I_D = 0.22 A		1.16	6	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.22 A	0.12	0.45		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		30	60	pF
C_{oss}	Output Capacitance			15	25	pF
C_{rss}	Reverse Transfer Capacitance			7.5	10	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 0.29 A, V_{GS} = 10 V, R_{GEN} = 50 Ω			8	ns
t_r	Turn - On Rise Time				12	ns
$t_{D(off)}$	Turn - Off Delay Time				16	ns
t_f	Turn - Off Fall Time				22	ns
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Source Current				0.22	A
I_{SM}	Maximum Pulse Source Current (Note 1)				0.88	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.44 A		0.8	1.4	V

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

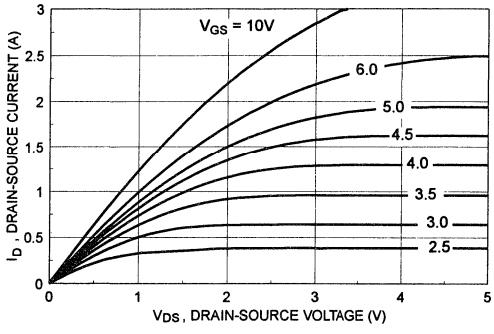


Figure 1. On-Region Characteristics.

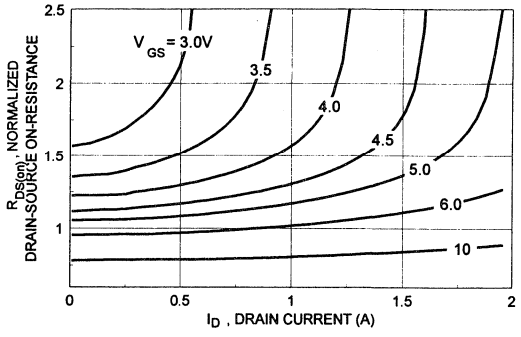


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

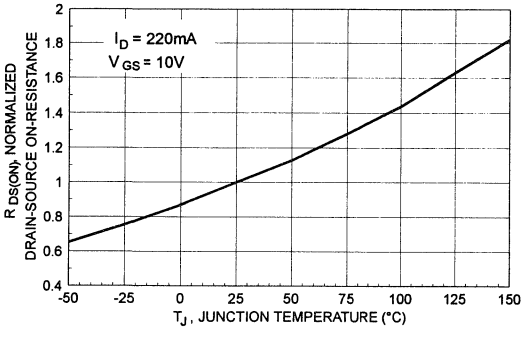


Figure 3. On-Resistance Variation with Temperature.

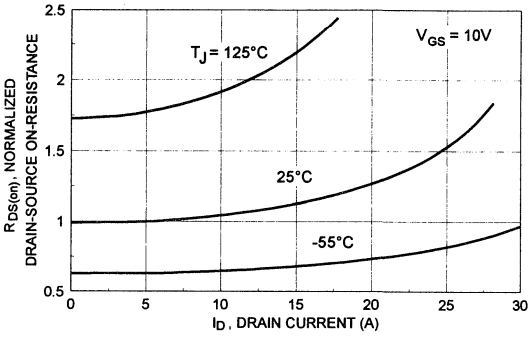


Figure 4. On-Resistance Variation with Drain Current and Temperature.

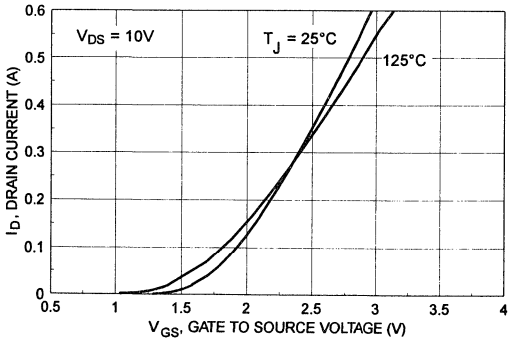


Figure 5. Transfer Characteristics.

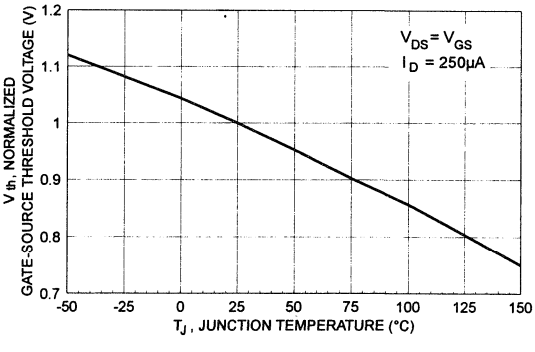


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

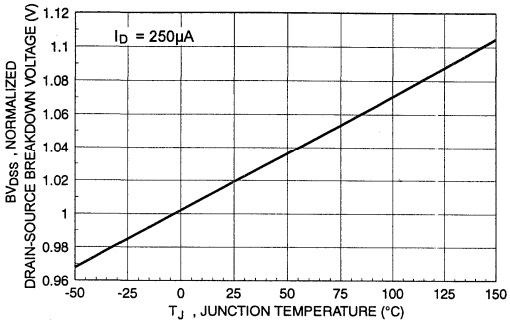


Figure 7. Breakdown Voltage Variation with Temperature.

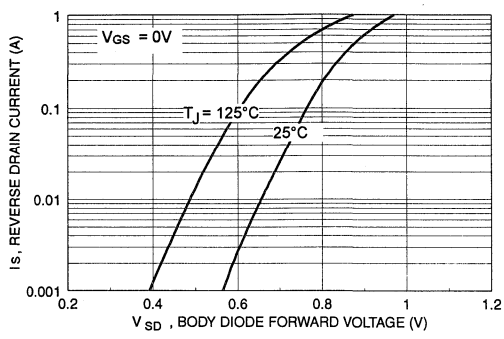


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

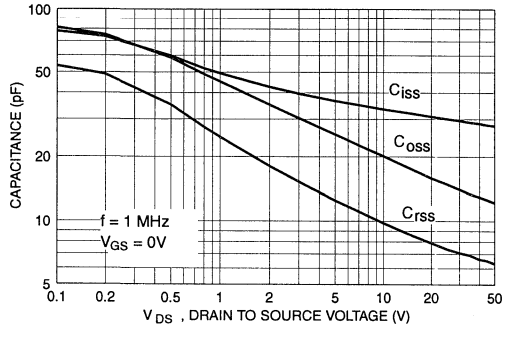


Figure 9. Capacitance Characteristics.

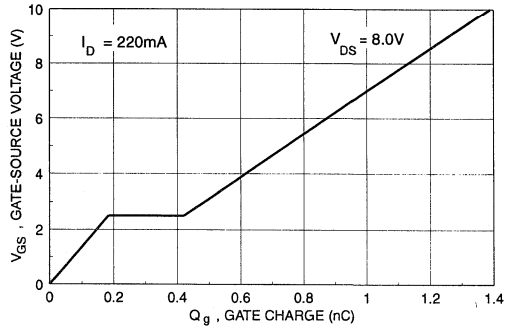


Figure 10. Gate Charge Characteristics.

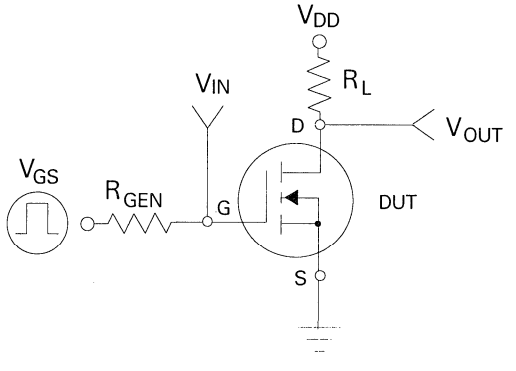


Figure 11. Switching Test Circuit

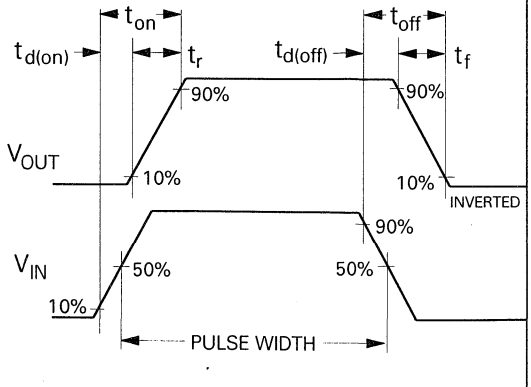


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

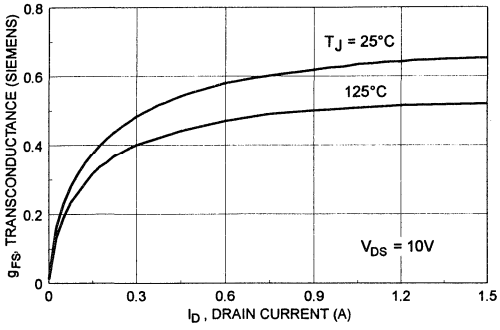


Figure 13. Transconductance Variation with Drain Current and Temperature.

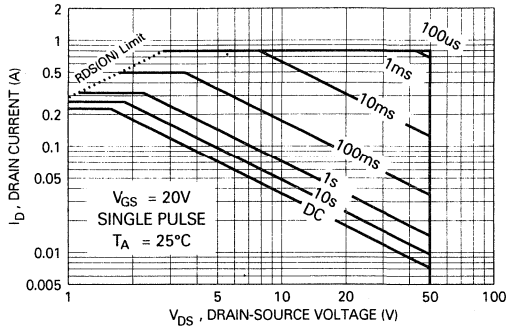


Figure 14. Maximum Safe Operating Area

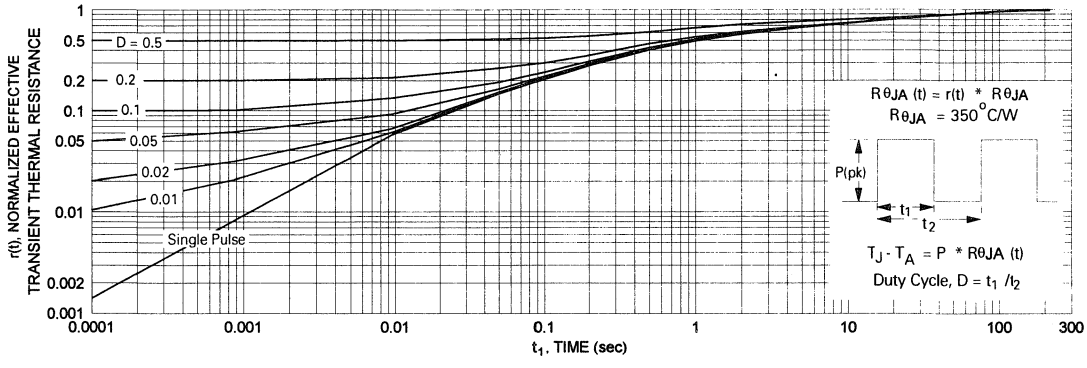


Figure 15. Transient Thermal Response Curve

National Semiconductor™

April 1995

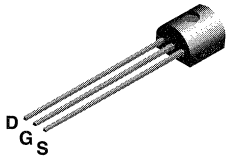
NDF0610 / NDS0610
P-Channel Enhancement Mode Field Effect Transistor

General Description

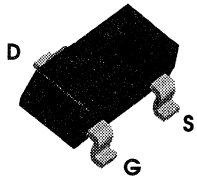
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 180mA DC and can deliver pulsed currents up to 1A. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

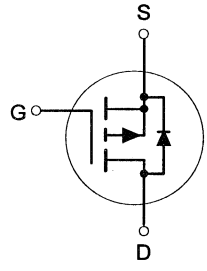
- -0.18 and -0.12A, -60V. $R_{DS(ON)}$ = 10Ω
- Voltage controlled p-channel small signal switch
- High density cell design for low $R_{DS(ON)}$
- TO-92 and SOT-23 packages for both through hole and surface mount applications
- High saturation current



TO-92
NDF0610



SOT23
(TO-236AB)
NDS0610



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	NDF0610	NDS0610	Units
V_{DSS}	Drain-Source Voltage	-60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-60		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
	- Nonrepetitive ($t_P < 50$ µs)	±30		V
I_D	Drain Current - Continuous	-0.18	-0.12	A
	- Pulsed	-1		
P_D	Maximum Power Dissipation T_A = 25°C	0.8	0.36	W
	Derate above 25°C	5	2.9	mW/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
T_L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	300		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	200	350	°C/W

7

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -10 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-200	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			10	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-10	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -1 mA	-1	-2.4	-3.5	V
		T_J = 125°C	-0.6	-2.1	-3.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.5 A		3.6	10	Ω
		T_J = 125°C		5.9	16	
		V_{GS} = -4.5 V, I_D = -0.25 A		5.2	20	
		T_J = 125°C		7.9	30	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -10 V	-0.6	-1.6		A
		V_{GS} = -4.5 V, V_{DS} = -10 V		-0.35		
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -0.1 A	70	170		mS
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz		40	60	pF
C_{oss}	Output Capacitance			11	25	pF
C_{rss}	Reverse Transfer Capacitance			3.2	5	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -25 V, I_D = -0.18 A, V_{GS} = -10 V, R_{GEN} = 25 Ω		7	10	nS
t_r	Turn - On Rise Time			5	15	nS
$t_{D(off)}$	Turn - Off Delay Time			13	15	nS
t_f	Turn - Off Fall Time			10	20	nS
Q_g	Total Gate Charge	V_{DS} = -48 V, I_D = -0.5 A, V_{GS} = -10 V		1.43		nC
Q_{gs}	Gate-Source Charge			0.6		nC
Q_{gd}	Gate-Drain Charge			0.25		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Source Current				-0.18	A
I_{SM}	Maximum Pulse Source Current (Note 1)				-1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.5 A (Note 1)		-1.2	-1.5	V
		T_J = 125°C		-0.98	-1.3	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -0.5 A, dI_F/dt = 100 A/µs		40		ns
I_{rr}	Reverse Recovery Current			2.8		A

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

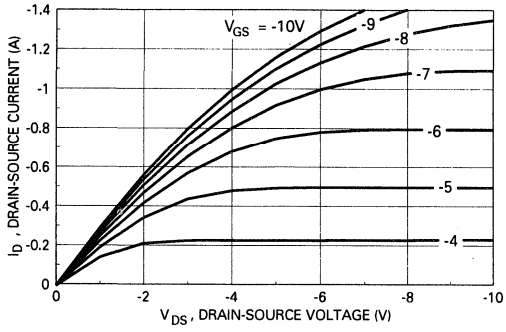


Figure 1. On-Region Characteristics

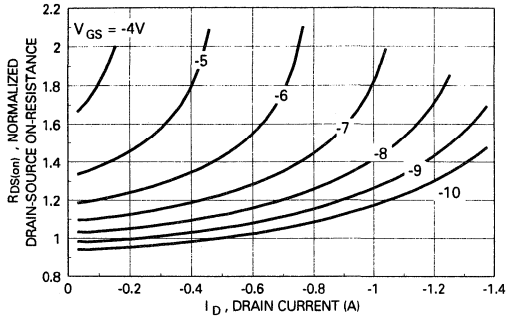


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

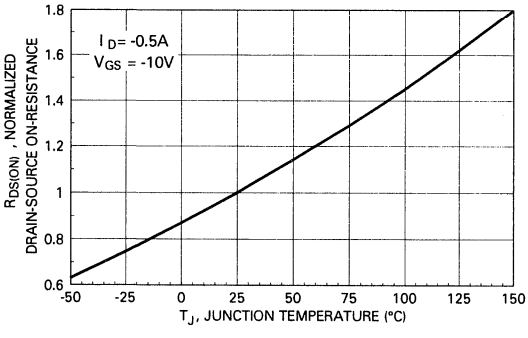


Figure 3. On-Resistance Variation with Temperature

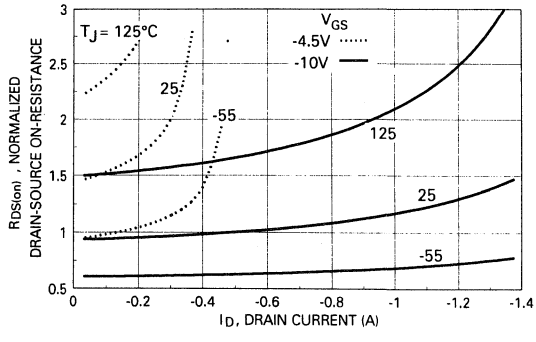


Figure 4. On-Resistance Variation with Drain

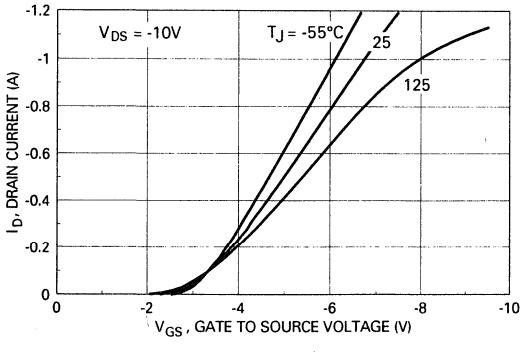


Figure 5. Transfer Characteristics

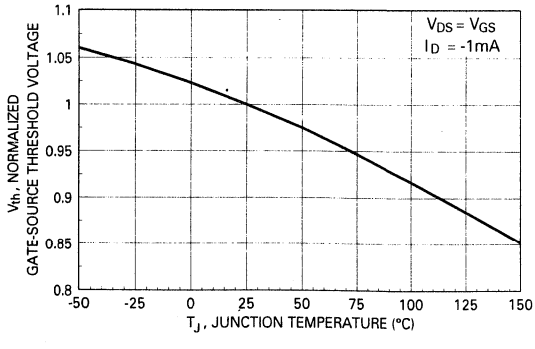


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

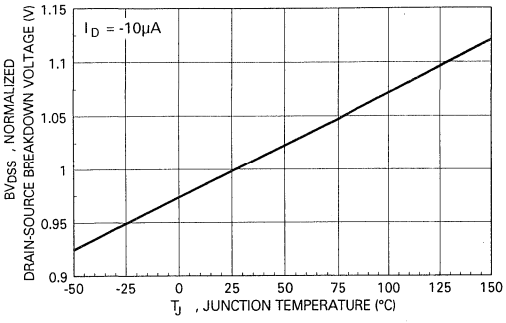


Figure 7. Breakdown Voltage Variation with Temperature

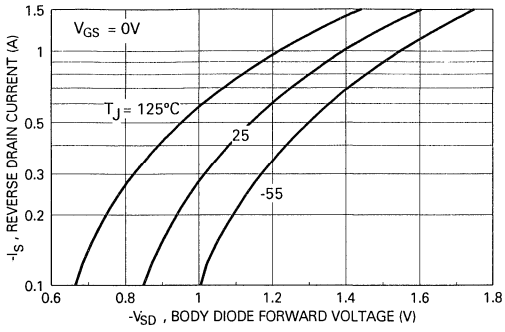


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

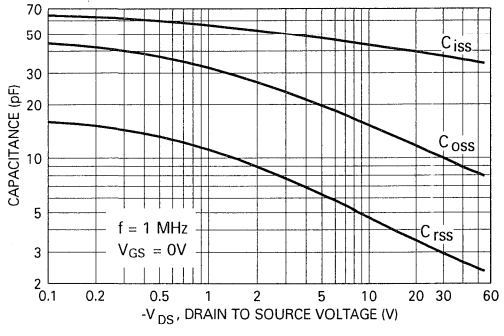


Figure 9. Capacitance Characteristics

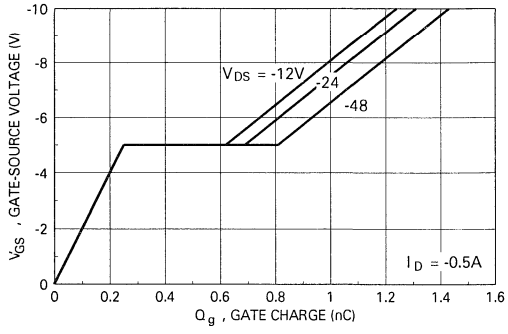


Figure 10. Gate Charge Characteristics

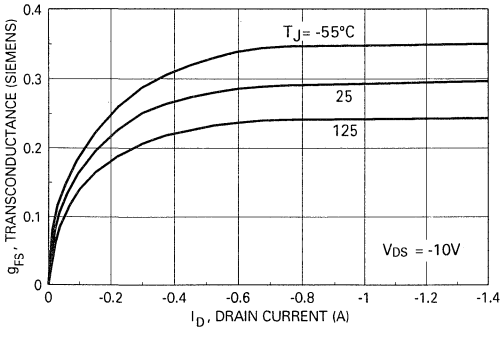


Figure 11. Transconductance Variation with Drain Current and Temperature

Typical Electrical Characteristics (continued)

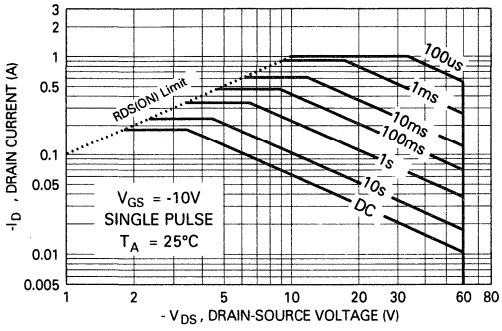


Figure 12. NDF0610 (TO-92) Maximum Safe Operating Area

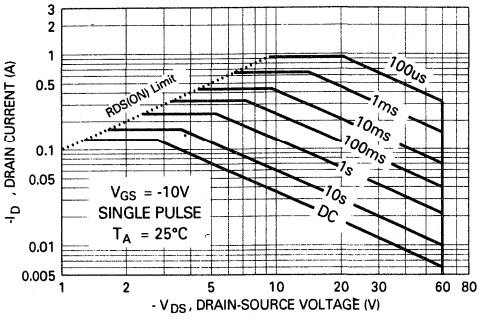


Figure 13. NDS0610 (SOT-23) Maximum Safe Operating Area

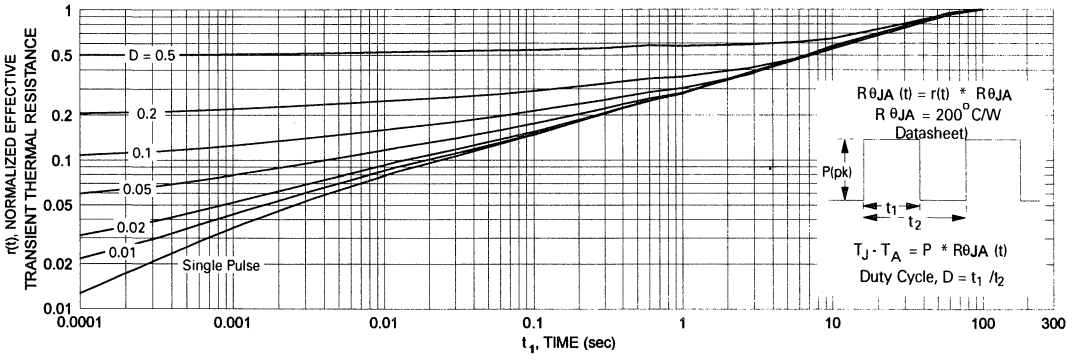


Figure 14. NDF0610 (TO-92) Transient Thermal Response Curve.

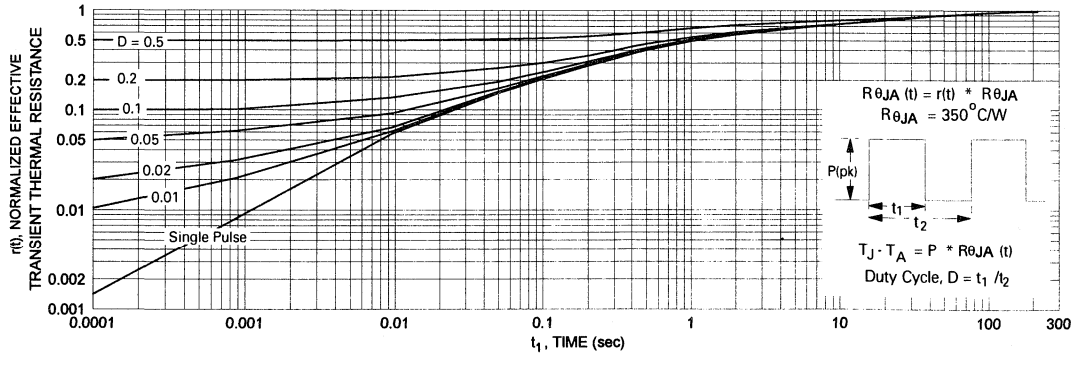


Figure 15. NDS0610 (SOT-23) Transient Thermal Response Curve.

National Semiconductor™

April 1995

NDS0605

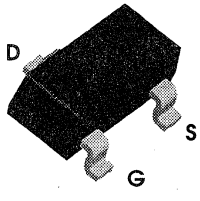
P-Channel Enhancement Mode Field Effect Transistor

General Description

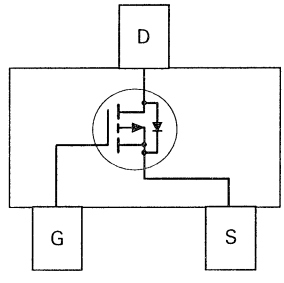
These P-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. They can be used, with a minimum of effort, in most applications requiring up to 0.18A DC and can deliver pulsed currents up to 1A. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- -0.18A, -60V. $R_{DS(ON)}$ = 5Ω @ V_{GS} = -10V.
- Voltage controlled p-channel small signal switch.
- High density cell design for low $R_{DS(ON)}$.
- High saturation current.



SOT23
(TO-236AB)



Absolute Maximum Ratings

T_A = 25°C unless otherwise noted

Symbol	Parameter	NDS0605	Units
V_{DSS}	Drain-Source Voltage	-60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	-60	V
V_{GSS}	Gate-Source Voltage - Continuous	±20	V
I_D	Drain Current - Continuous	-0.18	A
	- Pulsed	-1	
P_D	Maximum Power Dissipation T_A = 25°C	0.36	W
	Derate above 25°C	2.9	mW/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
T_L	Maximum lead temperature for soldering purposes, 1/16" from case for 10 seconds	300	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	350	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -10 µA	-60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -48 V, V_{GS} = 0 V			-1	µA
		T_J = 125°C			-500	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-3	V
		T_J = 125°C	-0.6		-2.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.5 A			5	Ω
		T_J = 125°C			10	
		V_{GS} = -4.5 V, I_D = -0.25 A			7.5	
		T_J = 125°C			15	
$I_{D(on)}$	On-State Drain Current	V_{GS} = -10 V, V_{DS} = -10 V	-0.6			A
		V_{GS} = -4.5 V, V_{DS} = -10 V	-0.25			
g_{FS}	Forward Transconductance	V_{DS} = -10 V, I_D = -0.2 A	0.07			S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz			60	pF
C_{oss}	Output Capacitance				25	pF
C_{rss}	Reverse Transfer Capacitance				5	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -30 V, I_D = -0.2 A, V_{GS} = -10 V, R_{GEN} = 25 Ω			10	nS
t_r	Turn - On Rise Time				15	nS
$t_{D(off)}$	Turn - Off Delay Time				15	nS
t_f	Turn - Off Fall Time				20	nS
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Continuous Source Diode Current				-0.18	A
I_{SM}	Maximum Pulsed Source Diode Current (Note 1)				-1	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.5 A (Note 1)			-1.5	V
		T_J = 125°C			-1.3	

Note :
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

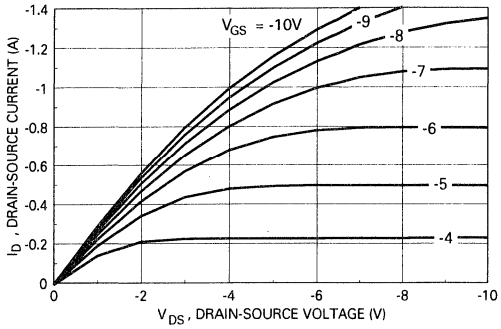


Figure 1. On-Region Characteristics

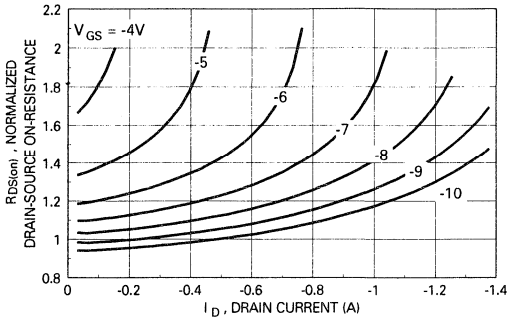


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

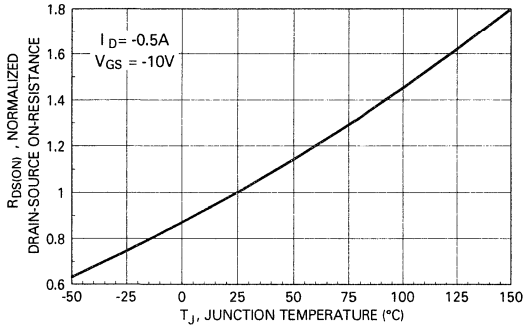


Figure 3. On-Resistance Variation with Temperature

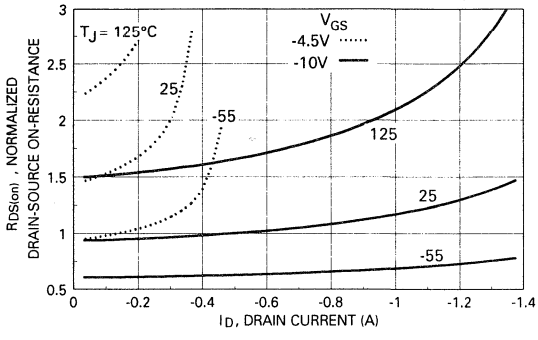


Figure 4. On-Resistance Variation with Drain Current and Temperature

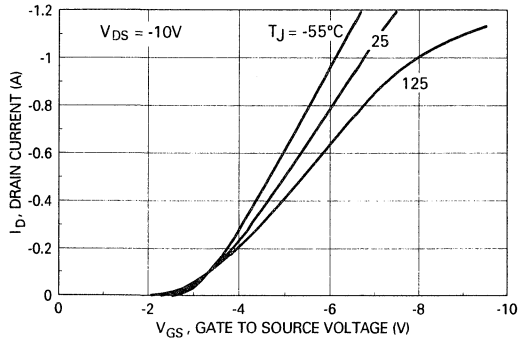


Figure 5. Transfer Characteristics

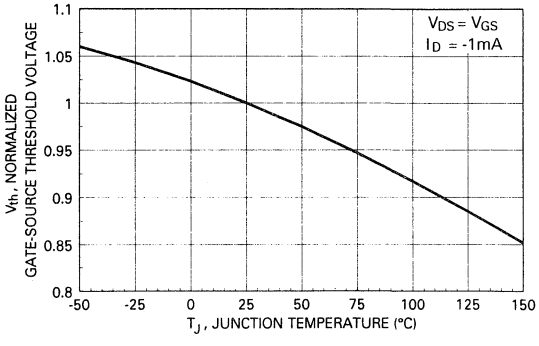


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

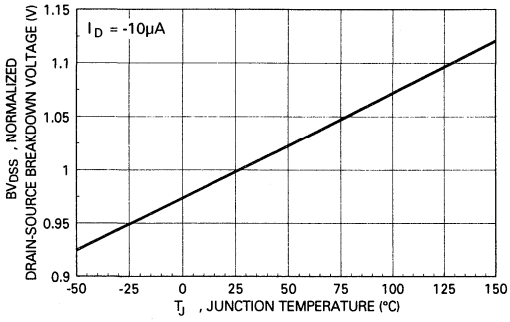


Figure 7. Breakdown Voltage Variation with Temperature

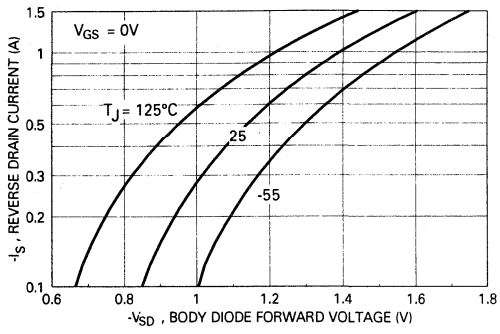


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

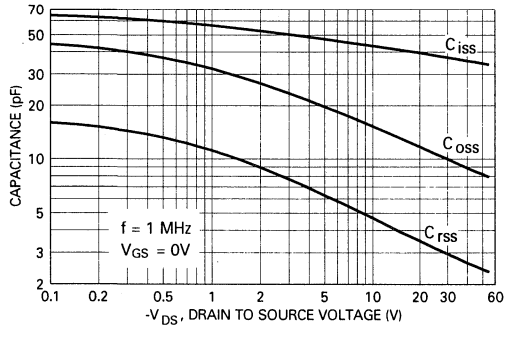


Figure 9. Capacitance Characteristics

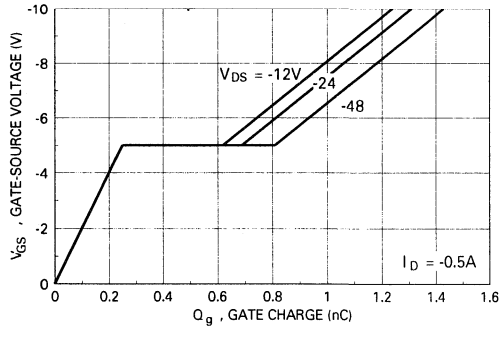


Figure 10. Gate Charge Characteristics

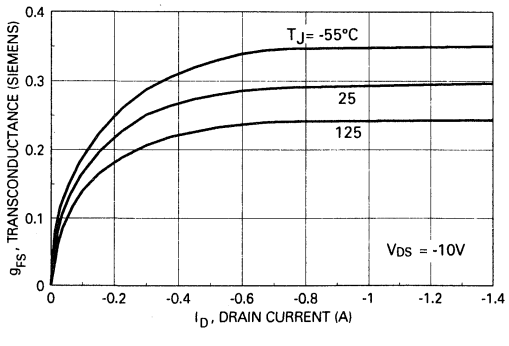


Figure 11. Transconductance Variation with Drain Current and Temperature

Typical Electrical Characteristics (continued)

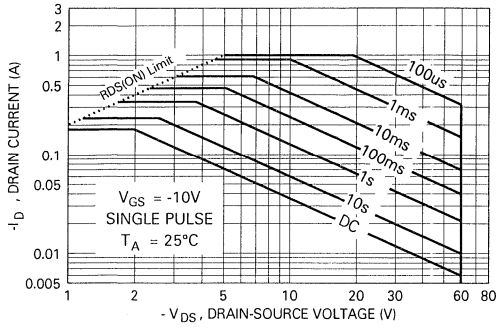


Figure 12. Maximum Safe Operating Area

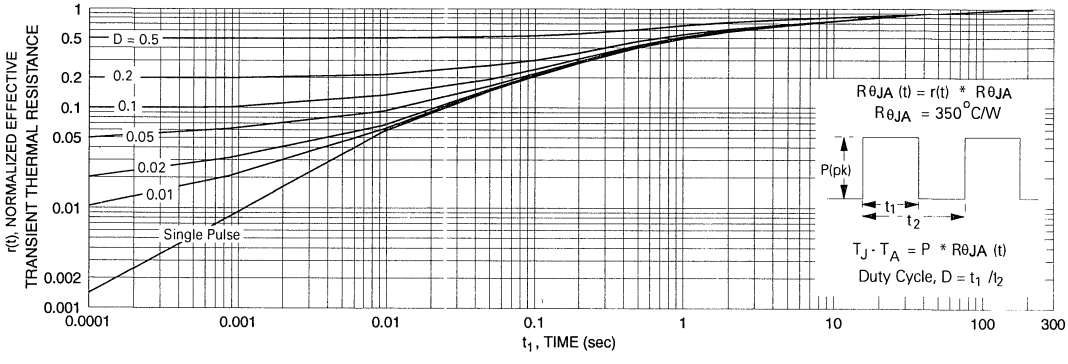


Figure 13. Transient Thermal Response Curve.

Section 8

TO-220 / TO-263 Data Sheets

National Semiconductor™

May 1995

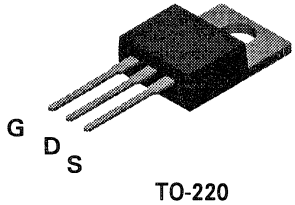
NDP506A / NDP506B
NDB506A / NDB506B
N-Channel Enhancement Mode Field Effect Transistor

General Description

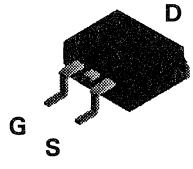
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

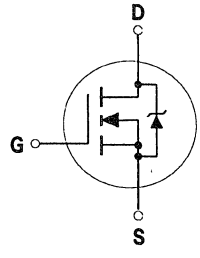
- 26 and 24A, 60V. $R_{DS(ON)}$ = 0.05 and 0.06Ω.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP506A NDB506A	NDP506B NDB506B	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	±20		V
	- Nonrepetitive ($t_P < 50$ µs)	±40		
I_D	Drain Current - Continuous	26	24	A
	- Pulsed	78	72	
P_D	Total Power Dissipation @ T_C = 25°C	75		W
	Derate above 25°C	0.5		W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	All			250	µA
		T_J = 125°C				1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	All	2	2.6	4	V
		T_J = 125°C		1.4	2	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 13 A	NDP506A NDB506A		0.04	0.05	Ω
		T_J = 125°C			0.064	0.08	
		V_{GS} = 10 V, I_D = 12 A	NDP506B NDB506B			0.06	
		T_J = 125°C				0.096	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	NDP506A NDB506A	26			A
			NDP506B NDB506B	24			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 13 A	All	6	9.4		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All		710	900	pF
C_{oss}	Output Capacitance		All		270	400	pF
C_{rss}	Reverse Transfer Capacitance		All		115	200	pF
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 26 A, V_{GS} = 10 V, R_{GEN} = 15 Ω	All		9	20	nS
t_r	Turn - On Rise Time		All		100	200	nS
$t_{D(off)}$	Turn - Off Delay Time		All		29	60	nS
t_f	Turn - Off Fall Time		All		60	120	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 26 A, V_{GS} = 10V	All		26	32	nC
Q_{gs}	Gate-Source Charge		All		5		nC
Q_{gd}	Gate-Drain Charge		All		15		nC

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuos Drain-Source Diode Forward Current		NDP506A NDB506A			26	A
			NDP506B NDB506B			24	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		NDP506A NDB506A			78	A
			NDP506B NDB506B			72	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 1)	All		0.94	1.3	V
		T_J = 125°C			0.83	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 26 A, dI_F/dt = 100 A/µs	All	30	55	120	ns
I_{rr}	Reverse Recovery Current		All	2	3.6	8	A
THERMAL CHARACTERISTICS							
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		All			2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		All			62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

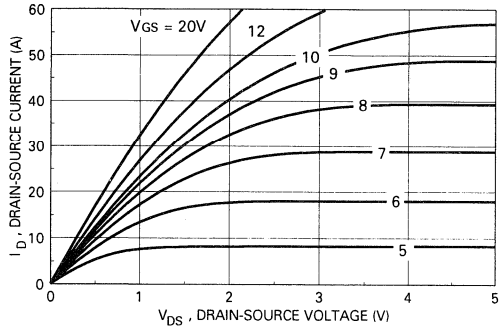


Figure 1. On-Region Characteristics

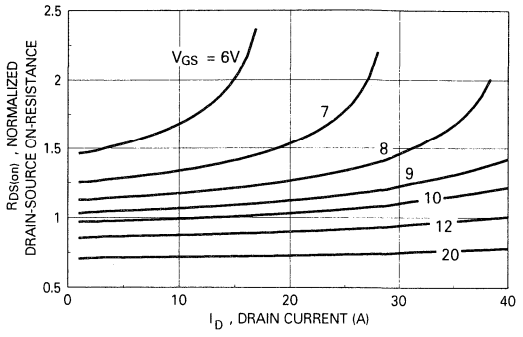


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

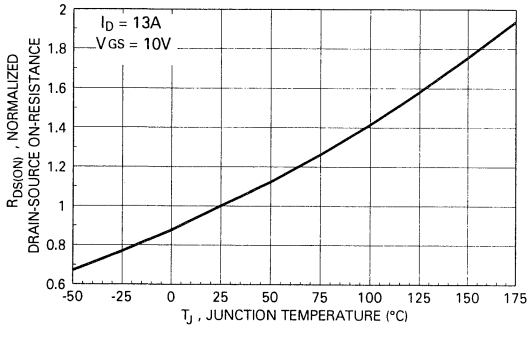


Figure 3. On-Resistance Variation with Temperature

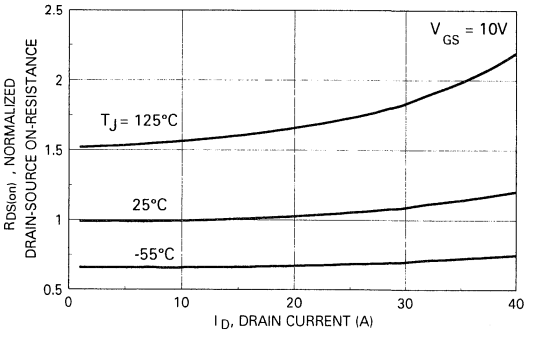


Figure 4. On-Resistance Variation with Drain Current and Temperature

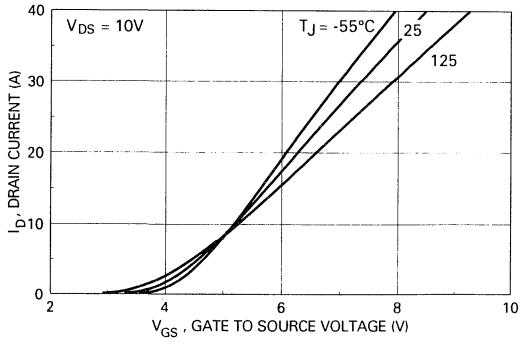


Figure 5. Transfer Characteristics

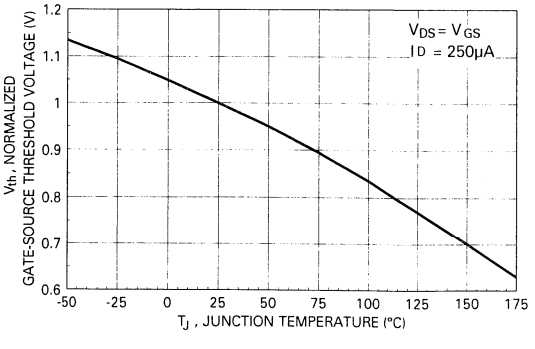


Figure 6. Gate Threshold Variation with Temperature

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Typical Electrical Characteristics (continued)

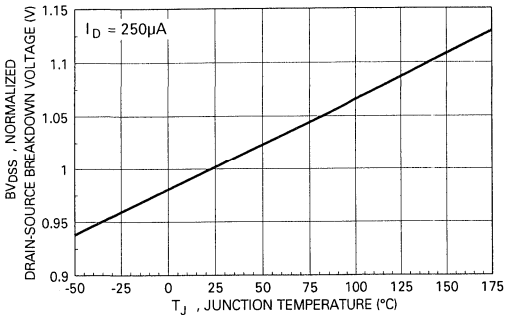


Figure 7. Breakdown Voltage Variation with Temperature

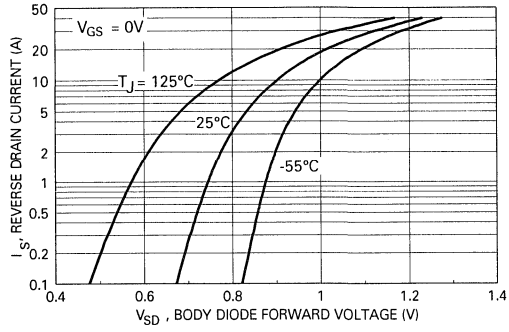


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

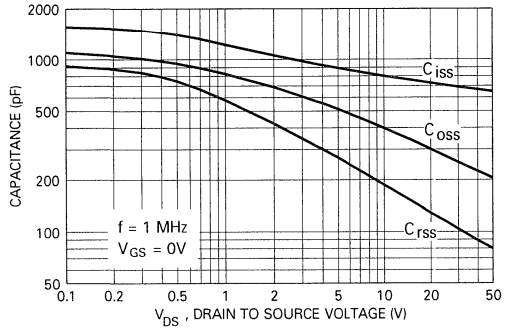


Figure 9. Capacitance Characteristics

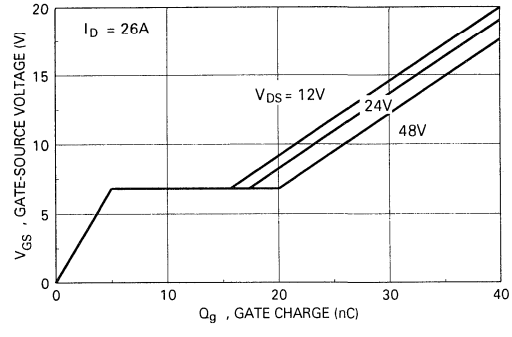


Figure 10. Gate Charge Characteristics

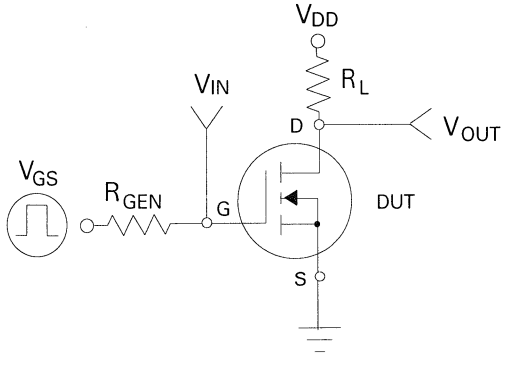


Figure 11. Switching Test Circuit

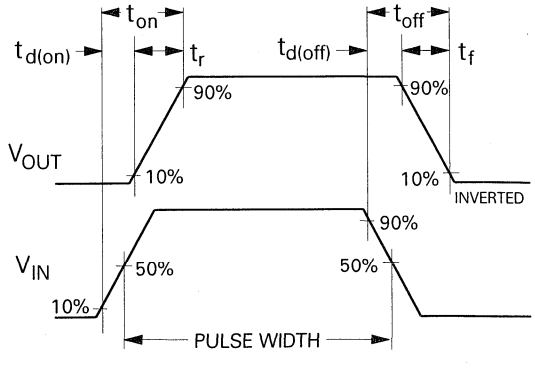


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

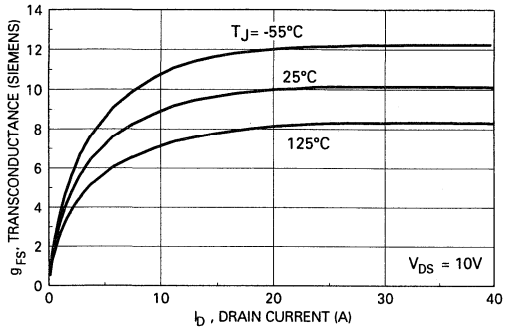


Figure 13. Transconductance Variation with Drain Current and Temperature

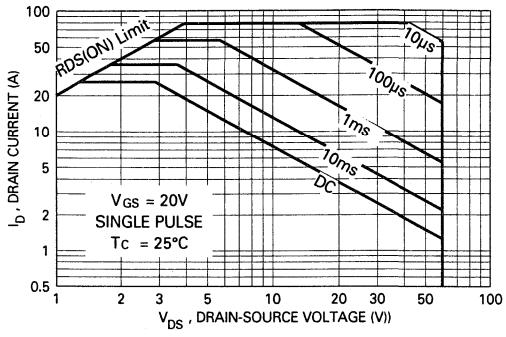


Figure 14. Maximum Safe Operating Area

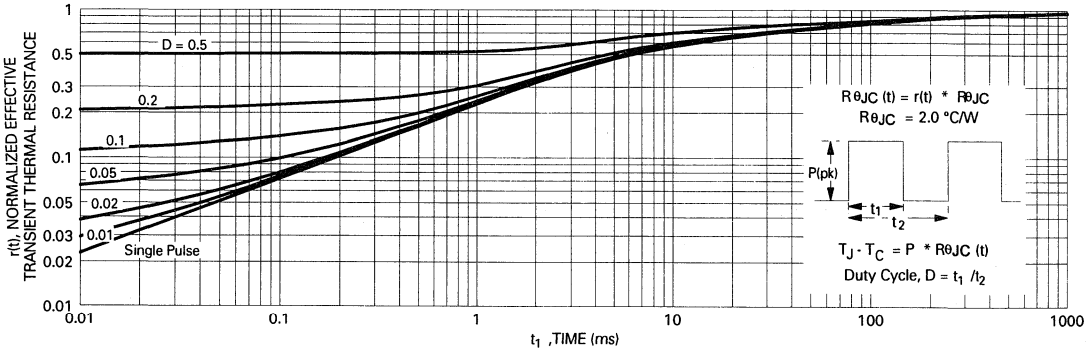


Figure 15. Transient Thermal Response Curve

8

National Semiconductor™

May 1995

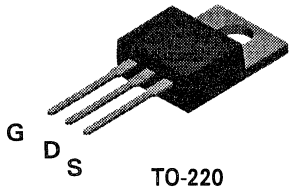
NDP506AL / NDP506BL
NDB506AL / NDB506BL
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

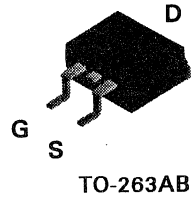
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to

Features

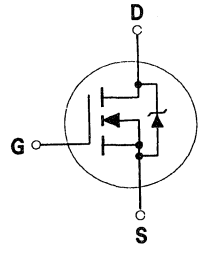
- 26 and 24A, 60V. $R_{DS(ON)}$ = 0.050 and 0.060Ω.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP506AL NDB506AL	NDP506BL NDB506BL	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	±10		V
	- Nonrepetitive (t_P < 50 μs)	±20		
I_D	Drain Current - Continuous	26	24	A
	- Pulsed	78	72	
P_D	Total Power Dissipation @ T_C = 25°C	75		W
	Derate above 25°C	0.5		W/°C
T_J,T_{STG}	Operating and Storage Temperature	-65 to 175		°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	All	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V	All			250	µA
		T_J = 125°C				1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 10 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -10 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 1)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	All	1	1.4	2	V
		T_J = 125°C		0.65	1	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 13 A	NDP506AL NDB506AL		0.045	0.05	Ω
		T_J = 125°C			0.069	0.08	
		V_{GS} = 5 V, I_D = 12 A	NDP506BL NDB506BL			0.06	
		T_J = 125°C				0.096	
		V_{GS} = 10 V, I_D = 13 A	NDP506AL NDB506AL		0.031	0.035	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	NDP506AL NDB506AL	26			A
			NDP506BL NDB506BL	24			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 13 A	All	6	13.8		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	All		835	1000	pF
C_{oss}	Output Capacitance		All		288	400	pF
C_{rss}	Reverse Transfer Capacitance		All		115	200	pF
SWITCHING CHARACTERISTICS (Note 1)							
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 26 A, V_{GS} = 5 V, R_{GEN} = 30 Ω, R_{GS} = 30 Ω	All		10	20	nS
t_r	Turn - On Rise Time		All		245	400	nS
$t_{D(off)}$	Turn - Off Delay Time		All		44	80	nS
t_f	Turn - Off Fall Time		All		105	200	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 26 A, V_{GS} = 5 V	All		21	32	nC
Q_{gs}	Gate-Source Charge		All		3.7		nC
Q_{gd}	Gate-Drain Charge		All		14.7		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS							
I_S	Maximum Continuos Drain-Source Diode Forward Current		NDP506AL NDB506AL			26	A
			NDP506BL NDB506BL			24	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		NDP506AL NDB506AL			78	A
			NDP506BL NDB506BL			72	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 13 A (Note 1)	All		0.92	1.3	V
		T_J = 125°C			0.81	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 26 A, dI_F/dt = 100 A/µs	All	30	55	120	ns
I_{rr}	Reverse Recovery Current		All	2	3.6	8	A
THERMAL CHARACTERISTICS							
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case		All			2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient		All			62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

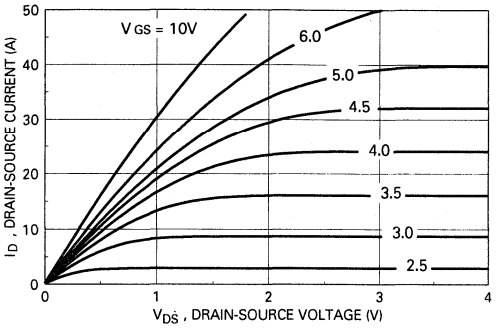


Figure 1. On-Region Characteristics

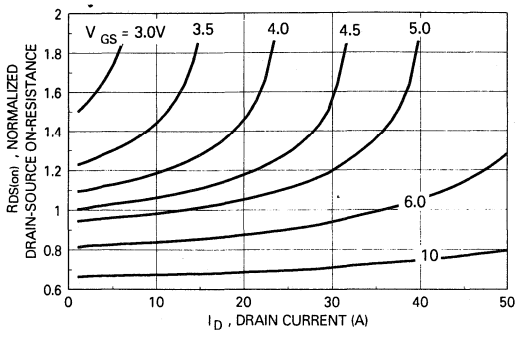


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

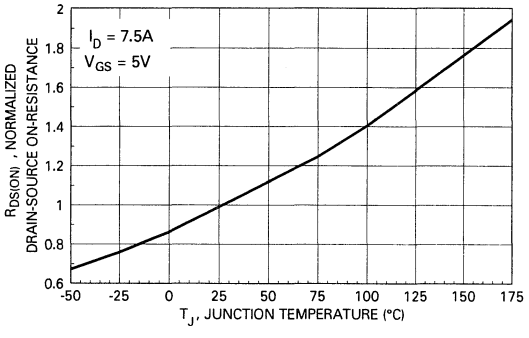


Figure 3. On-Resistance Variation with Temperature

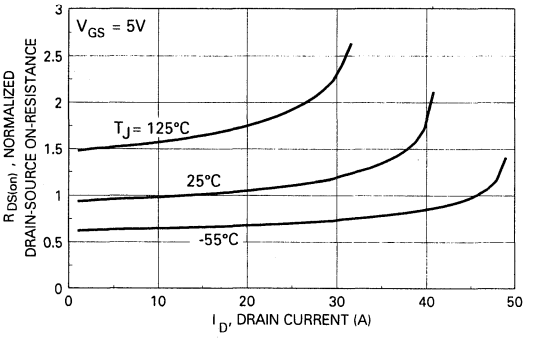


Figure 4. On-Resistance Variation with Drain Current and Temperature

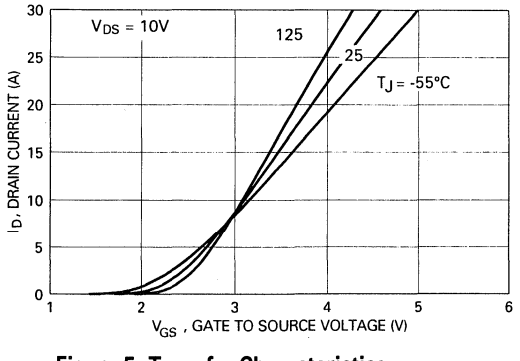


Figure 5. Transfer Characteristics

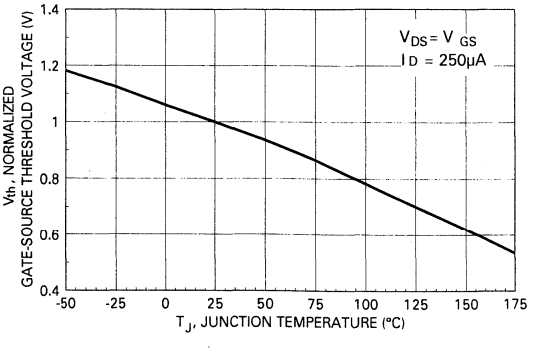


Figure 6. Gate Threshold Variation with Temperature

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Typical Electrical Characteristics (continued)

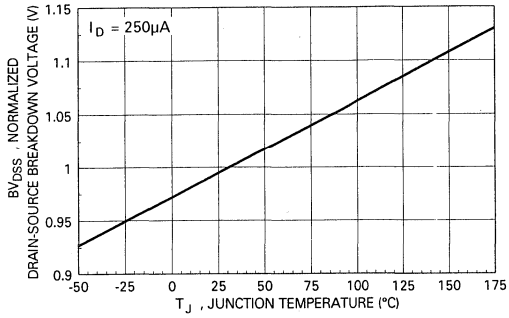


Figure 7. Breakdown Voltage Variation with Temperature

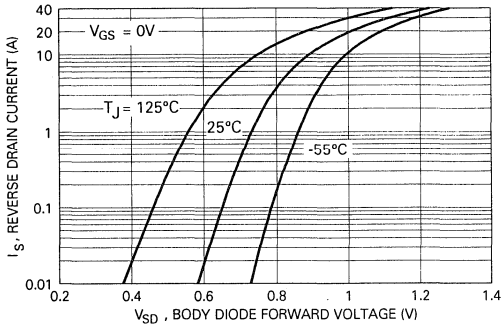


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

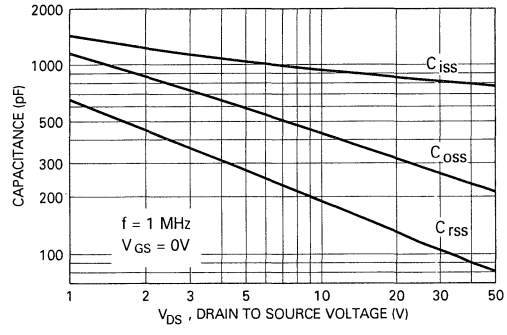


Figure 9. Capacitance Characteristics

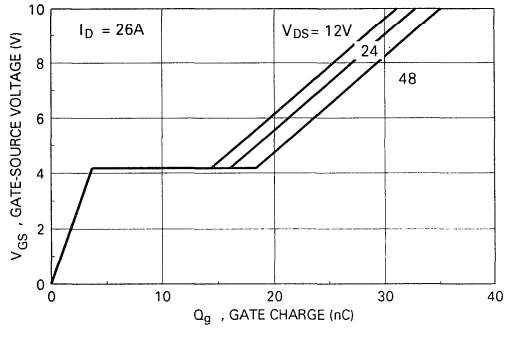


Figure 10. Gate Charge Characteristics

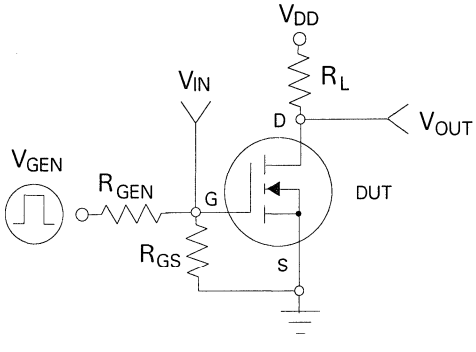


Figure 11. Switching Test Circuit

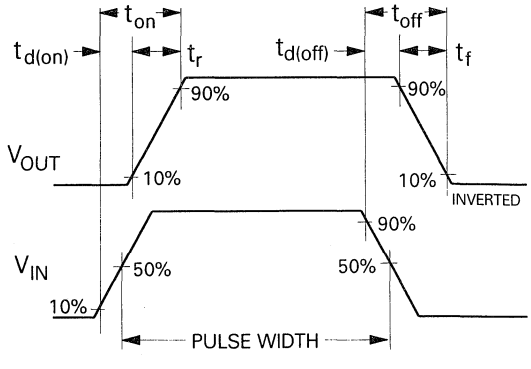


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

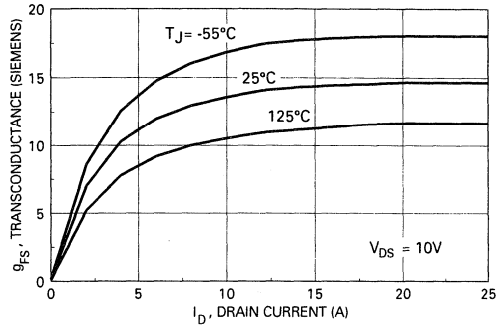


Figure 13. Transconductance Variation with Drain Current and Temperature

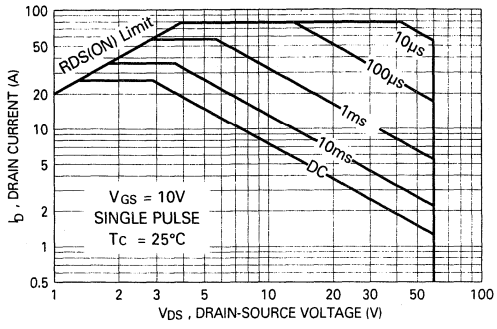


Figure 14. Maximum Safe Operating Area

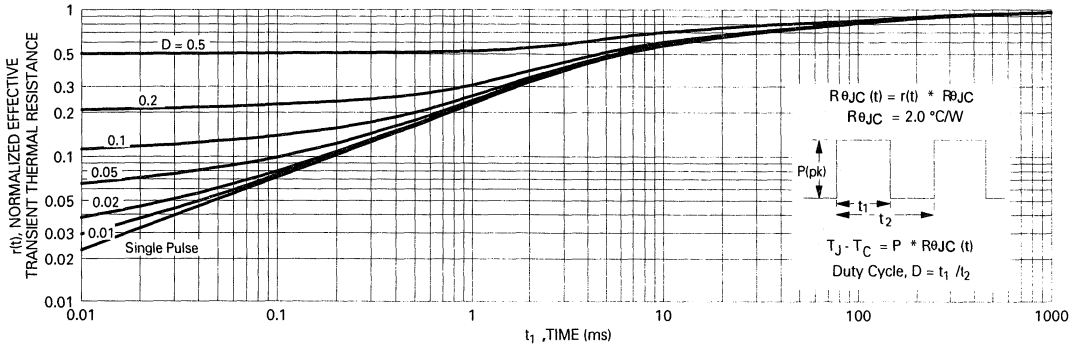


Figure 15. Transient Thermal Response Curve

8

National Semiconductor™

January 1996

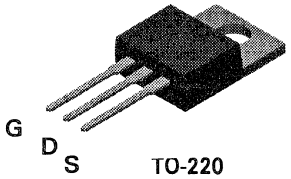
NDP603AL / NDB603AL
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

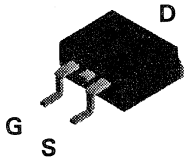
These N-Channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

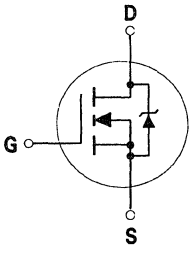
- 25A, 30V. $R_{DS(ON)}$ = 0.022Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low $R_{DS(ON)}$.
- 175°C maximum junction temperature rating.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP603AL	NDB603AL	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
I_D	Drain Current - Continuous	25 (Note 1)		A
	- Pulsed	100		
P_D	Total Power Dissipation @ T_C = 25°C	50		W
	Derate above 25°C	0.4		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 2)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 25 A			100	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				25	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.1	1.5	3	V
		T_J = 125°C	0.7	1.1	2.2	
		V_{DS} = V_{GS}, I_D = 10 mA	1.4	1.85	3	
		T_J = 125°C	1	1.5	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 25 A		0.019	0.022	Ω
		T_J = 125°C		0.028	0.045	
		V_{GS} = 4.5 V, I_D = 10 A		0.031	0.04	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	15			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 25 A		18		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1100		pF
C_{oss}	Output Capacitance			540		pF
C_{rss}	Reverse Transfer Capacitance			175		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 25 A, V_{GS} = 10 V, R_{GEN} = 24 Ω		15	30	ns
t_r	Turn - On Rise Time			70	110	ns
$t_{D(off)}$	Turn - Off Delay Time			90	150	ns
t_f	Turn - Off Fall Time			80	130	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 25 A, V_{GS} = 10 V		28	40	nC
Q_{gs}	Gate-Source Charge			5	7	nC
Q_{gd}	Gate-Drain Charge			7	10	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				25	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 25 A (Note 2)			1.3	V

Note:
1. Maximum DC current limited by the package.
2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

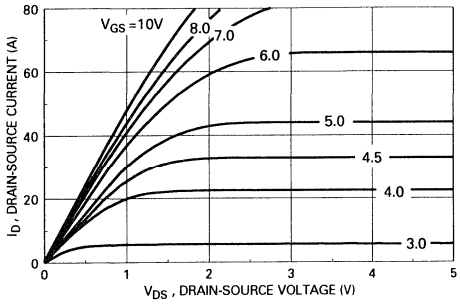


Figure 1. On-Region Characteristics.

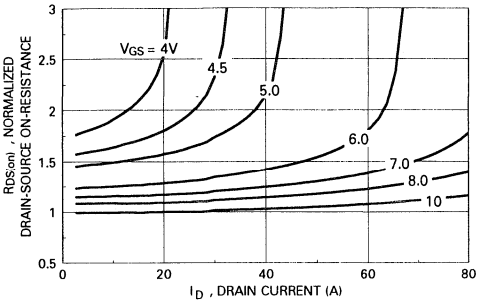


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

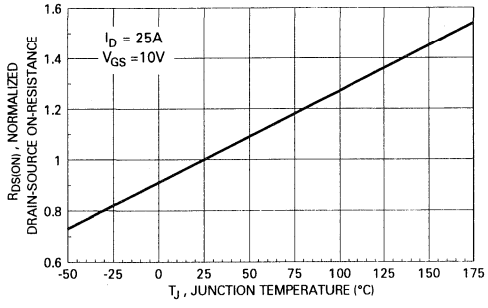


Figure 3. On-Resistance Variation with Temperature.

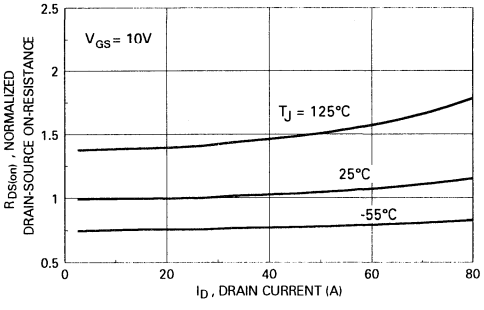


Figure 4. On-Resistance Variation with Drain Current and Temperature.

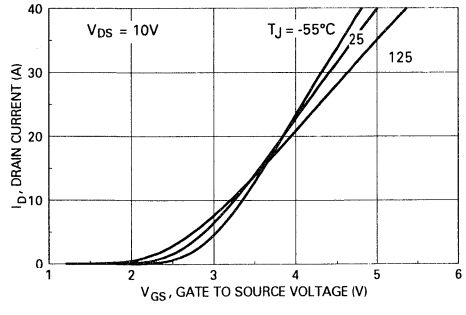


Figure 5. Drain Current Variation with Gate Voltage and Temperature.

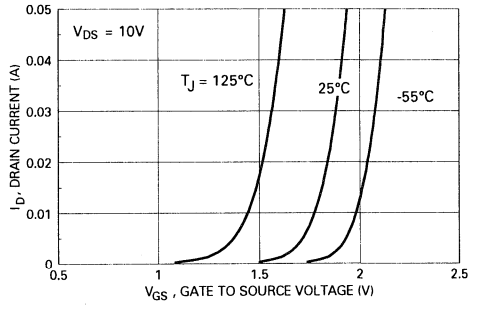


Figure 6. Sub-threshold Drain Current Variation with Gate Voltage and Temperature.

Typical Electrical Characteristics (continued)

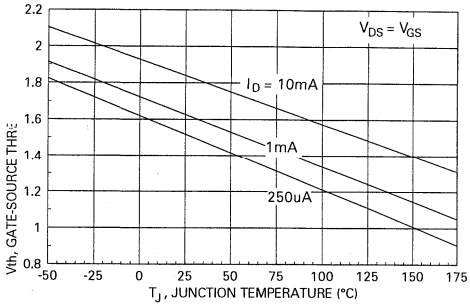


Figure 7. Gate Threshold Variation with Temperature

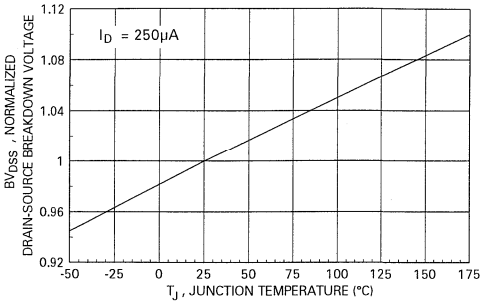


Figure 8. Breakdown Voltage Variation with Temperature.

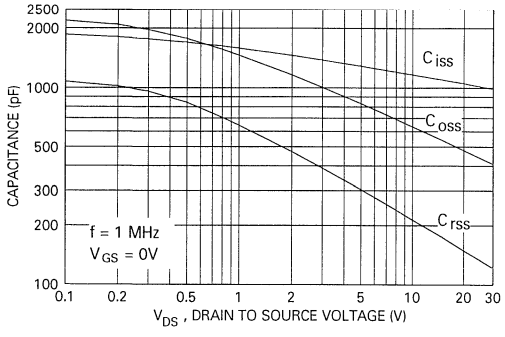


Figure 9. Capacitance Characteristics.

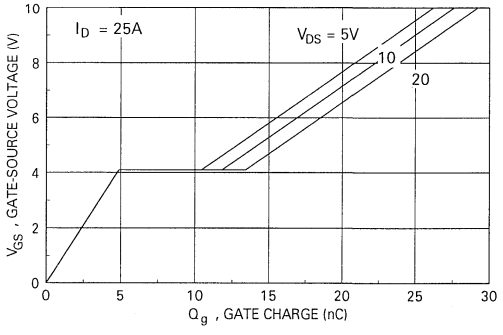


Figure 10. Gate Charge Characteristics.

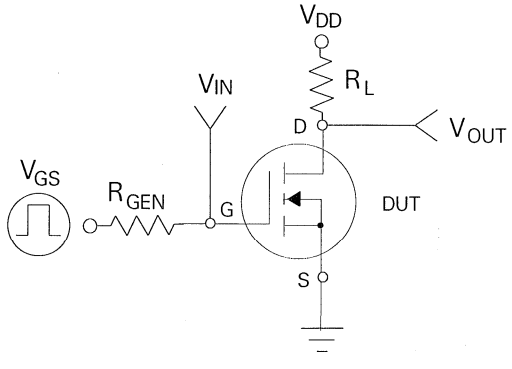


Figure 11. Switching Test Circuit

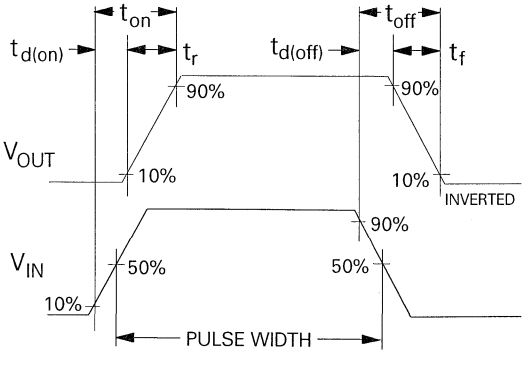


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

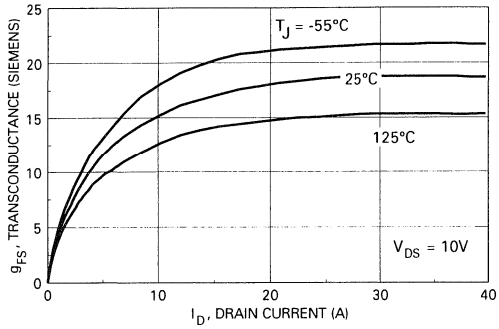


Figure 13. Transconductance Variation with Drain Current and Temperature

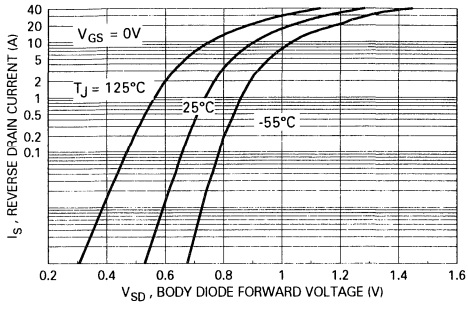


Figure 14. Body Diode Forward Voltage Variation with Current and Temperature

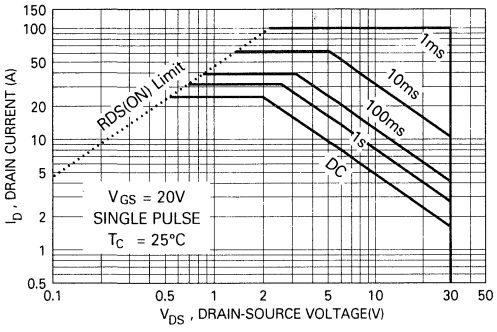


Figure 15. Maximum Safe Operating Area

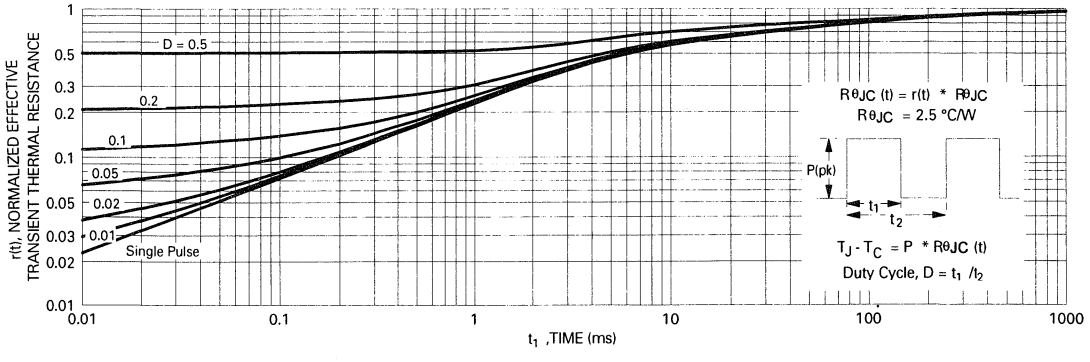


Figure 16. Transient Thermal Response Curve

National Semiconductor™

July 1996

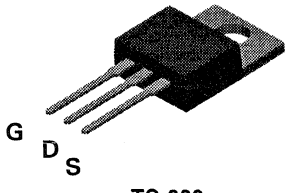
NDP4050 / NDB4050
N-Channel Enhancement Mode Field Effect Transistor

General Description

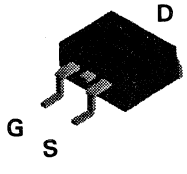
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

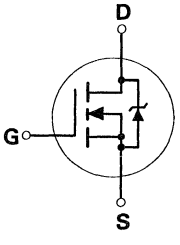
- 15A, 50V. $R_{DS(ON)}$ = 0.10Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings

T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP4050	NDB4050	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive ($t_P < 50$ µs)	± 40		
I_D	Drain Current - Continuous	± 15		A
	- Pulsed	± 45		
P_D	Total Power Dissipation	50		W
	Derate above 25°C	0.33		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 15 A			40	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				15	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
		T_J = 125°C	1.4	2.4	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.5 A		0.078	0.1	Ω
		T_J = 125°C		0.12	0.165	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.5 A	3	5.7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25, V_{GS} = 0 V, f = 1.0 MHz		370	450	pF
C_{oss}	Output Capacitance			165	200	pF
C_{rss}	Reverse Transfer Capacitance			50	100	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 15 A, V_{GS} = 10 V, R_{GEN} = 25 Ω		8	20	ns
t_r	Turn - On Rise Time			70	100	ns
$t_{D(off)}$	Turn - Off Delay Time			18	30	ns
t_f	Turn - Off Fall Time			37	50	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 15 A, V_{GS} = 10 V		12.7	17	nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			7		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				45	A
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.5 A (Note 1)		0.95	1.3	V
		T_J = 125°C		0.88	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 15 A, dI_F/dt = 100 A/µs	25	46	100	ns
I_{rr}	Reverse Recovery Current		1.5	3.4	7	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

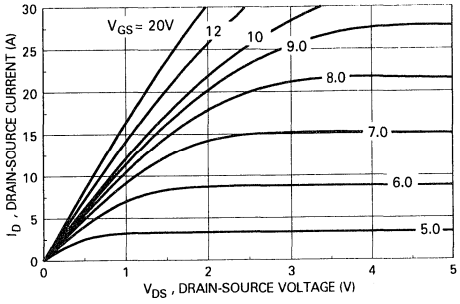


Figure 1. On-Region Characteristics.

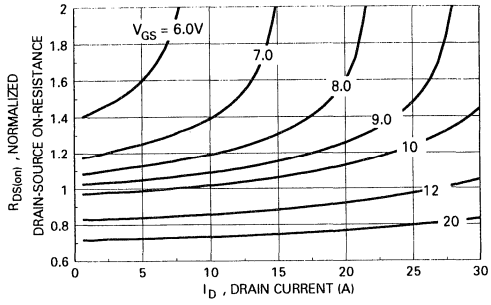


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

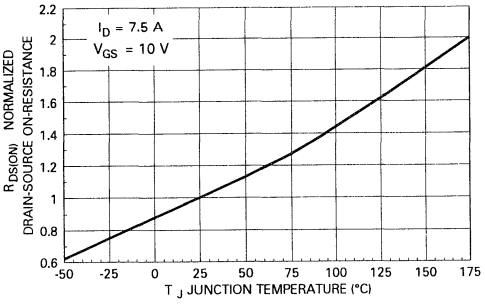


Figure 3. On-Resistance Variation with Temperature.

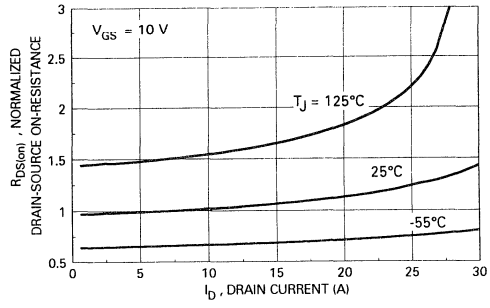


Figure 4. On-Resistance Variation with Drain Current and Temperature.

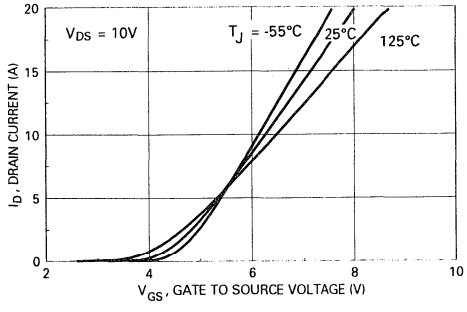


Figure 5. Drain Current Variation with Gate Voltage and Temperature.

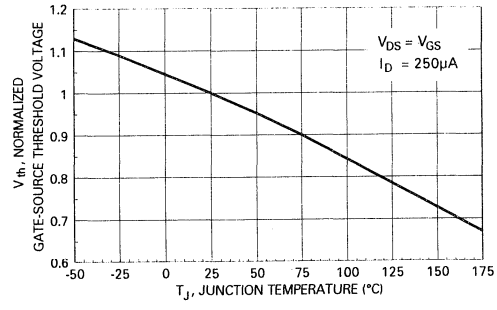


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

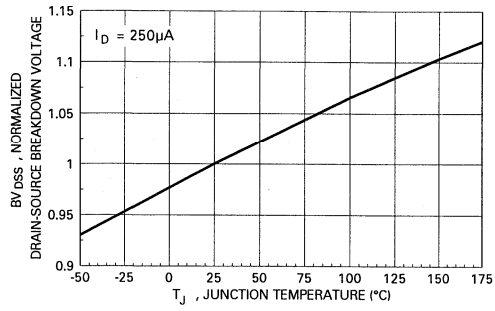


Figure 7. Breakdown Voltage Variation with Temperature.

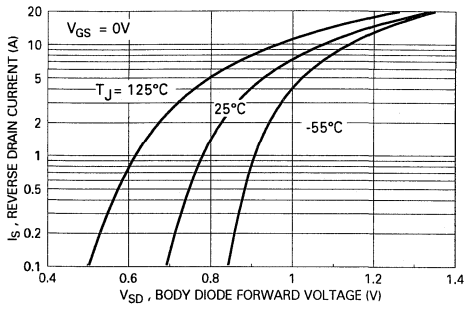


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

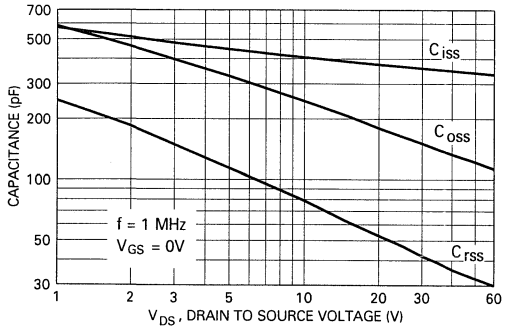


Figure 9. Capacitance Characteristics.

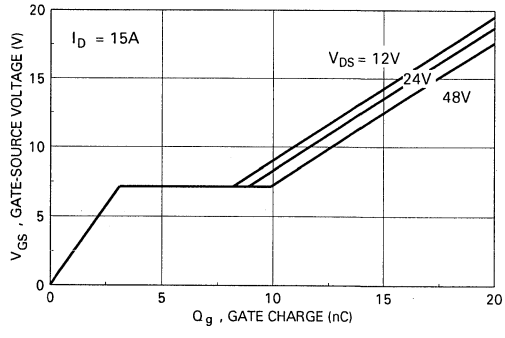


Figure 10. Gate Charge Characteristics.

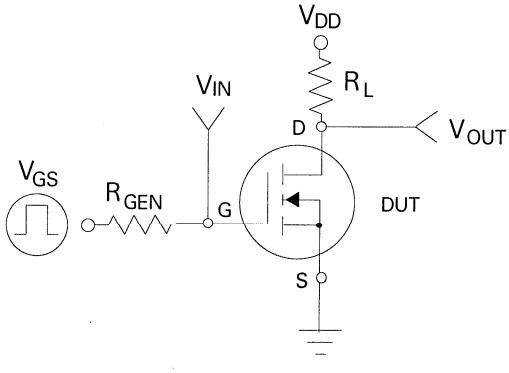


Figure 11. Switching Test Circuit.

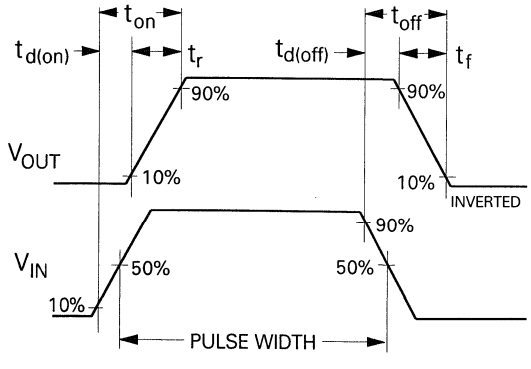


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

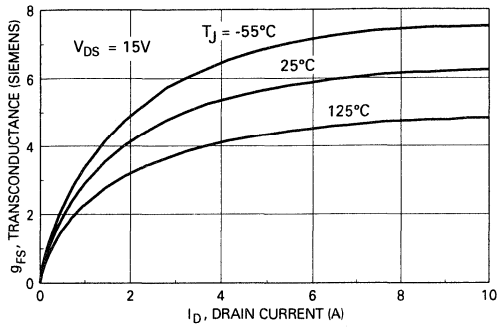


Figure 13. Transconductance Variation with Drain Current and Temperature.

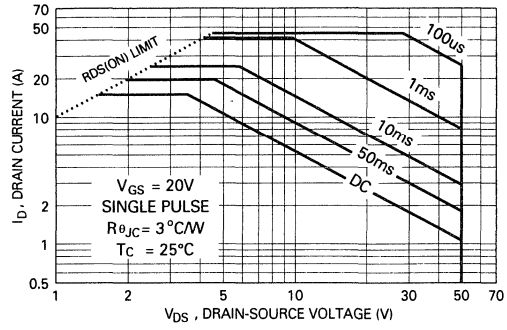


Figure 14. Maximum Safe Operating Area.

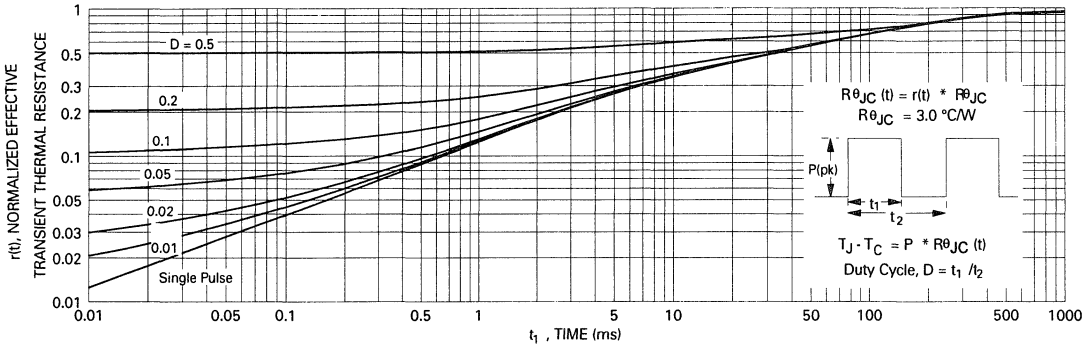


Figure 15. Transient Thermal Response Curve.

National Semiconductor™

April 1996

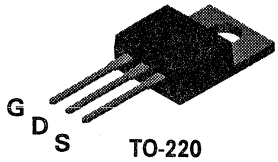
NDP4050L / NDB4050L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

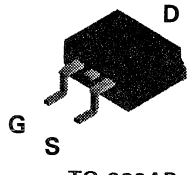
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

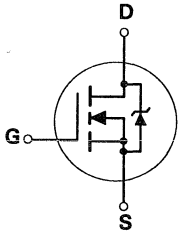
- 15A, 50V. $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = 5V
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP4050L	NDB4050L	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	±16		V
	- Nonrepetitive (t_P < 50 μs)	±25		
I_D	Drain Current - Continuous	15		A
	- Pulsed	45		
P_D	Total Power Dissipation @ T_C = 25°C	50		W
	Derate above 25°C	0.33		W/°C
T_J,T_{STG}	Operating and Storage Temperature	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 15 A			40	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				15	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		T_J =125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	2	V
		T_J =125°C	0.65	1.1	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 7.5 A		0.085	0.1	Ω
		T_J =125°C		0.14	0.16	
		V_{GS} = 10 V, I_D = 15 A		0.07	0.08	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.5 A	3	8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		510	600	pF
C_{oss}	Output Capacitance			170	200	pF
C_{rss}	Reverse Transfer Capacitance			50	100	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 15 A, V_{GS} = 5 V, R_{GEN} = 51 Ω, R_{GS} = 51 Ω		9	20	nS
t_r	Turn - On Rise Time			151	250	nS
$t_{D(off)}$	Turn - Off Delay Time			35	100	nS
t_f	Turn - Off Fall Time			61	150	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 15 A, V_{GS} = 5 V		11	17	nC
Q_{gs}	Gate-Source Charge			2		nC
Q_{gd}	Gate-Drain Charge			6.1		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				45	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.5 A (Note 1)		0.95	1.3	V
		T_J = 125°C		0.88	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 15 A, dI_F/dt = 100 A/µs		51	100	ns
I_{rr}	Reverse Recovery Current			3.6	7	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

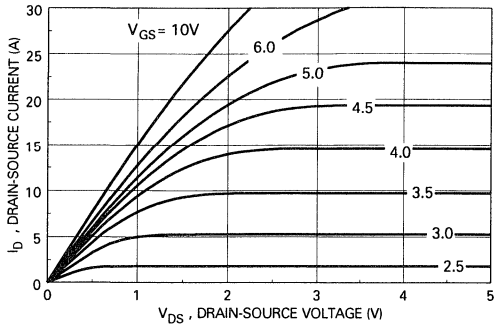


Figure 1. On-Region Characteristics

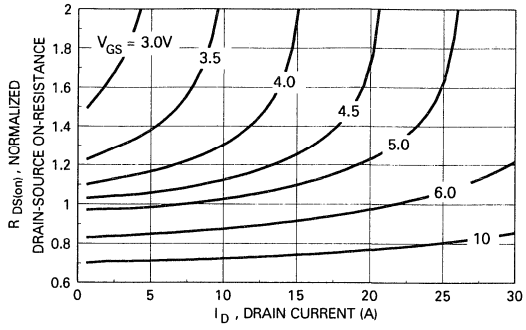


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

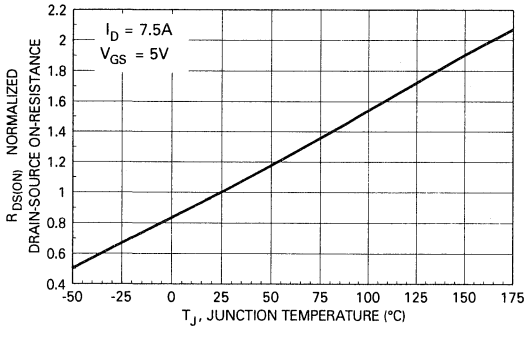


Figure 3. On-Resistance Variation with Temperature

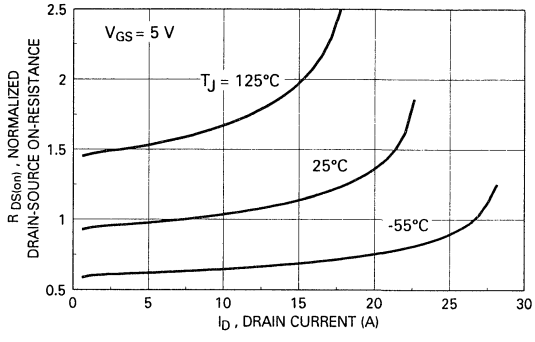


Figure 4. On-Resistance Variation with Drain Current and Temperature

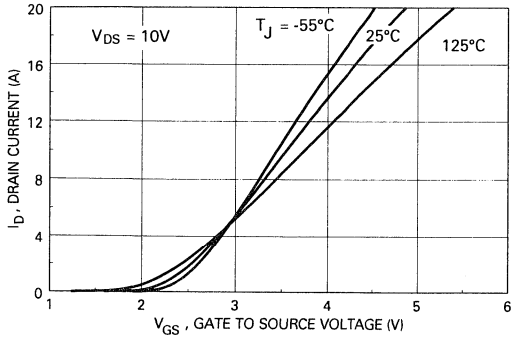


Figure 5. Transfer Characteristics

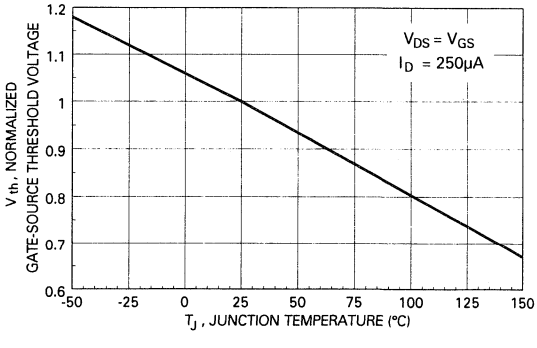


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

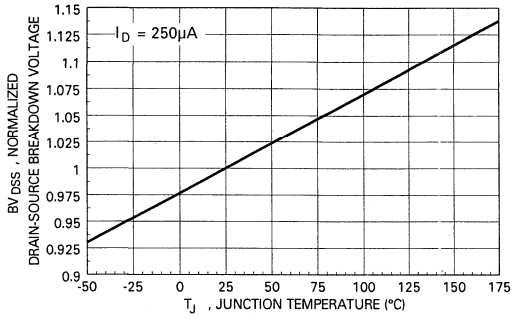


Figure 7. Breakdown Voltage Variation with Temperature

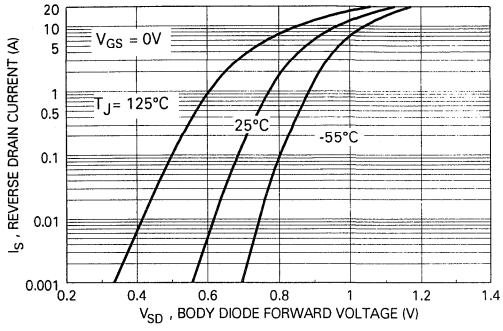


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

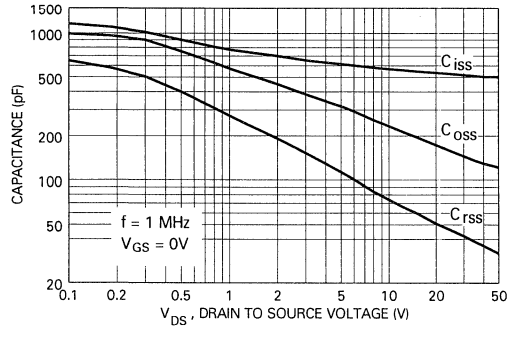


Figure 9. Capacitance Characteristics

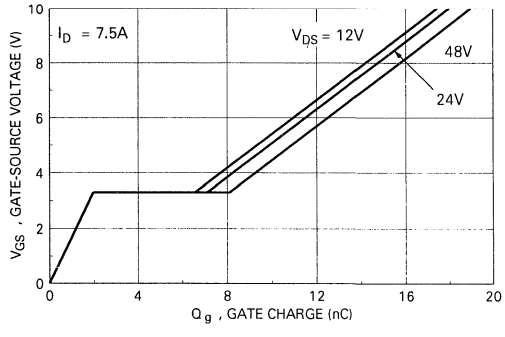


Figure 10. Gate Charge Characteristics

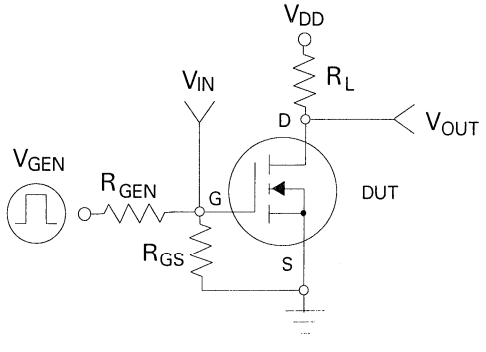


Figure 11. Switching Test Circuit

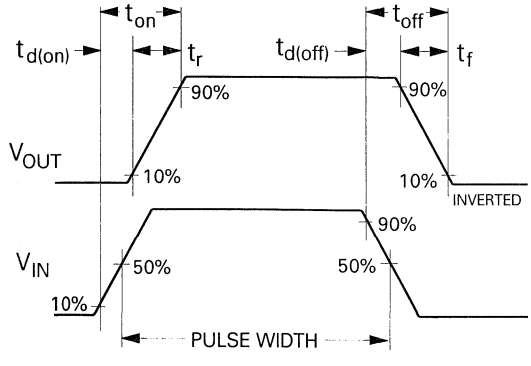


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

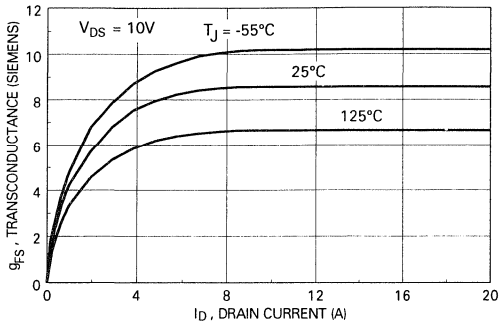


Figure 13. Transconductance Variation with Drain Current and Temperature

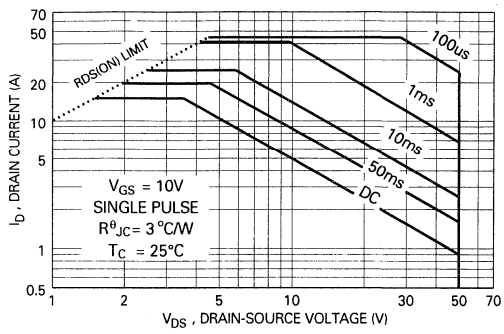


Figure 14. Maximum Safe Operating Area

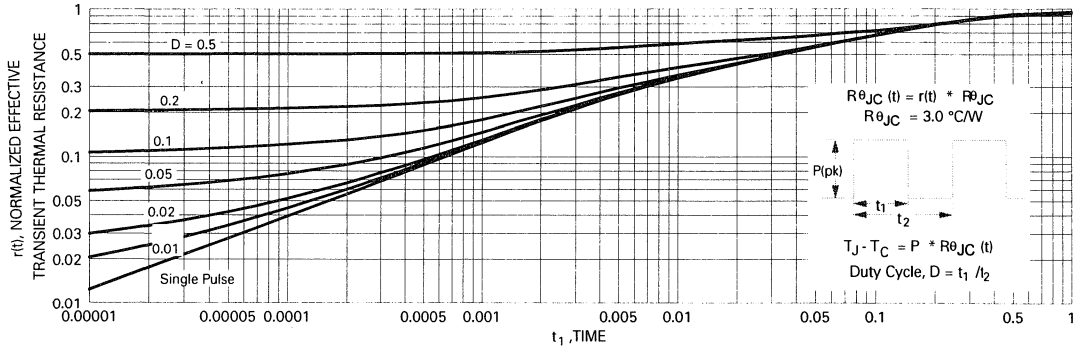


Figure 15. Transient Thermal Response Curve

National Semiconductor™

July 1996

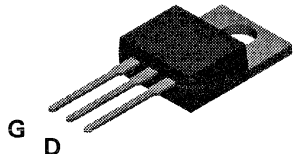
NDP4060 / NDB4060
N-Channel Enhancement Mode Field Effect Transistor

General Description

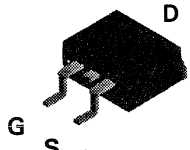
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

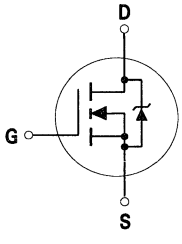
- 15A, 60V. $R_{DS(ON)}$ = 0.10Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP4060	NDB4060	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_P < 50 μs)	± 40		
I_D	Drain Current - Continuous	± 15		A
	- Pulsed	± 45		
P_D	Total Power Dissipation	50		W
	Derate above 25°C	0.33		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 15 A			40	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				15	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
		T_J = 125°C	1.4	2.4	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 7.5 A		0.078	0.1	Ω
		T_J = 125°C		0.12	0.165	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.5 A	3	5.7		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25, V_{GS} = 0 V, f = 1.0 MHz		370	450	pF
C_{oss}	Output Capacitance			165	200	pF
C_{rss}	Reverse Transfer Capacitance			50	100	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 15 A, V_{GS} = 10 V, R_{GEN} = 25 Ω		8	20	ns
t_r	Turn - On Rise Time			70	100	ns
$t_{D(off)}$	Turn - Off Delay Time			18	30	ns
t_f	Turn - Off Fall Time			37	50	ns
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 15 A, V_{GS} = 10 V		12.7	17	nC
Q_{gs}	Gate-Source Charge			3.2		nC
Q_{gd}	Gate-Drain Charge			7		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				45	A
V_{SD}	Source-Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.5 A (Note 1)		0.95	1.3	V
		T_J = 125°C		0.88	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 15 A, dI_F/dt = 100 A/µs	25	46	100	ns
I_{rr}	Reverse Recovery Current		1.5	3.4	7	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

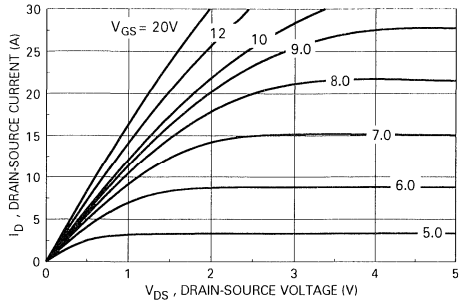


Figure 1. On-Region Characteristics.

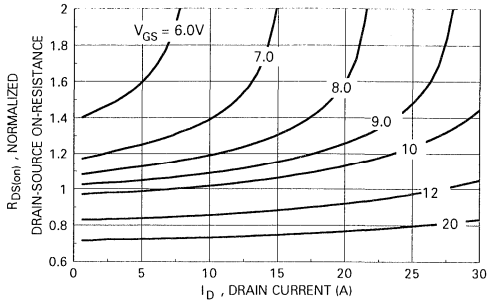


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.

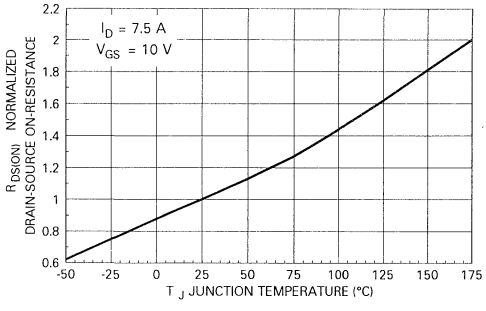


Figure 3. On-Resistance Variation with Temperature.

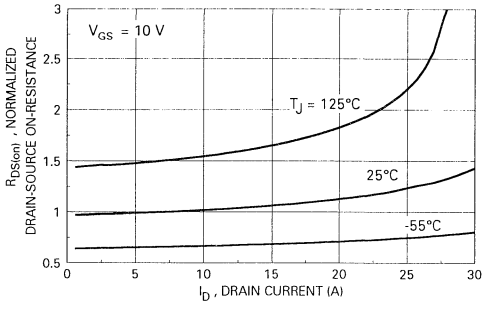


Figure 4. On-Resistance Variation with Drain Current and Temperature.

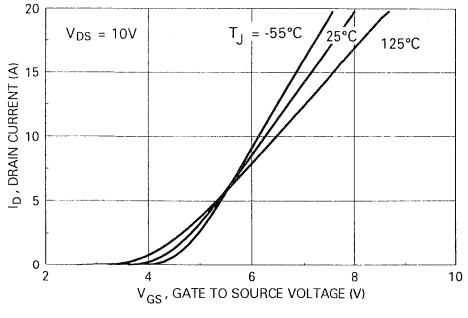


Figure 5. Transfer Characteristics

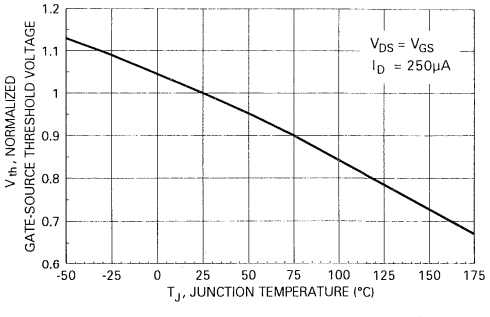


Figure 6. Gate Threshold Variation with Temperature.

Typical Electrical Characteristics (continued)

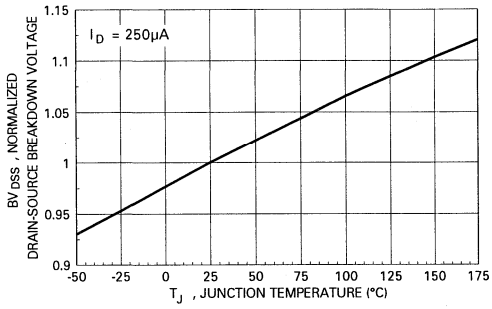


Figure 7. Breakdown Voltage Variation with Temperature.

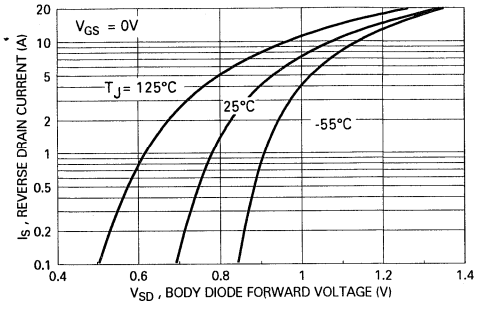


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature.

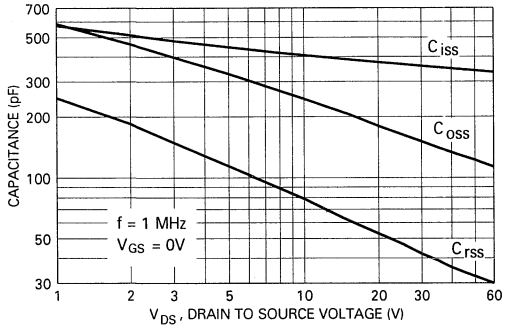


Figure 9. Capacitance Characteristics.

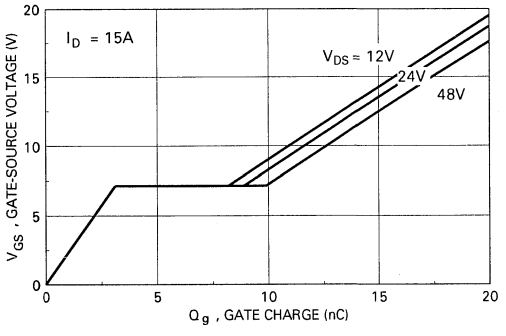


Figure 10. Gate Charge Characteristics.

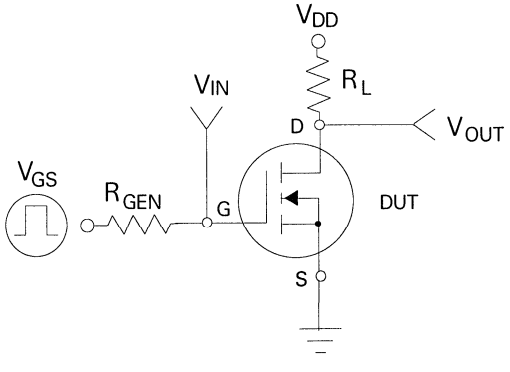


Figure 11. Switching Test Circuit.

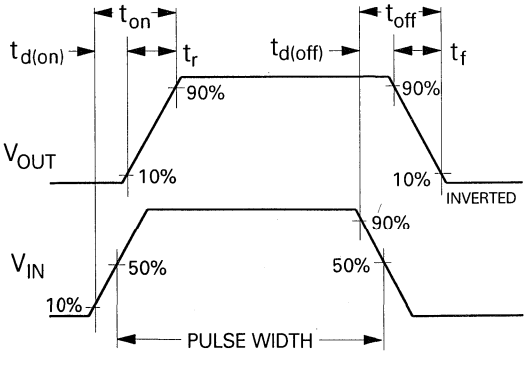


Figure 12. Switching Waveforms.

Typical Electrical Characteristics (continued)

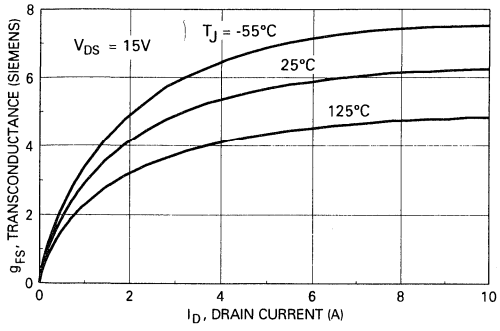


Figure 13. Transconductance Variation with Drain Current and Temperature.

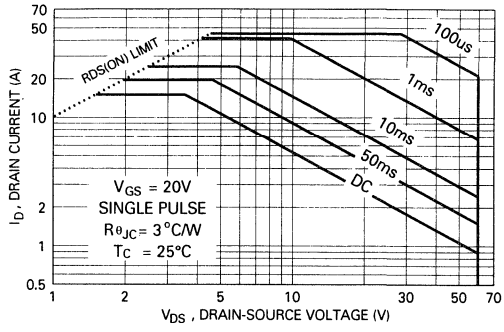


Figure 14. Maximum Safe Operating Area.

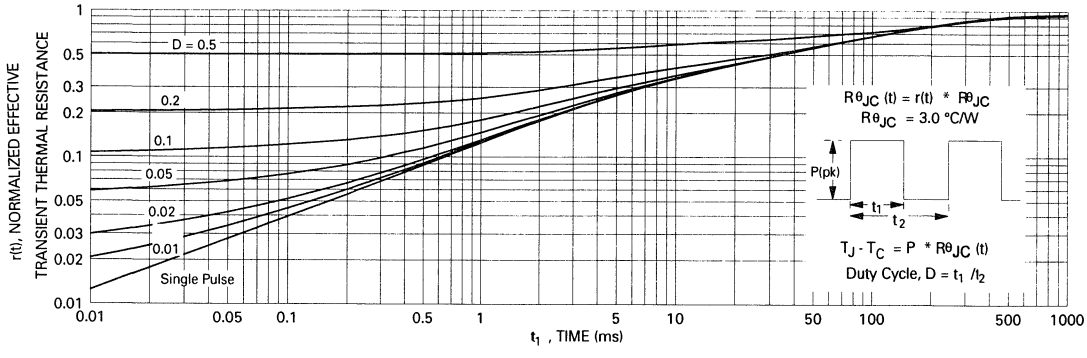


Figure 15. Transient Thermal Response Curve.

National Semiconductor™

April 1996

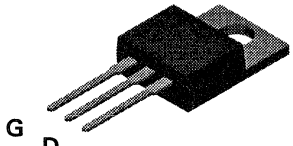
NDP4060L / NDB4060L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

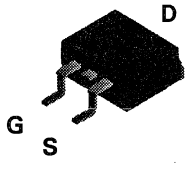
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

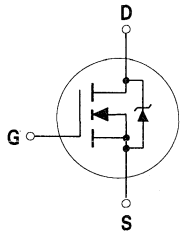
- 15A, 60V. $R_{DS(ON)}$ = 0.1Ω @ V_{GS} = 5V
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP4060L	NDB4060L	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	±16		V
	- Nonrepetitive (t_p < 50 μs)	±25		
I_D	Drain Current - Continuous	15		A
	- Pulsed	45		
P_D	Total Power Dissipation @ T_C = 25°C	50		W
	Derate above 25°C	0.33		W/°C
T_J, T_{STG}	Operating and Storage Temperature	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 15 A			40	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				15	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			250	µA
		T_J =125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS}= 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.5	2	V
		T_J =125°C	0.65	1.1	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 7.5 A		0.085	0.1	Ω
		T_J =125°C		0.14	0.16	
		V_{GS} = 10 V, I_D = 15 A		0.07	0.08	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	15			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 7.5 A	3	8		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		510	600	pF
C_{oss}	Output Capacitance			170	200	pF
C_{rss}	Reverse Transfer Capacitance			50	100	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 15 A, V_{GS} = 5 V, R_{GEN} = 51 Ω, R_{GS} = 51 Ω		9	20	nS
t_r	Turn - On Rise Time			151	250	nS
$t_{D(off)}$	Turn - Off Delay Time			35	100	nS
t_f	Turn - Off Fall Time			61	150	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 15 A, V_{GS} = 5 V		11	17	nC
Q_{gs}	Gate-Source Charge			2		nC
Q_{gd}	Gate-Drain Charge			6.1		nC

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				15	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				45	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.5 A (Note 1)		0.95	1.3	V
		T_J = 125°C		0.88	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 15 A, dI_F/dt = 100 A/µs		51	100	ns
I_{rr}	Reverse Recovery Current			3.6	7	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

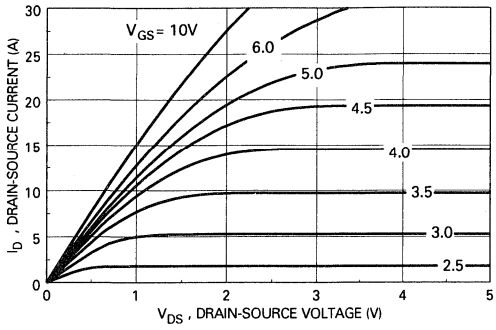


Figure 1. On-Region Characteristics

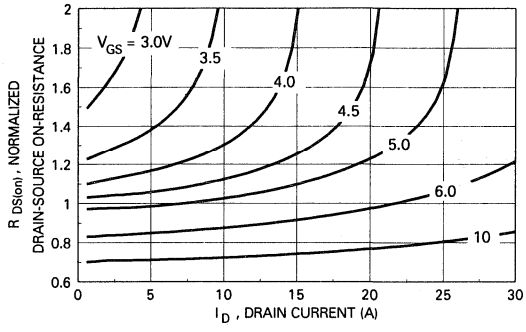


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

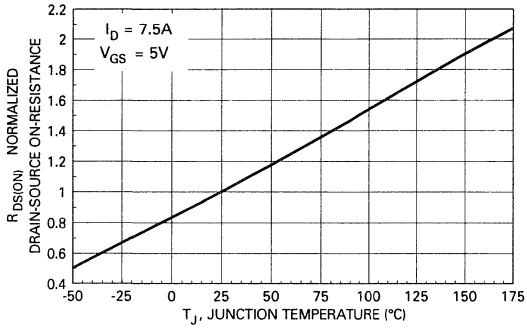


Figure 3. On-Resistance Variation with Temperature

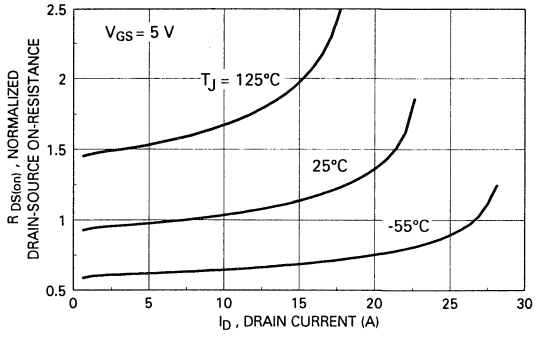


Figure 4. On-Resistance Variation with Drain Current and Temperature

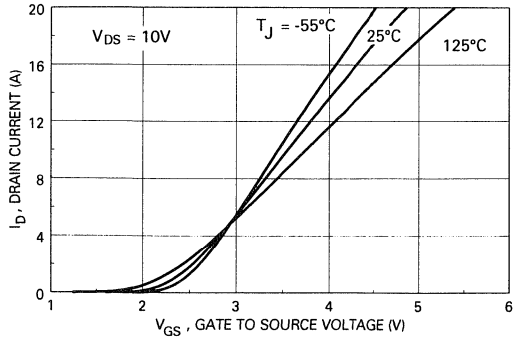


Figure 5. Transfer Characteristics

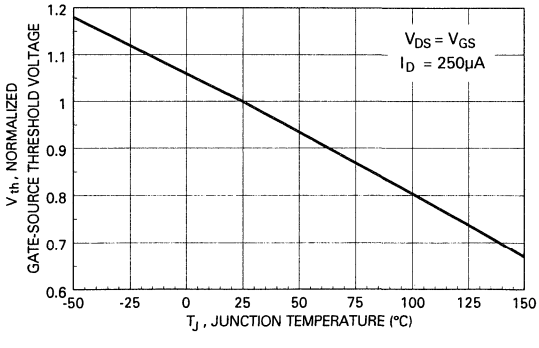


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

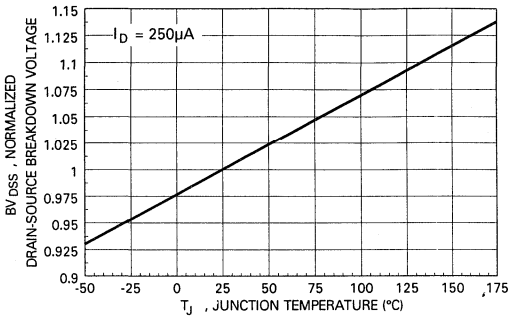


Figure 7. Breakdown Voltage Variation with Temperature

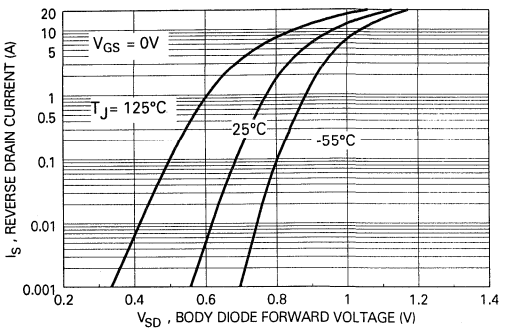


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

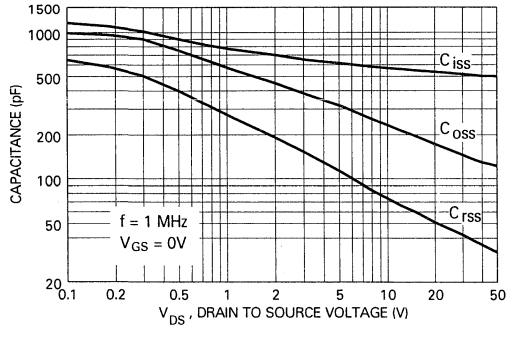


Figure 9. Capacitance Characteristics

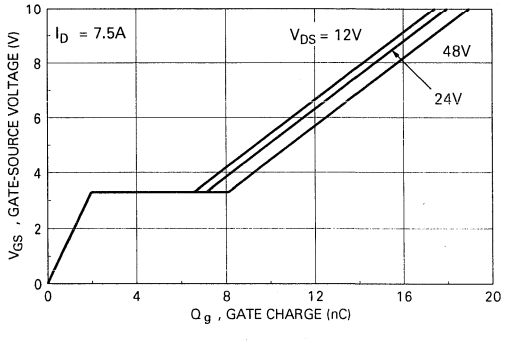


Figure 10. Gate Charge Characteristics

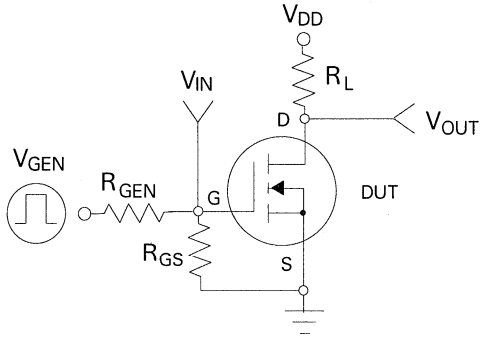


Figure 11. Switching Test Circuit

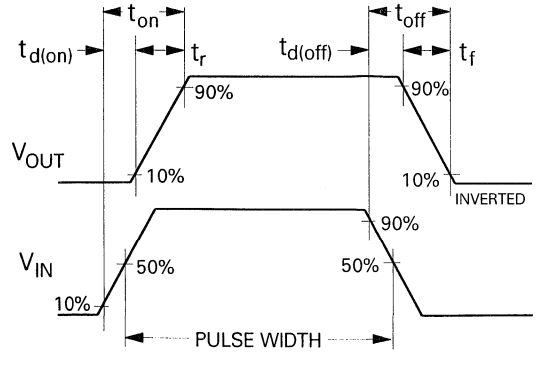


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

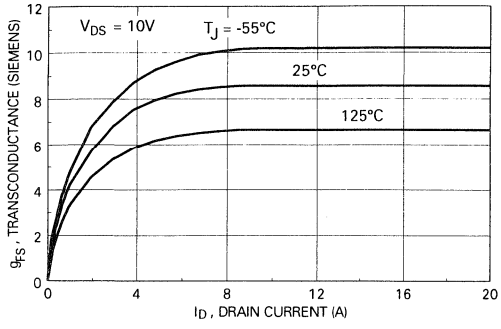


Figure 13. Transconductance Variation with Drain Current and Temperature

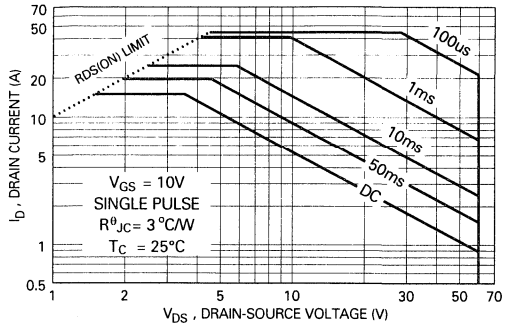


Figure 14. Maximum Safe Operating Area

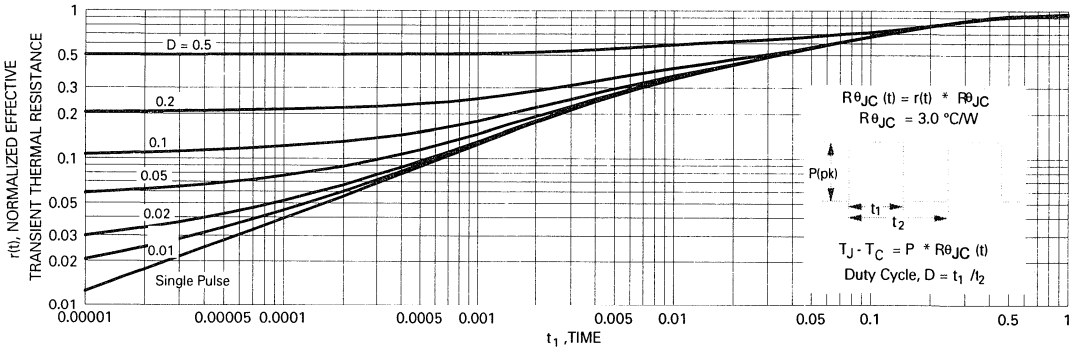


Figure 15. Transient Thermal Response Curve

National Semiconductor™

June 1996

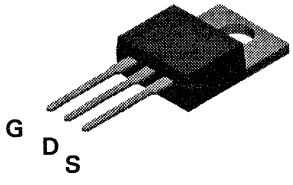
NDP6030L / NDB6030L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

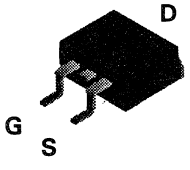
These N-Channel logic level enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications such as DC/DC converters and high efficiency switching circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

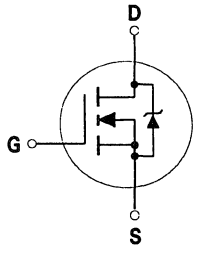
- 52 A, 30 V. $R_{DS(ON)}$ = 0.0135 Ω @ V_{GS}=10 V
  $R_{DS(ON)}$ = 0.020 Ω @ V_{GS}=4.5 V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- High density cell design for extremely low $R_{DS(ON)}$.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6030L	NDB6030L	Units
V_{DSS}	Drain-Source Voltage	30		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
I_D	Drain Current - Continuous	52		A
	- Pulsed	156		
P_D	Total Power Dissipation @ T_C = 25°C	75		W
	Derate above 25°C	0.5		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C
THERMAL CHARACTERISTICS				
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5		°C/W

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 15 V, I_D = 52 A			100	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				52	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	µA
		T_J = -55°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.6	3	V
		T_J = 125°C	0.7	1	2.2	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 26 A		0.011	0.0135	Ω
		T_J = 125°C		0.017	0.024	
		V_{GS} = 4.5 V, I_D = 21 A		0.018	0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
		V_{GS} = 4.5 V, V_{DS} = 10 V	15			
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 26 A		32		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1350		pF
C_{oss}	Output Capacitance			800		pF
C_{rss}	Reverse Transfer Capacitance			300		pF

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 15 V, I_D = 52A, V_{GS} = 10 V, R_{GEN} = 24Ω		8	16	nS
t_r	Turn - On Rise Time			130	250	nS
$t_{D(off)}$	Turn - Off Delay Time			45	90	nS
t_f	Turn - Off Fall Time			108	200	nS
Q_g	Total Gate Charge	V_{DS}= 10 V, I_D = 52 A, V_{GS} =10V		44	60	nC
Q_{gs}	Gate-Source Charge			6		nC
Q_{gd}	Gate-Drain Charge			14		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				52	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				120	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 26 A (Note 1)		0.93	1.3	V
		T_J = 125°C		0.85	1.2	

Note:
1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

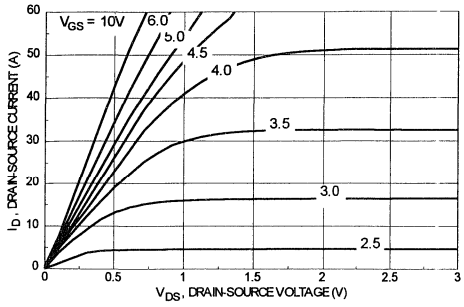


Figure 1. On-Region Characteristics

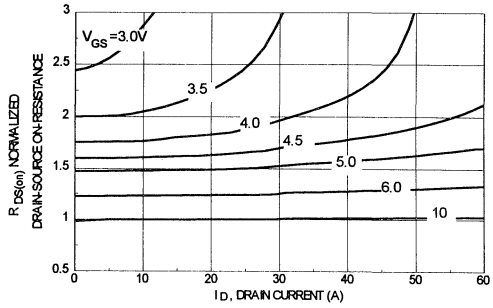


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

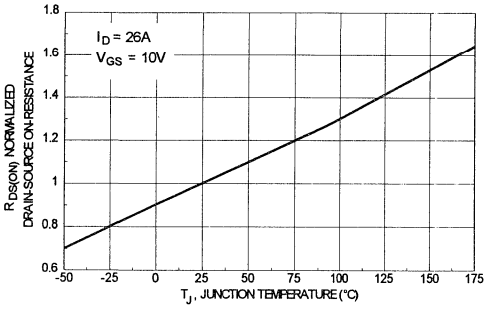


Figure 3. On-Resistance Variation with Temperature

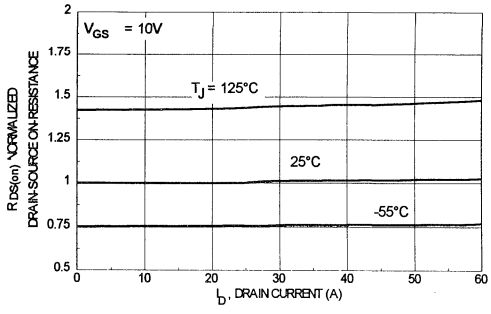


Figure 4. On-Resistance Variation with Drain Current and Temperature

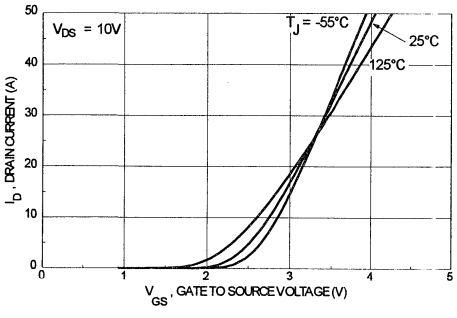


Figure 5. Transfer Characteristics

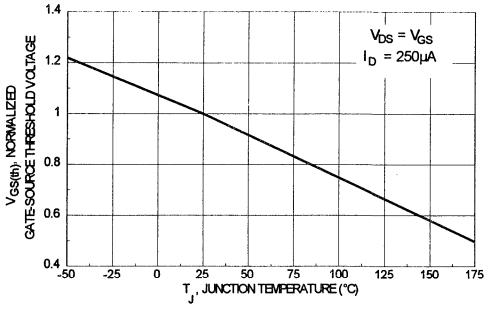


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

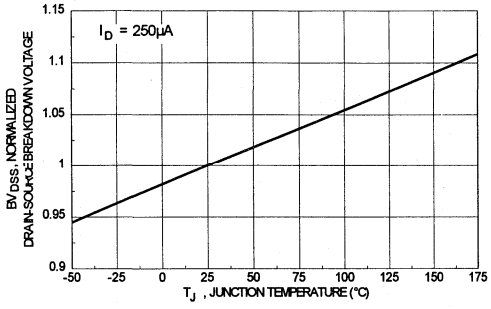


Figure 7. Breakdown Voltage Variation with Temperature

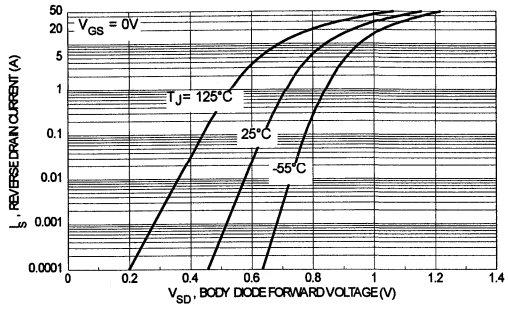


Figure 8. Body Diode Forward Voltage Variation with Source Current and Temperature

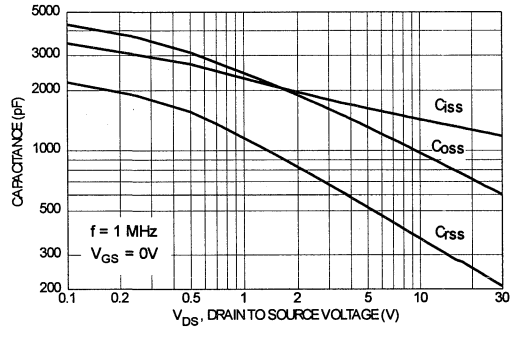


Figure 9. Capacitance Characteristics

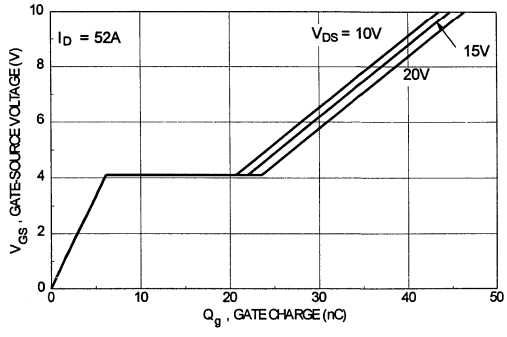


Figure 10. Gate Charge Characteristics

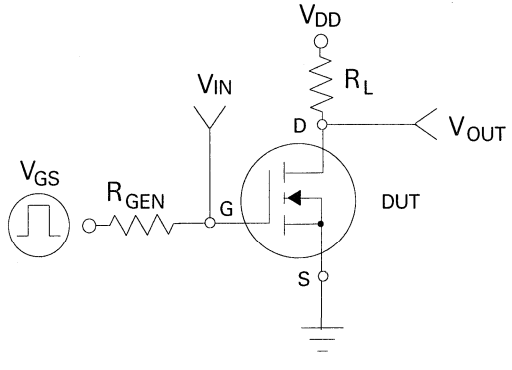


Figure 11. Switching Test Circuit

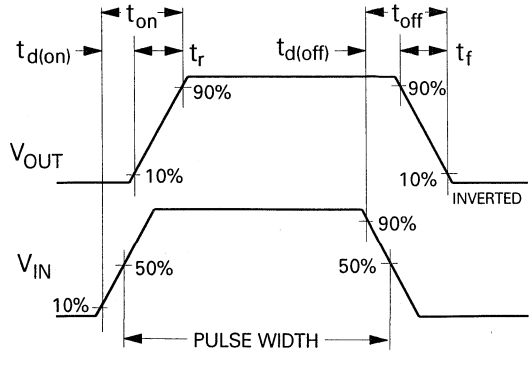


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

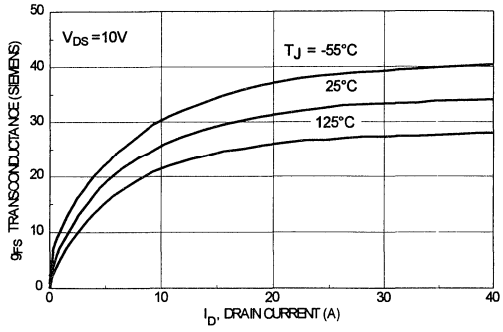


Figure 13. Transconductance Variation with Drain Current and Temperature

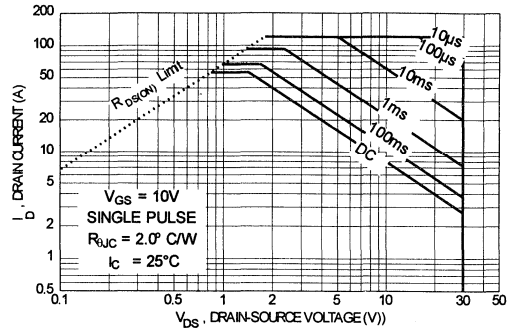


Figure 14. Maximum Safe Operating Area

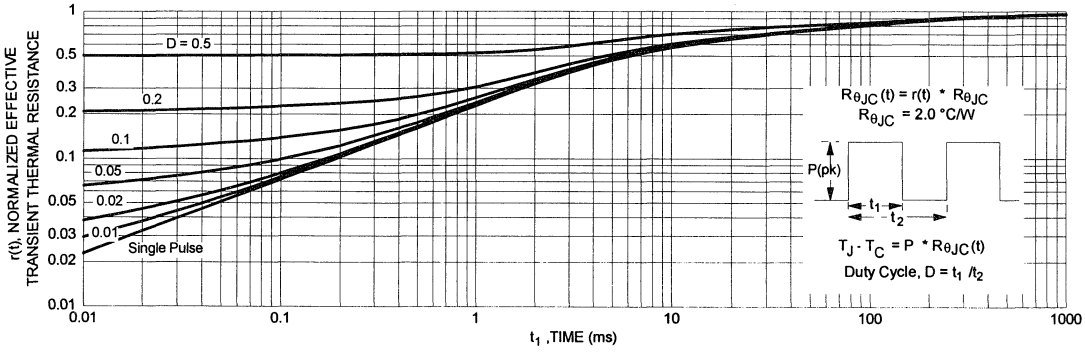


Figure 15. Transient Thermal Response Curve

National Semiconductor™

March 1996

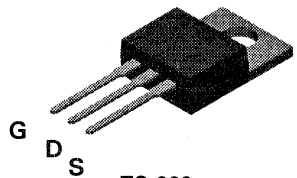
NDP6050 / NDB6050
N-Channel Enhancement Mode Field Effect Transistor

General Description

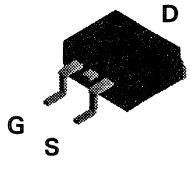
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

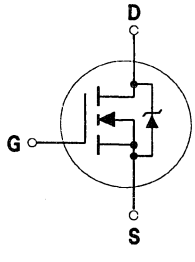
- 48A, 50V. $R_{DS(ON)}$ = 0.025Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6050	NDB6050	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive ($t_p < 50$ µs)	± 40		
I_D	Drain Current - Continuous	48		A
	- Pulsed	144		
P_D	Total Power Dissipation @ T_C = 25°C	100		W
	Derate above 25°C	0.67		W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 48 A			200	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				48	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.9	4	V
		T_J = 125°C	1.4	2.3	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 24 A		0.02	0.025	Ω
		T_J = 125°C		0.032	0.04	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	48			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 24 A	10	19		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1190	1800	pF
C_{oss}	Output Capacitance			475	800	pF
C_{rss}	Reverse Transfer Capacitance			150	400	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 48 A, V_{GS} = 10 V, R_{GEN} = 7.5 Ω		10	20	nS
t_r	Turn - On Rise Time			145	300	nS
$t_{D(off)}$	Turn - Off Delay Time			28	60	nS
t_f	Turn - Off Fall Time			77	150	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 48 A, V_{GS} = 10V		39	70	nC
Q_{gs}	Gate-Source Charge			7.6		
Q_{gd}	Gate-Drain Charge			22		

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				48	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				144	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.8	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 48 A, dI_F/dt = 100 A/µs	35	87	140	ns
I_{rr}	Reverse Recovery Current		2	3.6	8	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

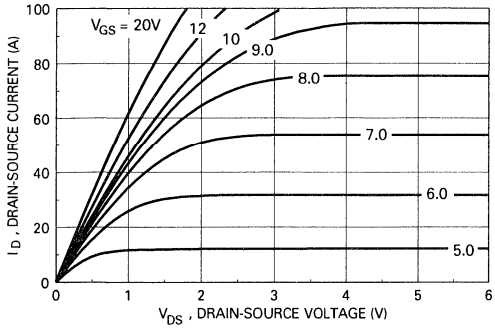


Figure 1. On-Region Characteristics

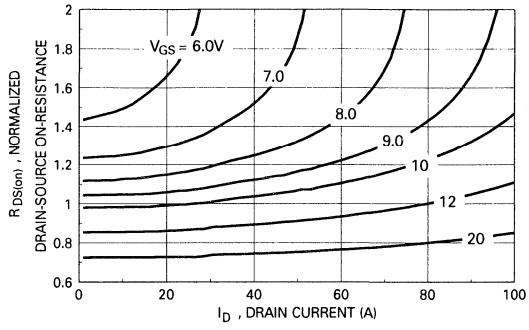


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

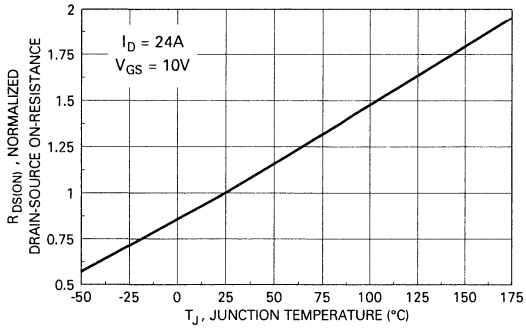


Figure 3. On-Resistance Variation with Temperature

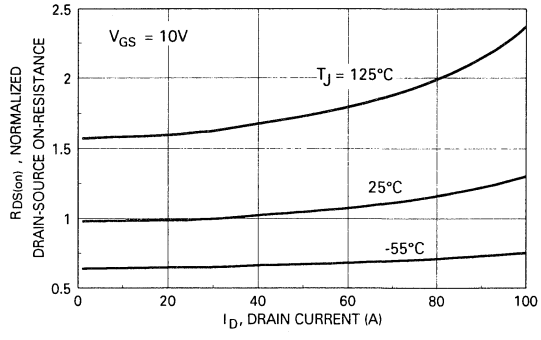


Figure 4. On-Resistance Variation with Drain Current and Temperature

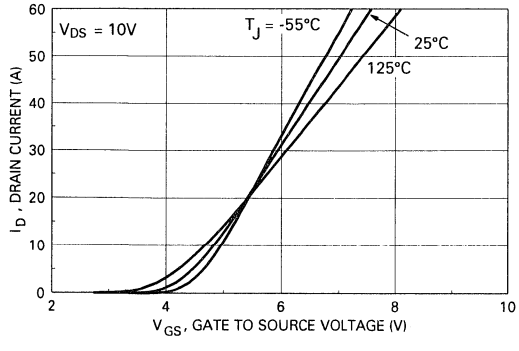


Figure 5. Transfer Characteristics

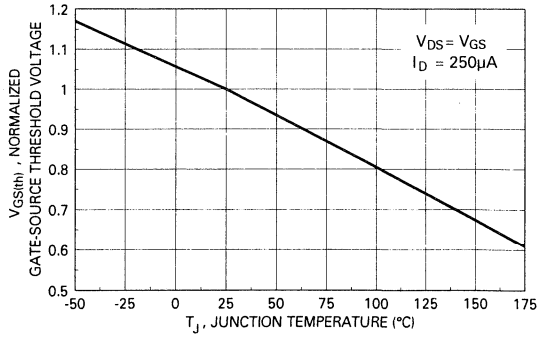


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

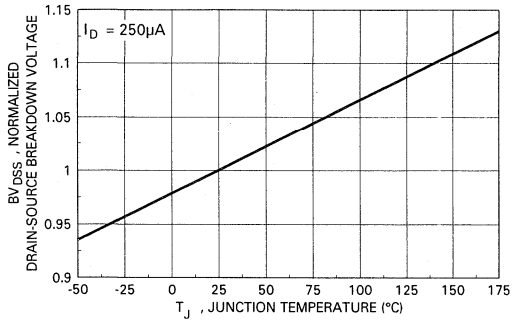


Figure 7. Breakdown Voltage Variation with Temperature

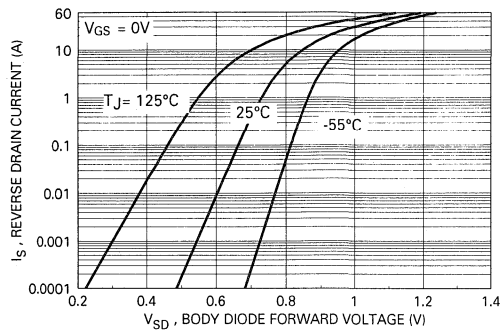


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

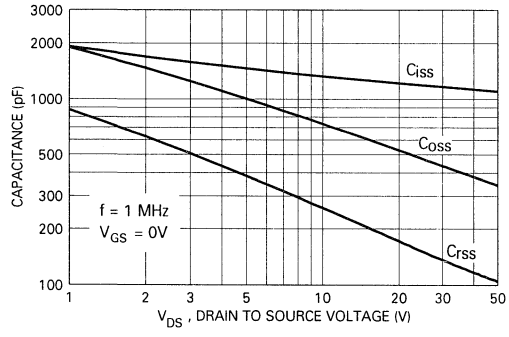


Figure 9. Capacitance Characteristics

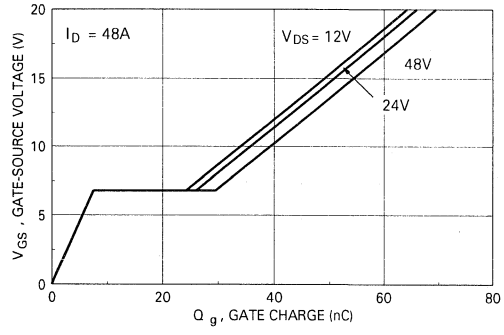


Figure 10. Gate Charge Characteristics

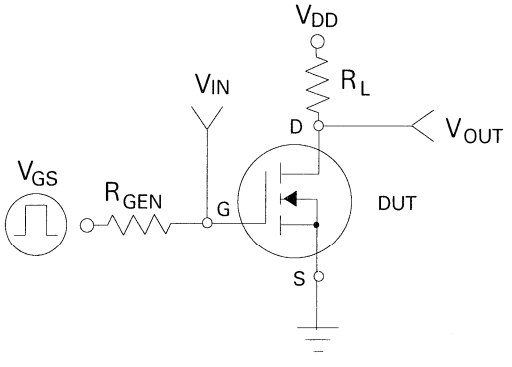


Figure 11. Switching Test Circuit

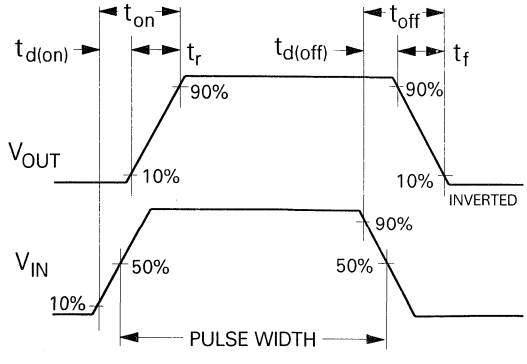


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

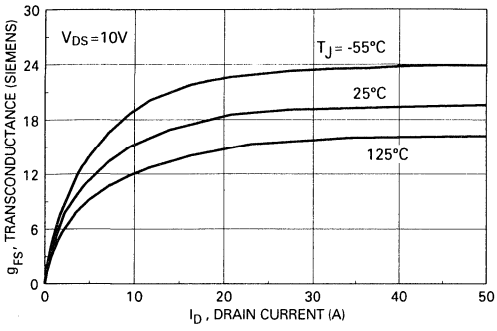


Figure 13. Transconductance Variation with Drain Current and Temperature

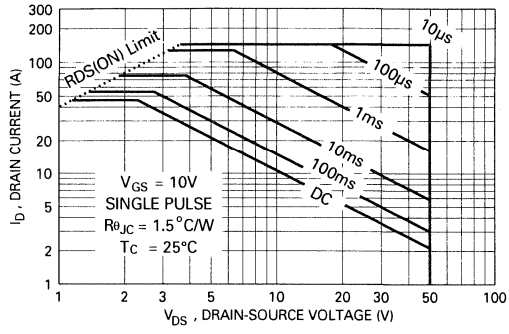


Figure 14. Maximum Safe Operating Area

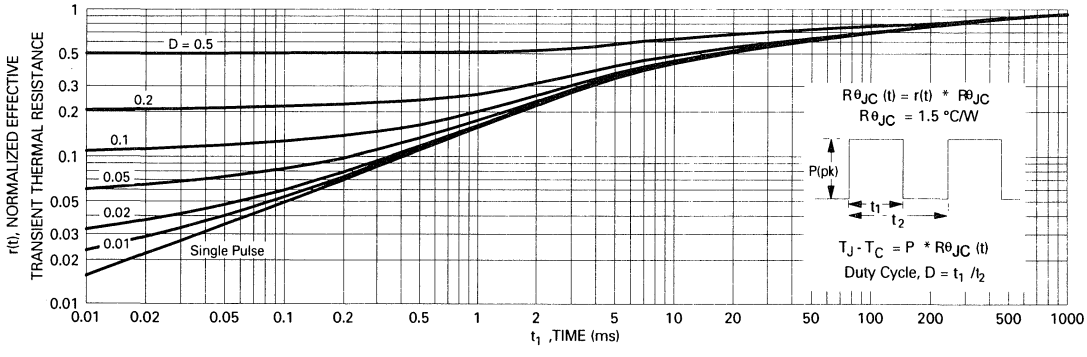


Figure 15. Transient Thermal Response Curve

National Semiconductor™

April 1996

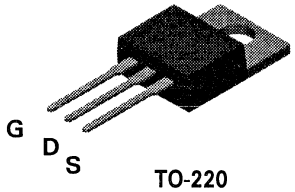
NDP6050L / NDB6050L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

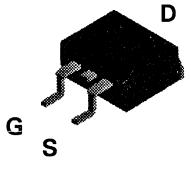
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

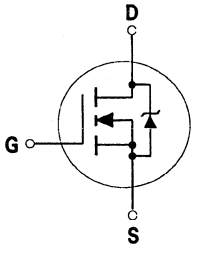
- 48A, 50V. $R_{DS(ON)}$ = 0.025Ω @ V_{GS} = 5V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6050L	NDB6050L	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive (t_p < 50 µs)	± 25		
I_D	Drain Current - Continuous	48		A
	- Pulsed	144		
P_D	Total Power Dissipation @ T_C = 25°C	100		W
	Derate above 25°C	0.67		W/°C
T_J,T_{STG}	Operating and Storage Temperature	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 48 A			200	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				48	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2	V
		T_J = 125°C	0.65		1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 24 A			0.025	Ω
		T_J = 125°C			0.04	
		V_{GS} = 10 V, I_D = 24 A			0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	48			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 24 A	10			S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1630	2000	pF
C_{oss}	Output Capacitance			460	800	pF
C_{rss}	Reverse Transfer Capacitance			150	400	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 48 A, V_{GS} = 5 V, R_{GEN} = 15 Ω, R_{GS} = 15 Ω		15	30	nS
t_r	Turn - On Rise Time			320	500	nS
$t_{D(off)}$	Turn - Off Delay Time			49	100	nS
t_f	Turn - Off Fall Time			161	300	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 48 A, V_{GS} = 5 V		36	60	nC
Q_{gs}	Gate-Source Charge			8.2		nC
Q_{gd}	Gate-Drain Charge			21		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				48	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				144	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A (Note 1)			1.3	V
		T_J = 125°C			1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 48 A, dI_F/dt = 100 A/µs	35	75	140	ns
I_{rr}	Reverse Recovery Current		2	3.6	8	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

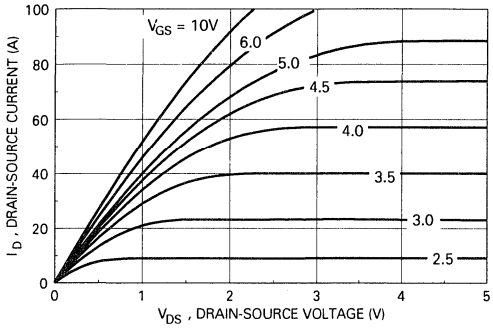


Figure 1. On-Region Characteristics

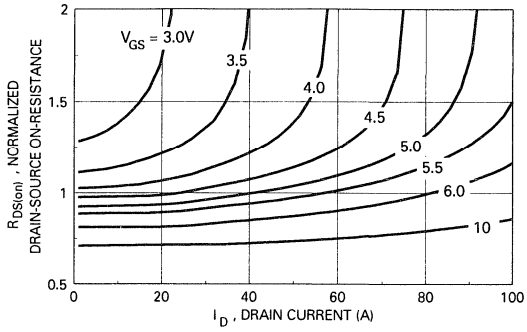


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

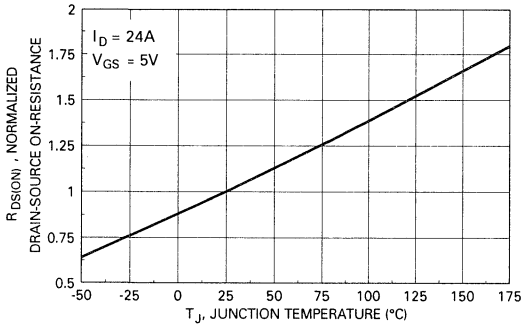


Figure 3. On-Resistance Variation with Temperature

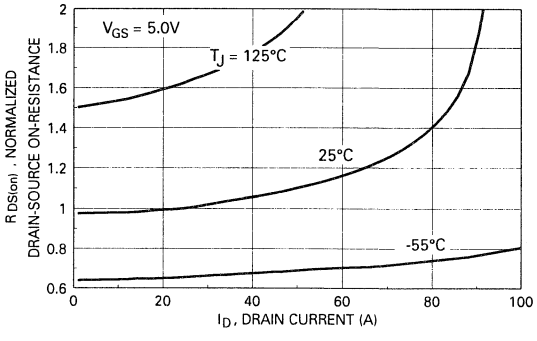


Figure 4. On-Resistance Variation with Drain Current and Temperature

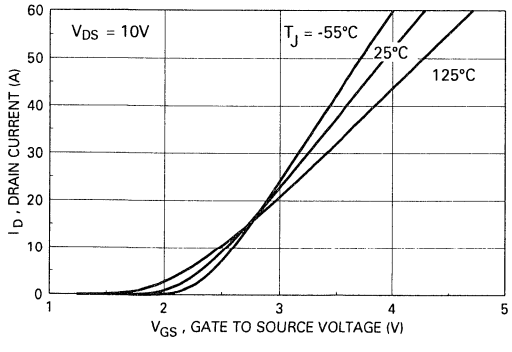


Figure 5. Transfer Characteristics

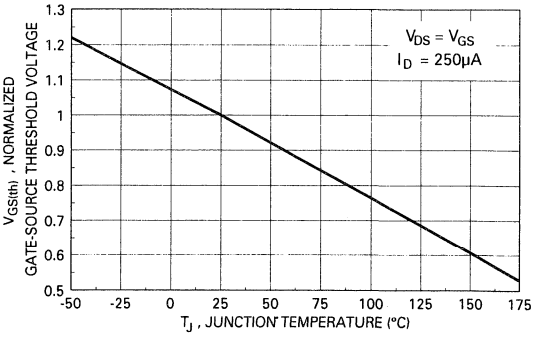


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

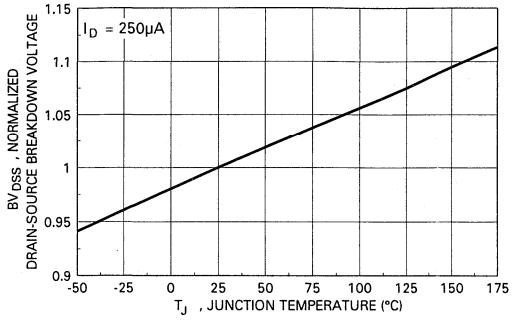


Figure 7. Breakdown Voltage Variation with Temperature

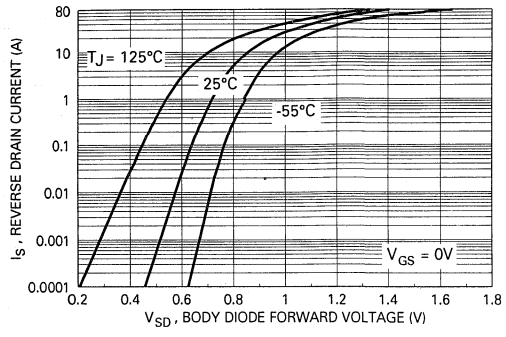


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

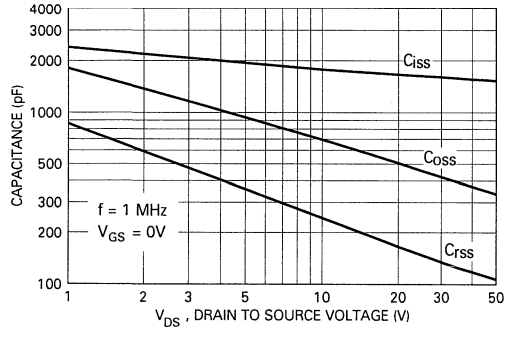


Figure 9. Capacitance Characteristics

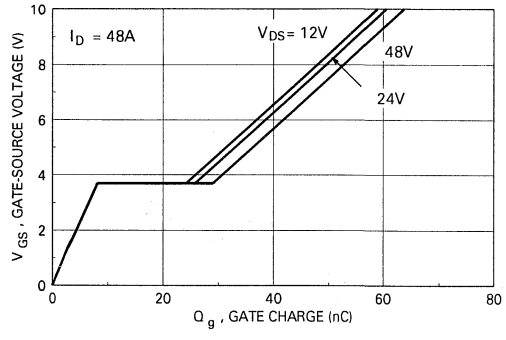


Figure 10. Gate Charge Characteristics

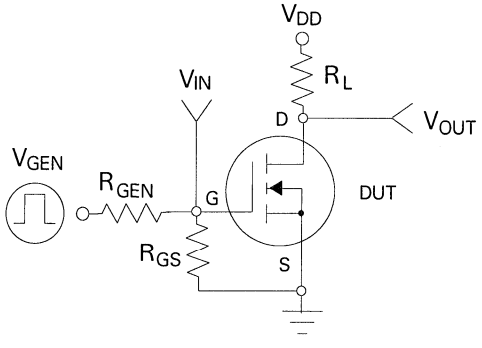


Figure 11. Switching Test Circuit

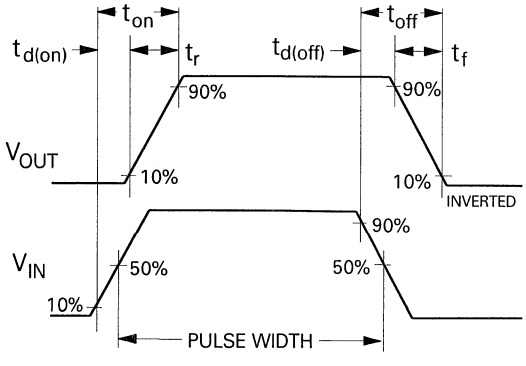


Figure 12. Switching Waveforms

8

Typical Electrical Characteristics (continued)

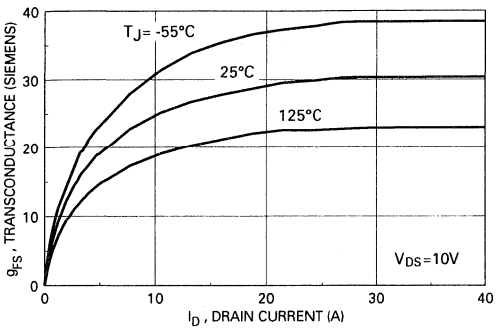


Figure 13. Transconductance Variation with Drain Current and Temperature

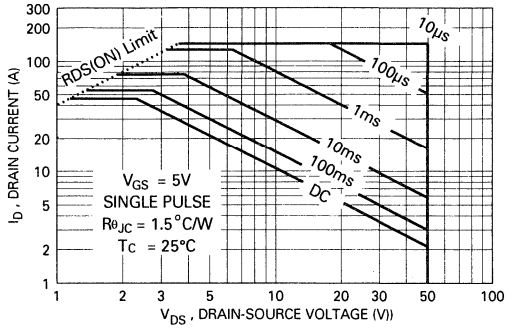


Figure 14. Maximum Safe Operating Area

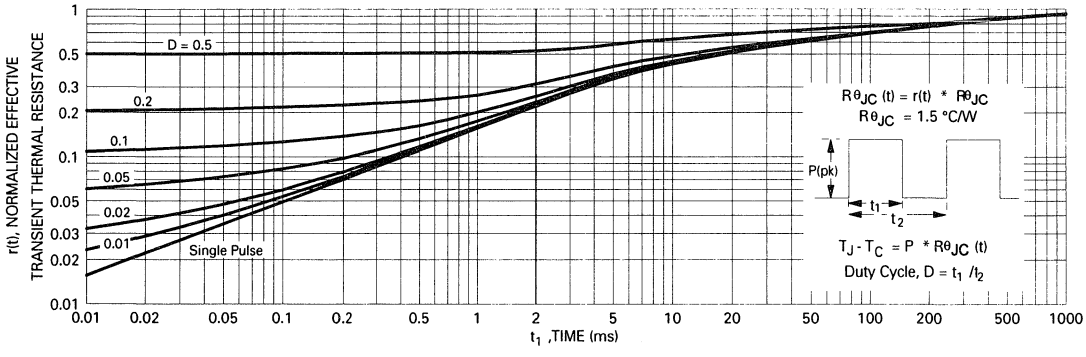


Figure 15. Transient Thermal Response Curve

National Semiconductor™

May 1996

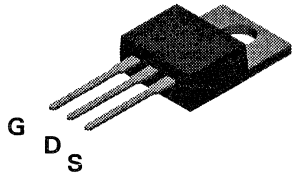
NDP6051 / NDB6051
N-Channel Enhancement Mode Field Effect Transistor

General Description

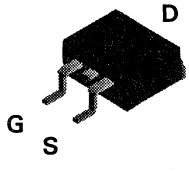
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

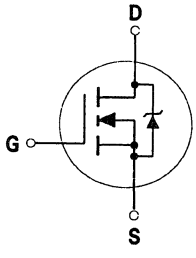
- 48A, 50V. $R_{DS(ON)}$ = 0.022Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP6051	NDB6051	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_P < 50 μs)	± 40		
I_D	Drain Current - Continuous	48		A
	- Pulsed	144		
P_D	Total Power Dissipation @ T_C = 25°C	100		W
	Derate above 25°C	0.67		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 48 A			300	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				48	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.8	4	V
		T_J = 125°C	1.4	2.2	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 24 A		0.018	0.022	Ω
		T_J = 125°C		0.03	0.04	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 24 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1220		pF
C_{oss}	Output Capacitance			520		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 48 A, V_{GS} = 10 V, R_{GEN} = 7.5 Ω		10	20	nS
t_r	Turn - On Rise Time			132	250	nS
$t_{D(off)}$	Turn - Off Delay Time			28	55	nS
t_f	Turn - Off Fall Time			80	150	nS
Q_g	Total Gate Charge	V_{DS} = 24 V, I_D = 48 A, V_{GS} = 10V		37	53	nC
Q_{gs}	Gate-Source Charge			8		
Q_{gd}	Gate-Drain Charge			22		

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				48	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				144	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.8	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 48 A, dI_F/dt = 100 A/µs	35		140	ns
I_{rr}	Reverse Recovery Current		2		8	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

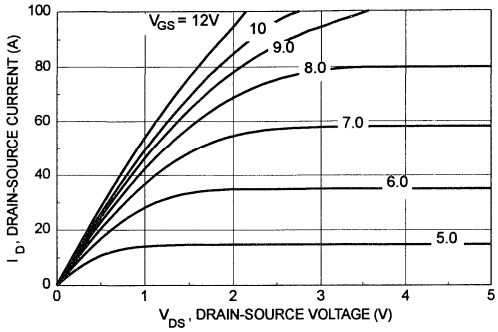


Figure 1. On-Region Characteristics

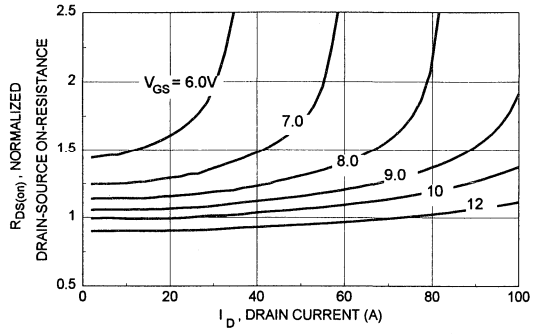


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

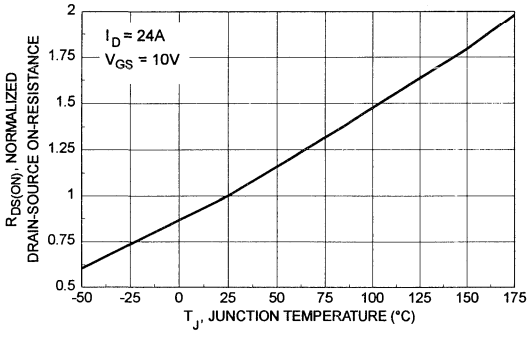


Figure 3. On-Resistance Variation with Temperature

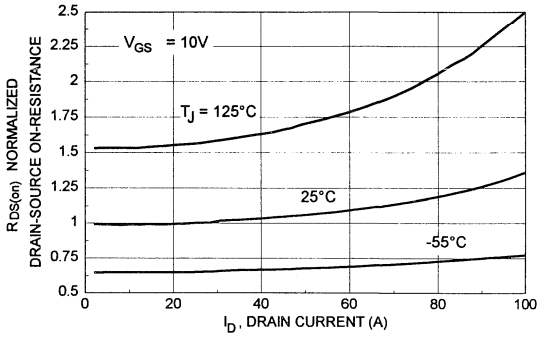


Figure 4. On-Resistance Variation with Drain Current and Temperature

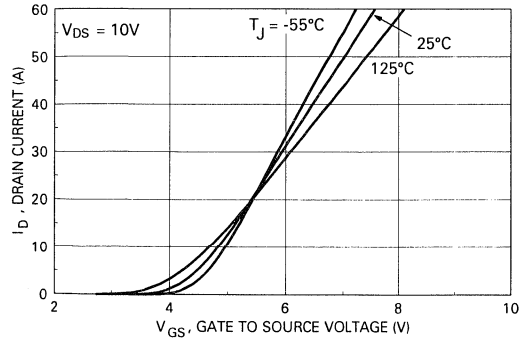


Figure 5. Transfer Characteristics

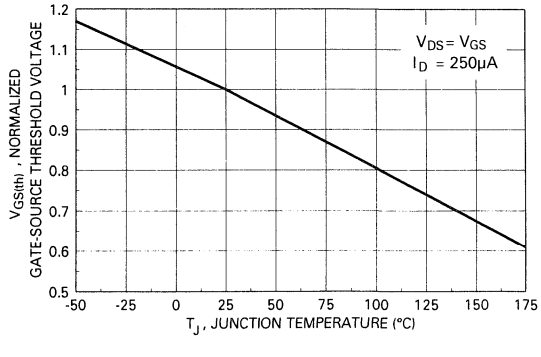


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

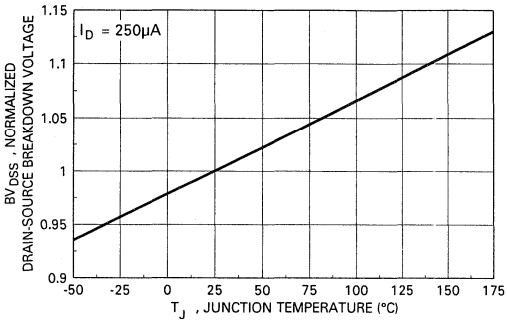


Figure 7. Breakdown Voltage Variation with Temperature

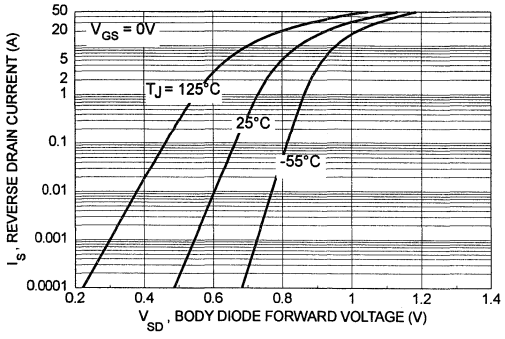


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

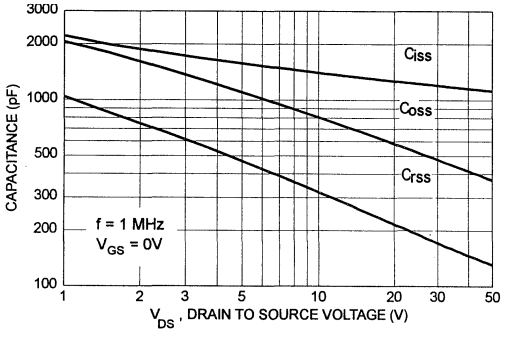


Figure 9. Capacitance Characteristics

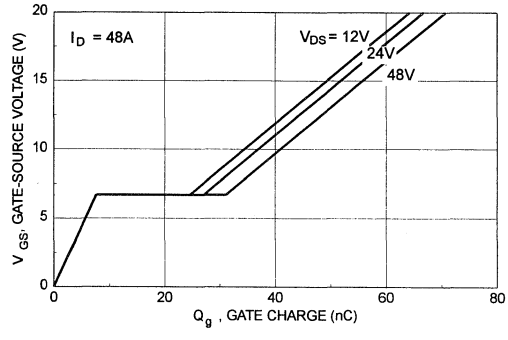


Figure 10. Gate Charge Characteristics

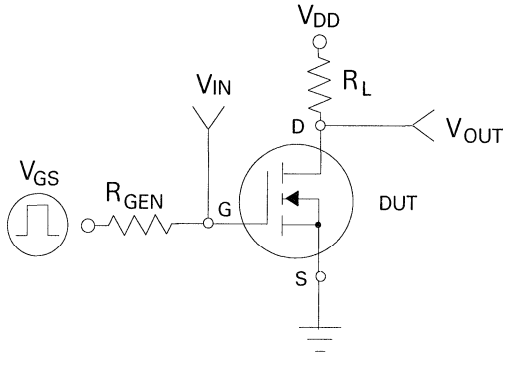


Figure 11. Switching Test Circuit

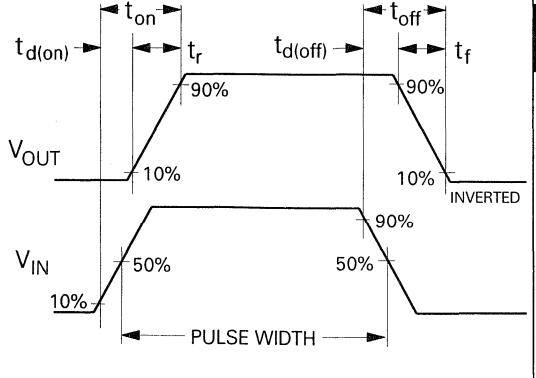


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

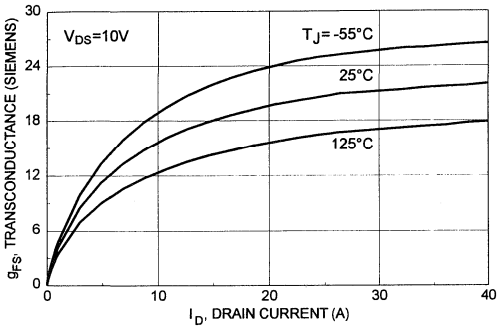


Figure 13. Transconductance Variation with Drain Current and Temperature

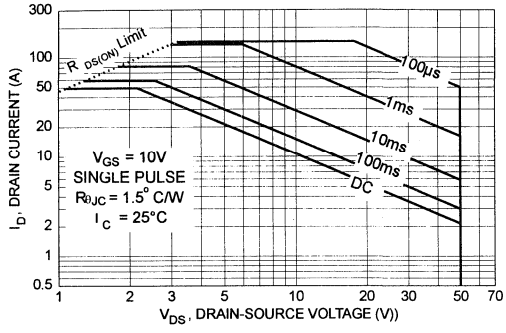


Figure 14. Maximum Safe Operating Area

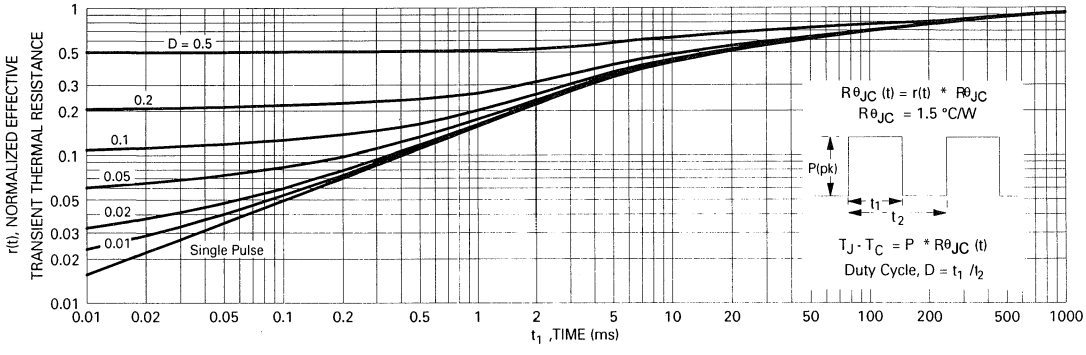


Figure 15. Transient Thermal Response Curve

National Semiconductor™

March 1996

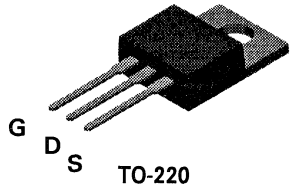
NDP6060 / NDB6060
N-Channel Enhancement Mode Field Effect Transistor

General Description

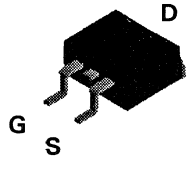
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

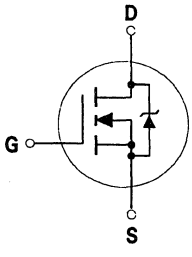
- 48A, 60V. $R_{DS(ON)}$ = 0.025Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6060	NDB6060	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_P < 50 μs)	± 40		
I_D	Drain Current - Continuous	48		A
	- Pulsed	144		
P_D	Total Power Dissipation @ T_C = 25°C	100		W
	Derate above 25°C	0.67		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 48 A			200	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				48	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.9	4	V
		T_J = 125°C	1.4	2.3	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 24 A		0.02	0.025	Ω
		T_J = 125°C		0.032	0.04	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	48			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 24 A	10	19		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1190	1800	pF
C_{oss}	Output Capacitance			475	800	pF
C_{rss}	Reverse Transfer Capacitance			150	400	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 48 A, V_{GS} = 10 V, R_{GEN} = 7.5 Ω		10	20	nS
t_r	Turn - On Rise Time			145	300	nS
$t_{D(off)}$	Turn - Off Delay Time			28	60	nS
t_f	Turn - Off Fall Time			77	150	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 48 A, V_{GS} = 10V		39	70	nC
Q_{gs}	Gate-Source Charge			7.6		
Q_{gd}	Gate-Drain Charge			22		

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				48	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				144	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.8	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 48 A, dI_F/dt = 100 A/µs	35	87	140	ns
I_{rr}	Reverse Recovery Current		2	3.6	8	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

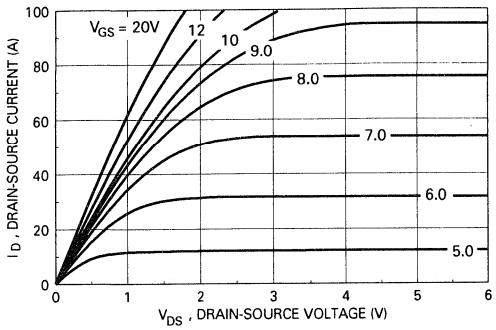


Figure 1. On-Region Characteristics

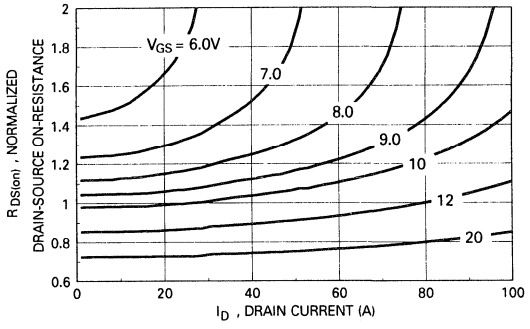


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

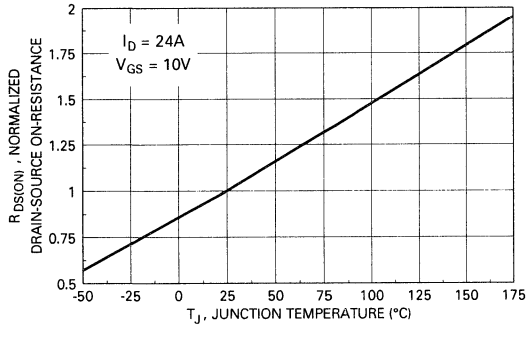


Figure 3. On-Resistance Variation with Temperature

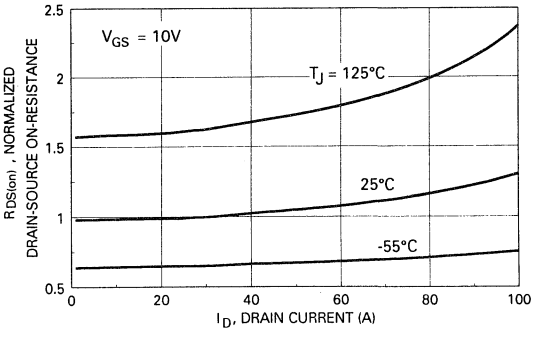


Figure 4. On-Resistance Variation with Drain Current and Temperature

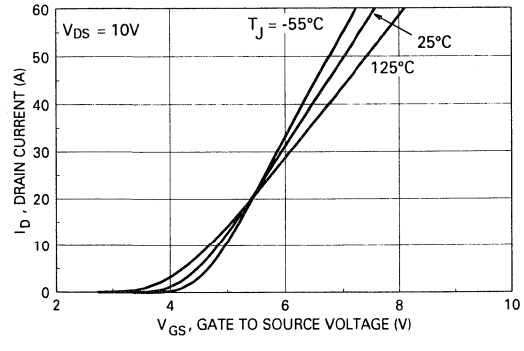


Figure 5. Transfer Characteristics

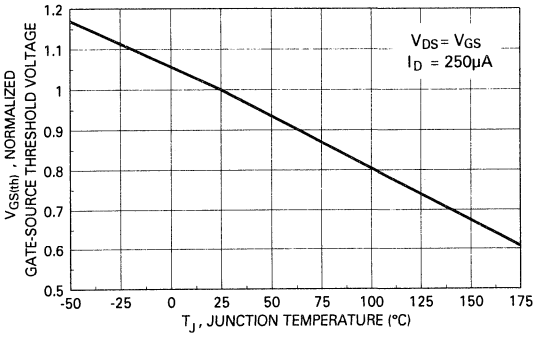


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

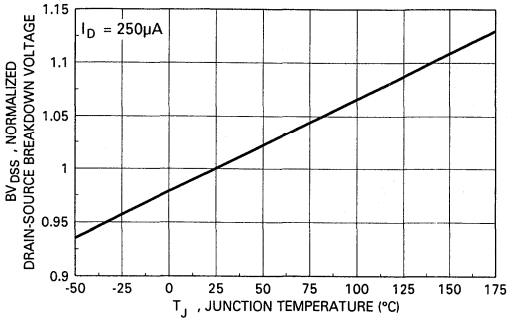


Figure 7. Breakdown Voltage Variation with Temperature

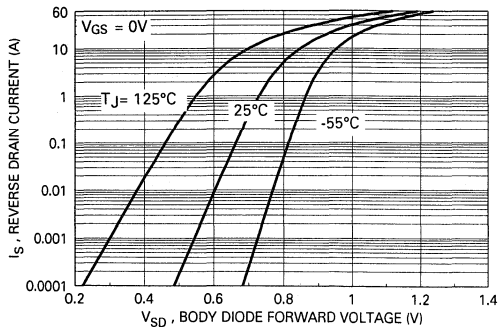


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

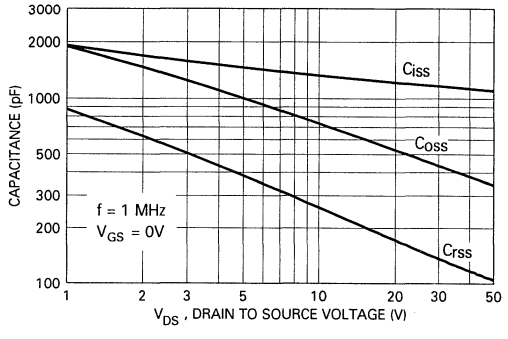


Figure 9. Capacitance Characteristics

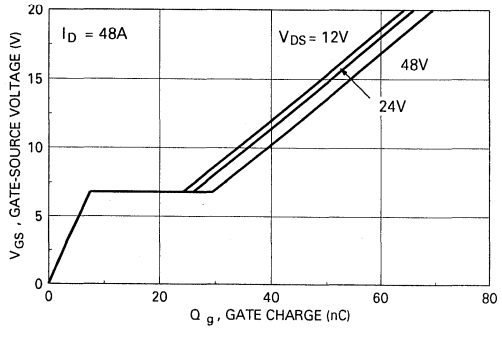


Figure 10. Gate Charge Characteristics

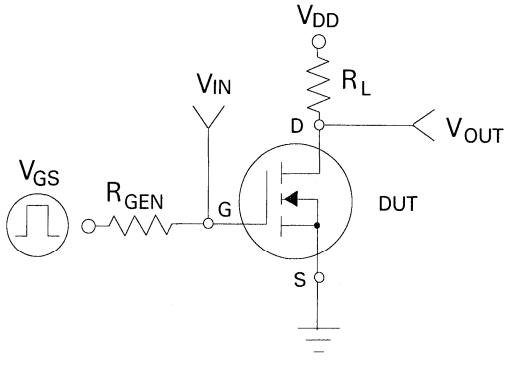


Figure 11. Switching Test Circuit

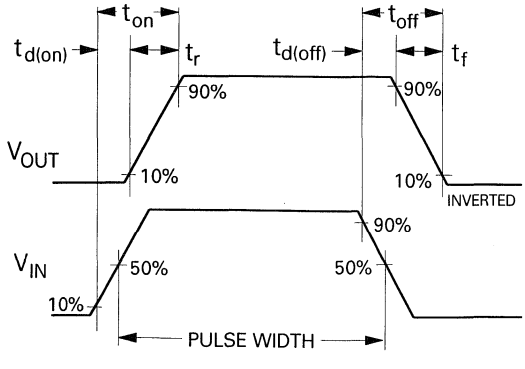


Figure 12. Switching Waveforms

Typical Electrical Characteristics (continued)

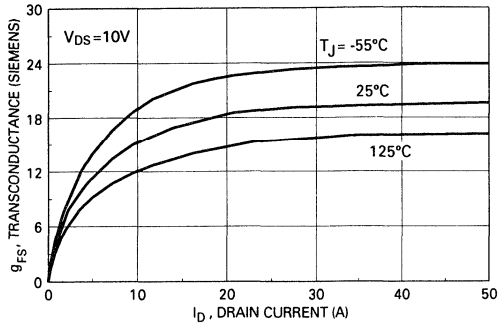


Figure 13. Transconductance Variation with Drain Current and Temperature

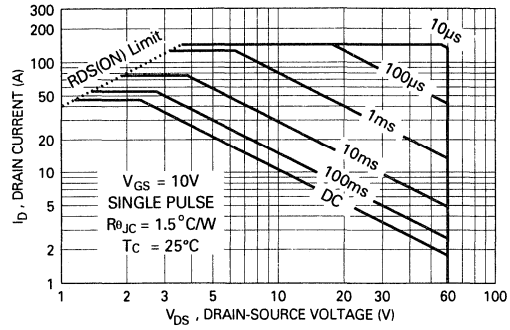


Figure 14. Maximum Safe Operating Area

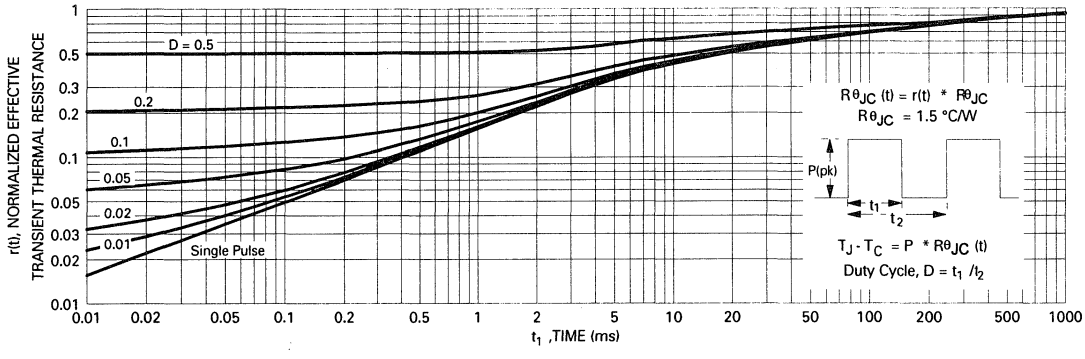


Figure 15. Transient Thermal Response Curve

National Semiconductor™

April 1996

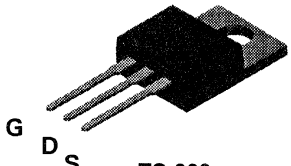
NDP6060L / NDB6060L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

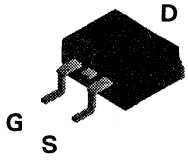
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

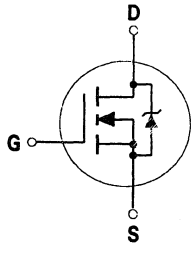
- 48A, 60V. $R_{DS(ON)}$ = 0.025Ω @ V_{GS} = 5V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP6060L	NDB6060L	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive (t_P < 50 µs)	± 25		
I_D	Drain Current - Continuous	48		A
	- Pulsed	144		
P_D	Total Power Dissipation @ T_C = 25°C	100		W
	Derate above 25°C	0.67		W/°C
T_J,T_{STG}	Operating and Storage Temperature	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

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Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 48 A			200	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				48	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2	V
		T_J = 125°C	0.65		1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 24 A			0.025	Ω
		T_J = 125°C			0.04	
		V_{GS} = 10 V, I_D = 24 A			0.02	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	48			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 24 A	10			S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1630	2000	pF
C_{oss}	Output Capacitance			460	800	pF
C_{rss}	Reverse Transfer Capacitance			150	400	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 48 A, V_{GS} = 5 V, R_{GEN} = 15 Ω, R_{GS} = 15 Ω		15	30	nS
t_r	Turn - On Rise Time			320	500	nS
$t_{D(off)}$	Turn - Off Delay Time			49	100	nS
t_f	Turn - Off Fall Time			161	300	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 48 A, V_{GS} = 5 V		36	60	nC
Q_{gs}	Gate-Source Charge			8.2		nC
Q_{gd}	Gate-Drain Charge			21		nC

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				48	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				144	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 24 A (Note 1)			1.3	V
		T_J = 125°C			1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 48 A, dI_F/dt = 100 A/µs	35	75	140	ns
I_{rr}	Reverse Recovery Current		2	3.6	8	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

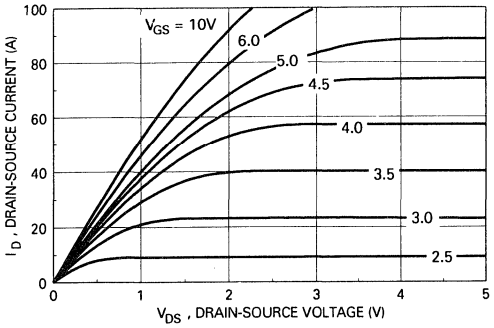

Figure 1. On-Region Characteristics

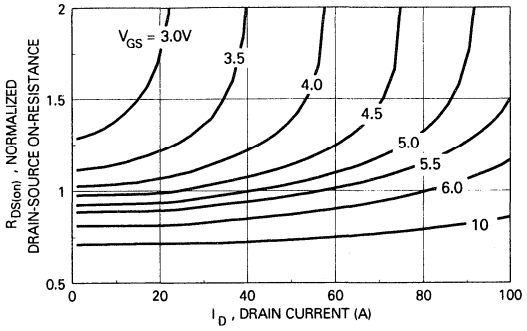

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

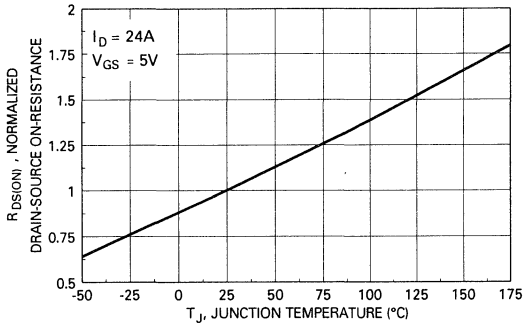

Figure 3. On-Resistance Variation with Temperature

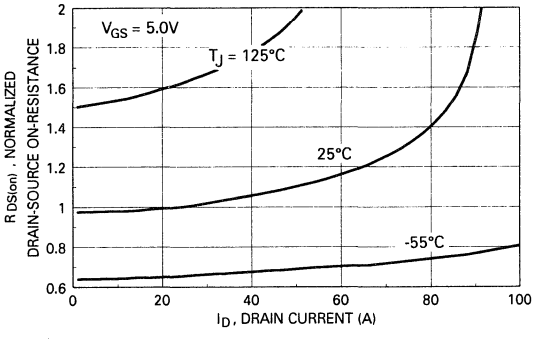

Figure 4. On-Resistance Variation with Drain Current and Temperature

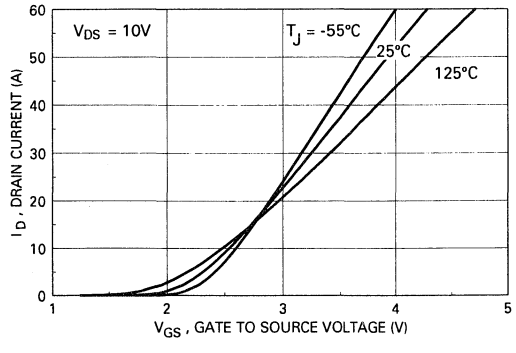

Figure 5. Transfer Characteristics

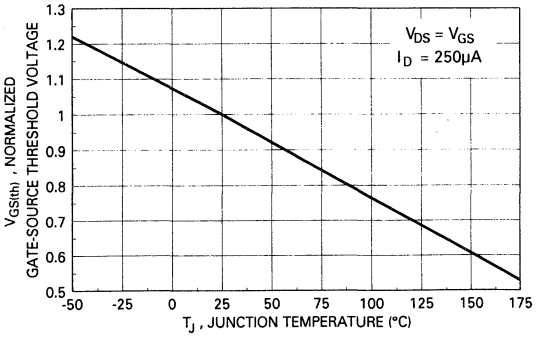

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

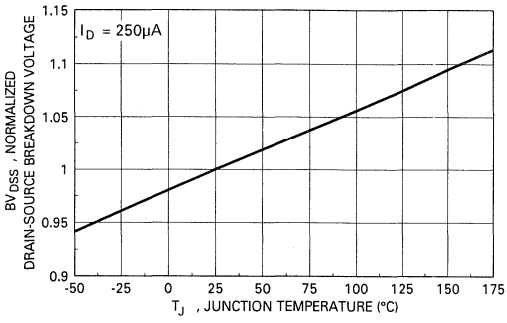

Figure 7. Breakdown Voltage Variation with Temperature

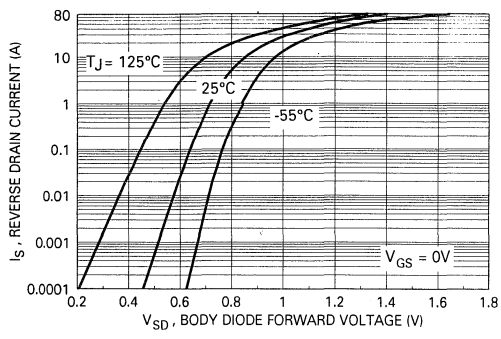

Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

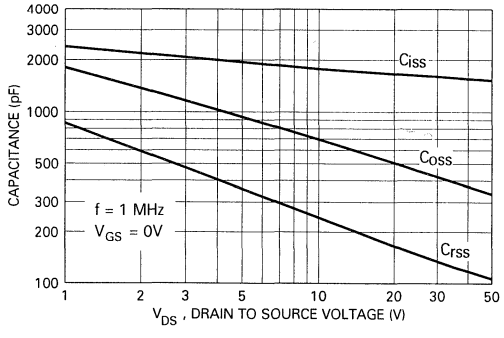

Figure 9. Capacitance Characteristics

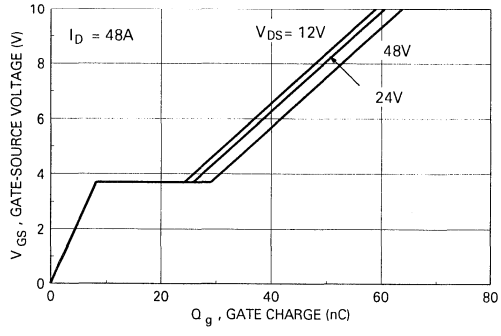

Figure 10. Gate Charge Characteristics

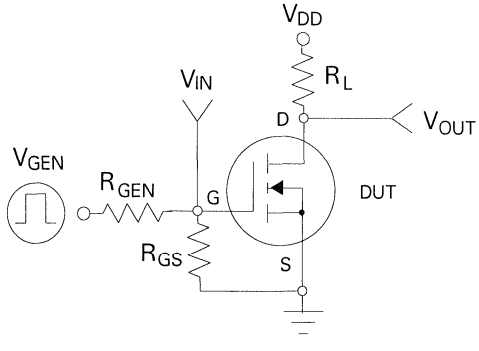

Figure 11. Switching Test Circuit

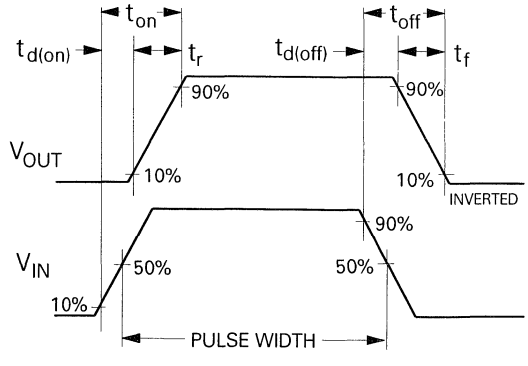

Figure 12. Switching Waveforms

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Typical Electrical Characteristics (continued)

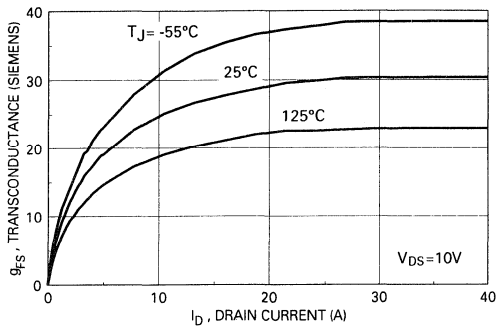


Figure 13. Transconductance Variation with Drain Current and Temperature

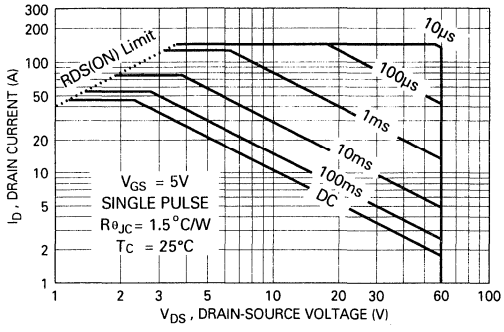


Figure 14. Maximum Safe Operating Area

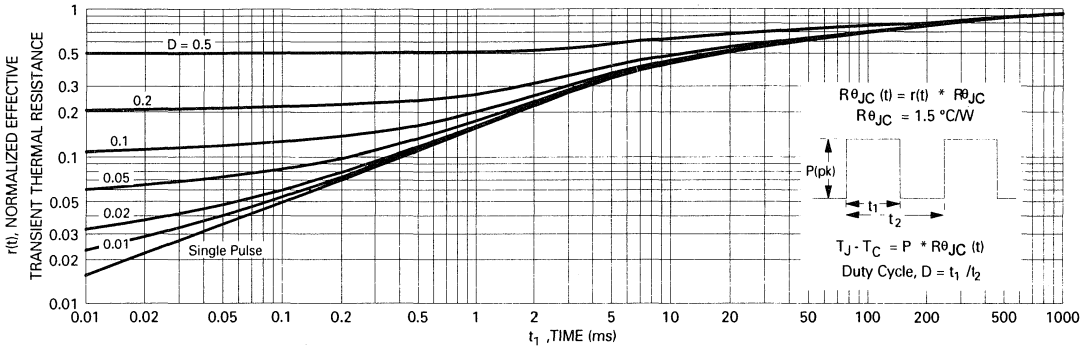


Figure 15. Transient Thermal Response Curve

National Semiconductor™

May 1996

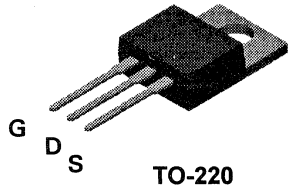
NDP7051 / NDB7051
N-Channel Enhancement Mode Field Effect Transistor

General Description

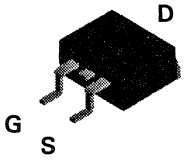
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

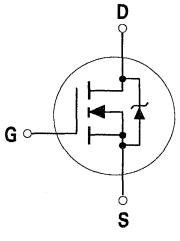
- 64A, 50V. $R_{DS(ON)}$ = 0.016Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7051	NDB7051	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_P < 50 µs)	± 40		
I_D	Drain Current - Continuous	64		A
	- Pulsed	190		
P_D	Maximum Power Dissipation @ T_C = 25°C	130		W
	Derate above 25°C	0.87		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 64 A			500	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				64	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.9	4	V
		T_J = 125°C	1.4	2.2	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 35 A		0.013	0.016	Ω
		T_J = 125°C		0.021	0.025	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 35 A		30		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1930		pF
C_{oss}	Output Capacitance			870		pF
C_{rss}	Reverse Transfer Capacitance			310		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 64 A, V_{GS} = 10 V, R_{GEN} = 5 Ω		13	30	nS
t_r	Turn - On Rise Time			98	200	nS
$t_{D(off)}$	Turn - Off Delay Time			36	80	nS
t_f	Turn - Off Fall Time			65	150	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 64 A, V_{GS} = 10 V		67	100	nC
Q_{gs}	Gate-Source Charge			11		nC
Q_{gd}	Gate-Drain Charge			37.5		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				64	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				190	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 35 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.8	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 64 A, dI_F/dt = 100 A/µs	40	105	150	ns
I_{rr}	Reverse Recovery Current		2	4.5	10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.15	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

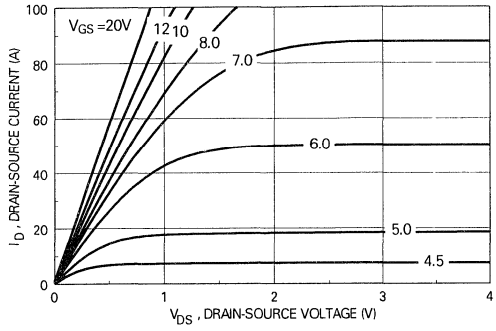


Figure 1. On-Region Characteristics

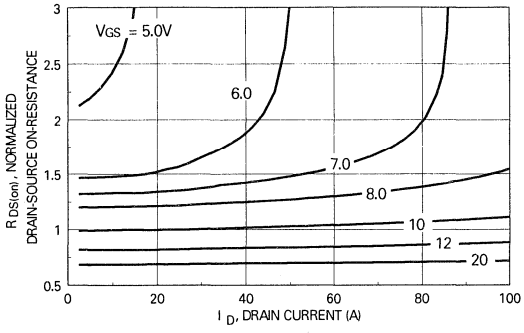


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

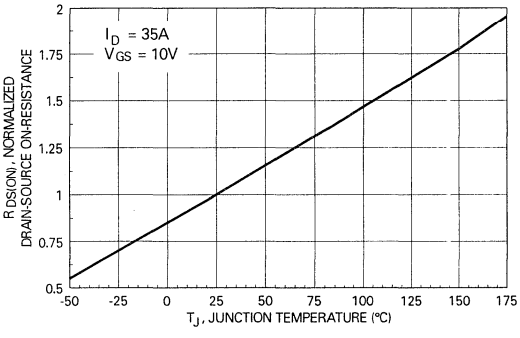


Figure 3. On-Resistance Variation with Temperature

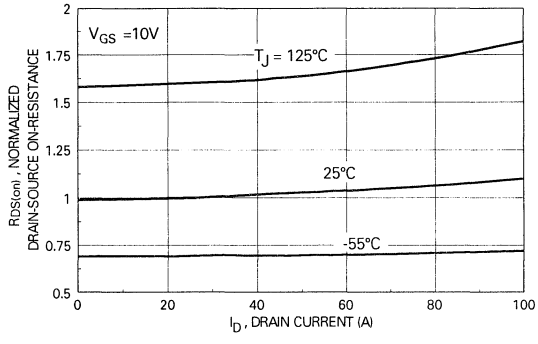


Figure 4. On-Resistance Variation with Drain Current and Temperature

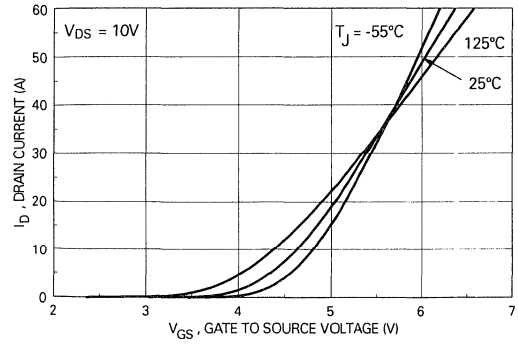


Figure 5. Transfer Characteristics

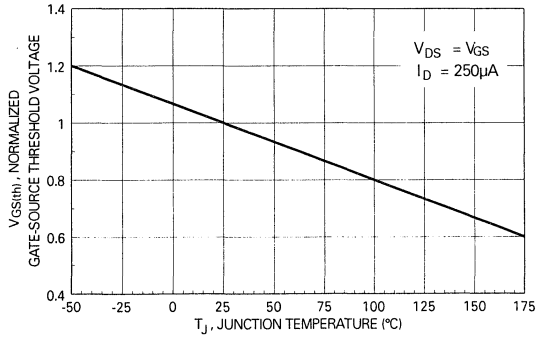


Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

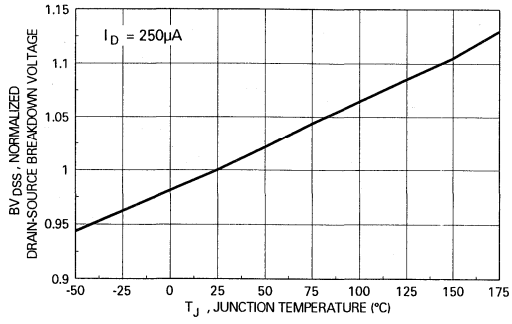


Figure 7. Breakdown Voltage Variation with Temperature

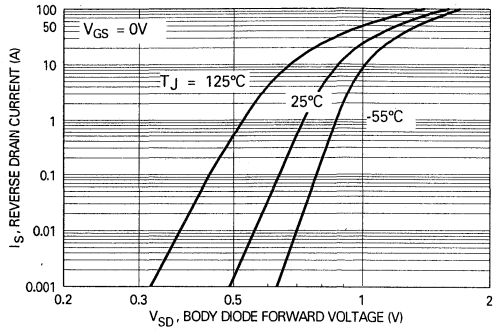


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

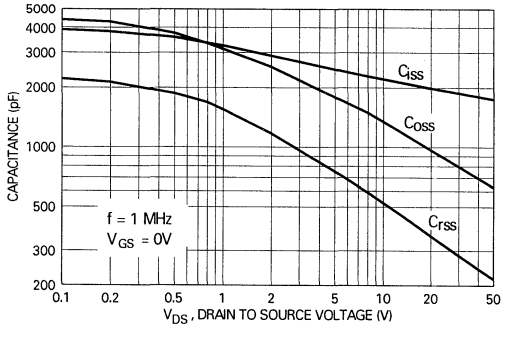


Figure 9. Capacitance Characteristics

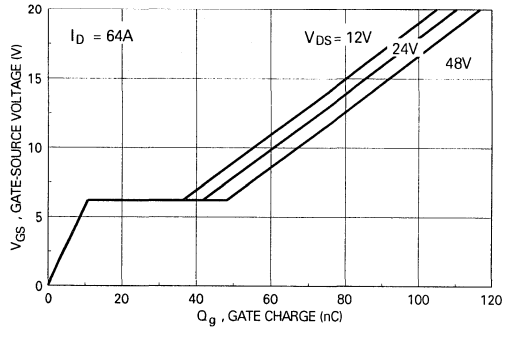


Figure 10. Gate Charge Characteristics

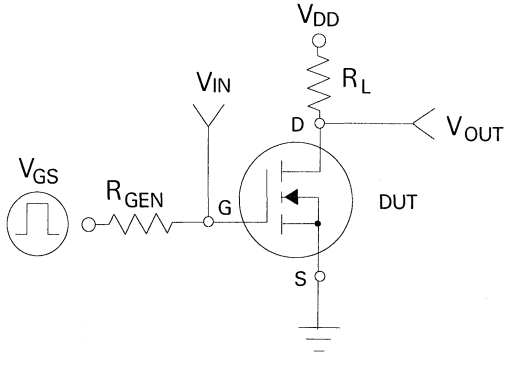


Figure 11. Switching Test Circuit

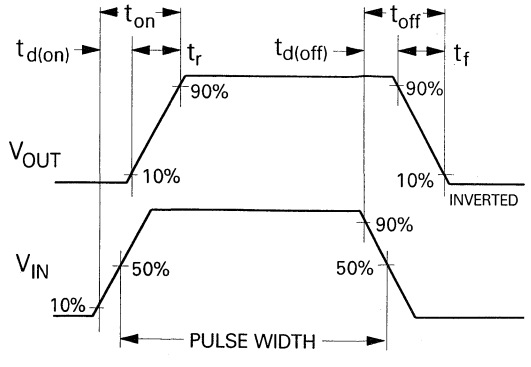


Figure 12. Switching Waveforms

8

Typical Electrical Characteristics (continued)

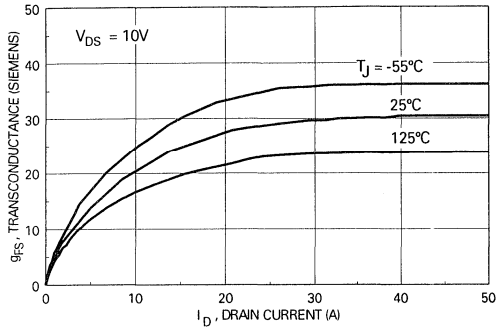


Figure 13. Transconductance Variation with Drain Current and Temperature

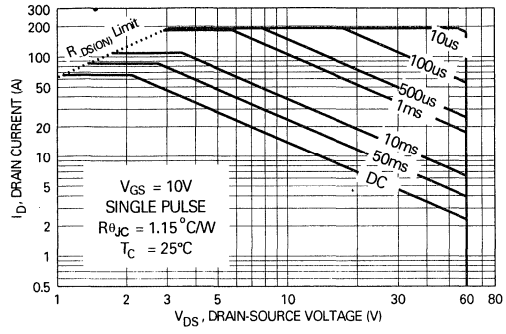


Figure 14. Maximum Safe Operating Area

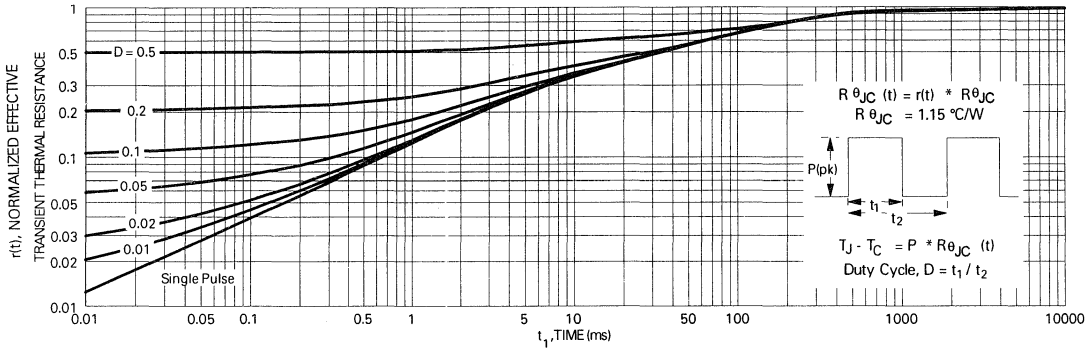


Figure 15. Transient Thermal Response Curve

National Semiconductor™

May 1996
ADVANCE INFORMATION

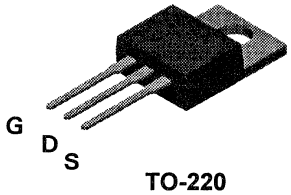
NDP7051L / NDB7051L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

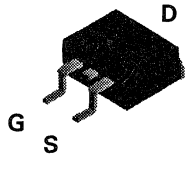
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

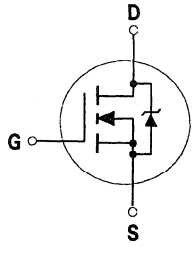
- 68A, 50V. $R_{DS(ON)}$ = 0.014 @ V_{GS}=5V
  $R_{DS(ON)}$ = 0.01Ω @ V_{GS}=10V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7051L	NDB7051L	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive (t_P < 50 µs)	± 25		
I_D	Drain Current - Continuous	68		A
	- Pulsed	200		
P_D	Maximum Power Dissipation @ T_C = 25°C	130		W
	Derate above 25°C	0.87		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 68 A			430	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				68	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2	V
		T_J = 125°C	0.65		1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 34 A			0.014	Ω
		T_J = 125°C			0.025	
		V_{GS} = 10 V, I_D = 34 A			0.01	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	60			A
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				68	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				200	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 34 A (Note 1)			1.3	V
		T_J = 125°C			1.2	
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.15	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

April 1996
ADVANCE INFORMATION

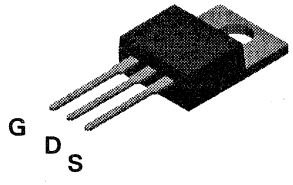
NDP7052 / NDB7052
N-Channel Enhancement Mode Field Effect Transistor

General Description

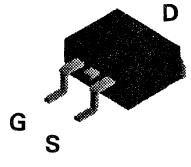
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

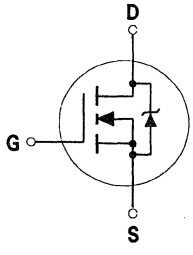
- 75A, 50V. $R_{DS(ON)}$ = 0.01Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7052	NDB7052	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive ($t_P < 50$ µs)	± 40		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Maximum Power Dissipation @ T_C = 25°C	150		W
	Derate above 25°C	1		W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

8

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 75 A			550	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				75	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
		T_J = 125°C	1.4		3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 37.5 A		0.008	0.01	Ω
		T_J = 150°C		0.014	0.018	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				75	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				225	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 37.5 A (Note 1)			1.3	V
		T_J = 125°C			1.2	
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

April 1996
ADVANCE INFORMATION

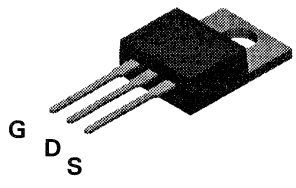
NDP7052L / NDB7052L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

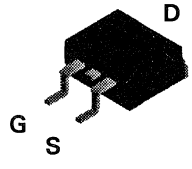
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

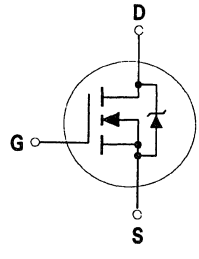
- 75A, 50V. $R_{DS(ON)}$ = 0.010Ω @ V_{GS}=5V
  $R_{DS(ON)}$ = 0.0075Ω @ V_{GS}=10V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7052L	NDB7052L	Units
V_{DSS}	Drain-Source Voltage	50		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	50		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive (t_P < 50 µs)	± 25		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Maximum Power Dissipation @ T_C = 25°C	150		W
	Derate above 25°C	1		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C

8

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 70 A			550	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				75	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	50			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 40 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2	V
		T_J = 125°C	0.65		1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 37.5 A			0.01	Ω
		T_J = 150°C			0.018	
		V_{GS} = 10 V, I_D = 37.5 A			0.0075	
		T_J = 150°C			0.014	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 10 V	60			A
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				75	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				225	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 35 A (Note 1)			1.3	V
		T_J = 125°C			1.2	
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

National Semiconductor™

June 1996

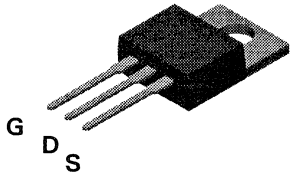
NDP7060 / NDB7060
N-Channel Enhancement Mode Field Effect Transistor

General Description

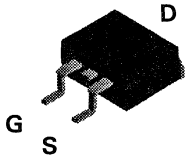
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

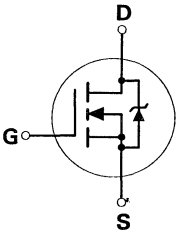
- 75A, 60V. $R_{DS(ON)}$ = 0.013Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7060	NDB7060	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive ($t_P < 50$ µs)	± 40		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Maximum Power Dissipation @ T_C = 25°C	150		W
	Derate above 25°C	1		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 75 A			550	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				75	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.8	4	V
		T_J = 125°C	1.4	2.1	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 40 A		0.01	0.013	Ω
		T_J = 125°C		0.015	0.024	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 37.5 A	15	39		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		2960	3600	pF
C_{oss}	Output Capacitance			1130	1600	pF
C_{rss}	Reverse Transfer Capacitance			380	800	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 75 A, V_{GS} = 10 V, R_{GEN} = 5 Ω		17	30	nS
t_r	Turn - On Rise Time			128	400	nS
$t_{D(off)}$	Turn - Off Delay Time			54	80	nS
t_f	Turn - Off Fall Time			90	200	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 75 A, V_{GS} = 10 V		100	115	nC
Q_{gs}	Gate-Source Charge			14.5		nC
Q_{gd}	Gate-Drain Charge			51		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				75	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				225	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 37.5 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.84	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 75 A, dI_F/dt = 100 A/µs	40	76	150	ns
I_{rr}	Reverse Recovery Current		2	4.7	10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

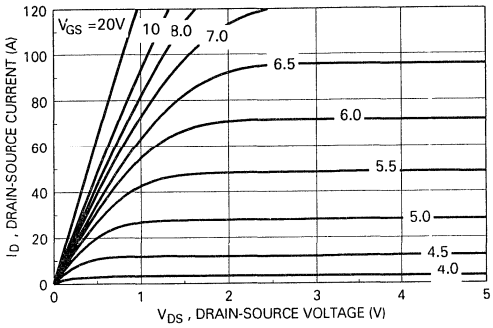

Figure 1. On-Region Characteristics

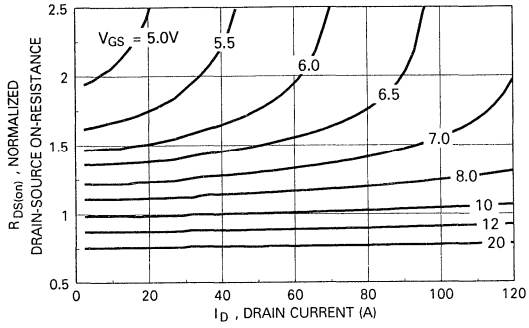

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

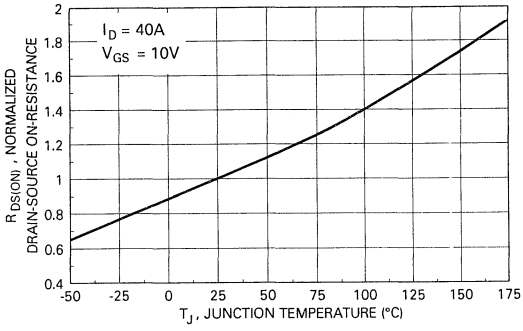

Figure 3. On-Resistance Variation with Temperature

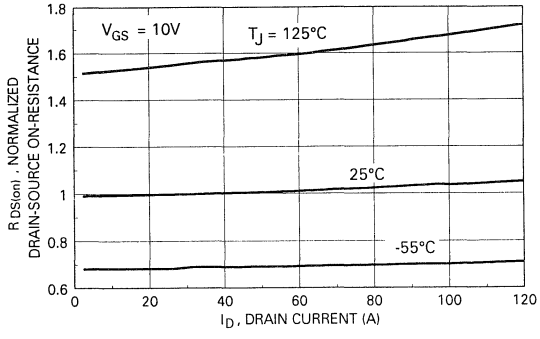

Figure 4. On-Resistance Variation with Drain Current and Temperature

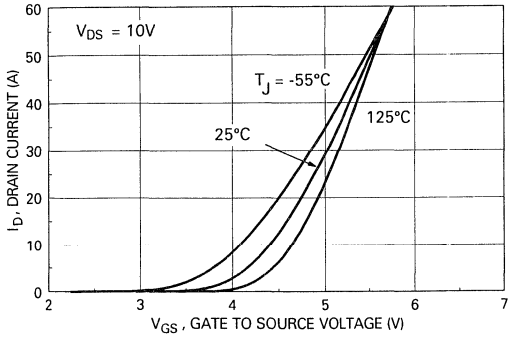

Figure 5. Transfer Characteristics

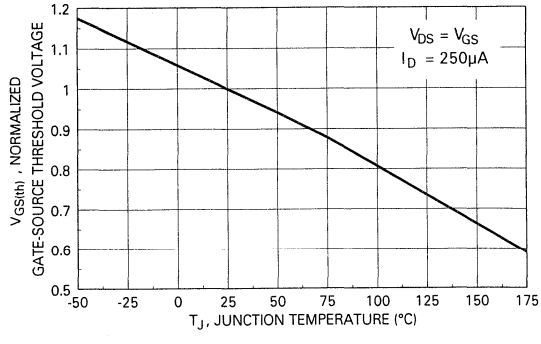

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

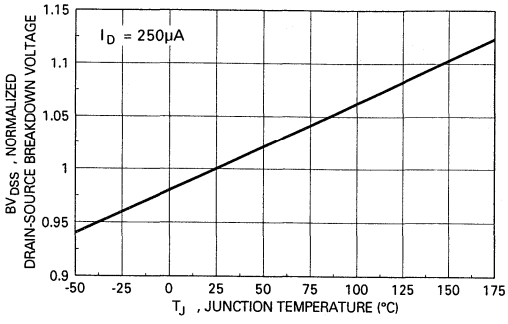

Figure 7. Breakdown Voltage Variation with Temperature

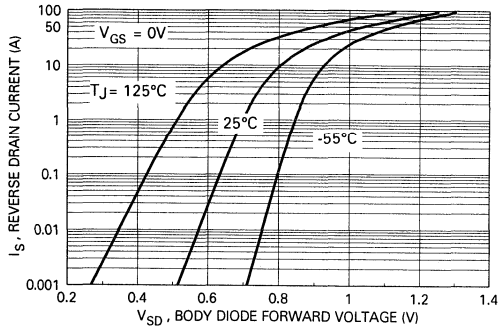

Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

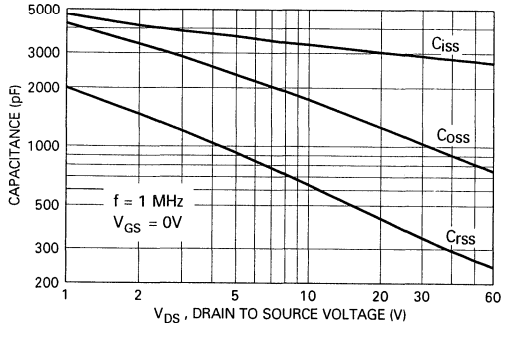

Figure 9. Capacitance Characteristics

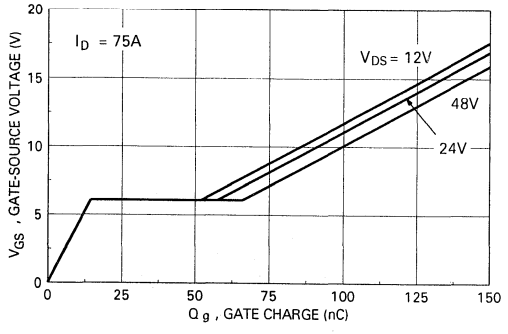

Figure 10. Gate Charge Characteristics

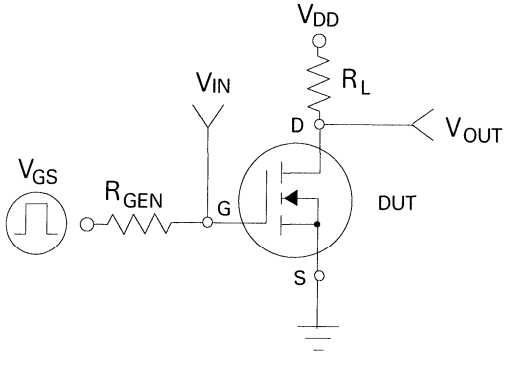

Figure 11. Switching Test Circuit

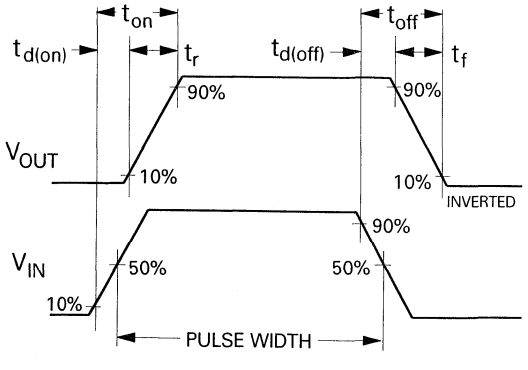

Figure 12. Switching Waveforms

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Typical Electrical Characteristics (continued)

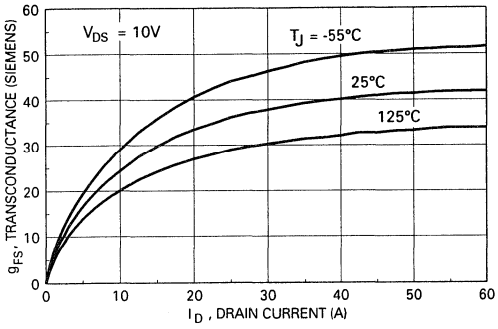


Figure 13. Transconductance Variation with Drain Current and Temperature

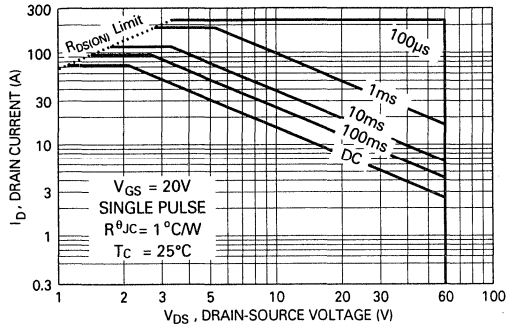


Figure 14. Maximum Safe Operating Area

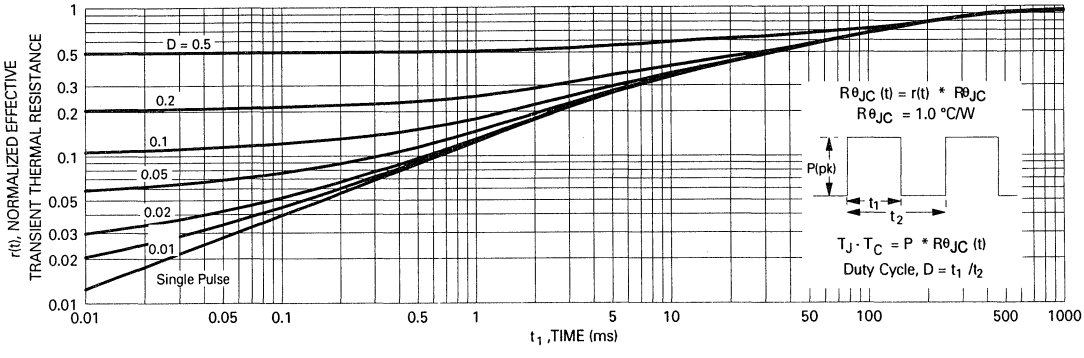


Figure 15. Transient Thermal Response Curve

National Semiconductor™

June 1996

NDP7060L / NDB7060L

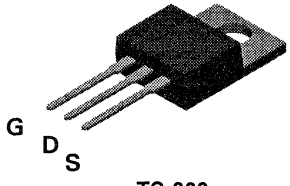
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

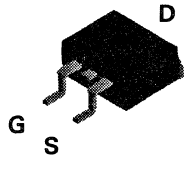
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

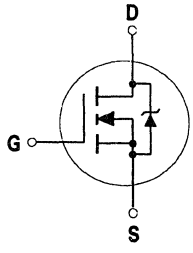
- 75A, 60V. $R_{DS(ON)}$ = 0.013Ω @ V_{GS} = 5V
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_c = 25°C unless otherwise noted

Symbol	Parameter	NDP7060L	NDB7060L	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_p < 50 μs)	± 40		
I_D	Drain Current - Continuous	75		A
	- Pulsed	225		
P_D	Total Power Dissipation @ T_C = 25°C	150		W
	Derate above 25°C	1		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 25 V, I_D = 75 A			550	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				75	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60 V, V_{GS} = 0 V			250	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.3	2	V
		T_J = 125°C	0.65	0.8	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 37.5 A		0.01	0.013	Ω
		T_J = 125°C		0.016	0.024	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 37.5 A	15	67		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		4200	4000	pF
C_{oss}	Output Capacitance			1100	1600	pF
C_{rss}	Reverse Transfer Capacitance			310	800	pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 75 A, V_{GS} = 5 V, R_{GEN} = 10Ω R_{GS} = 10 Ω		23	40	nS
t_r	Turn - On Rise Time			460	600	nS
$t_{D(off)}$	Turn - Off Delay Time			100	150	nS
t_f	Turn - Off Fall Time			270	400	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 75 A, V_{GS} = 5 V		86	115	nC
Q_{gs}	Gate-Source Charge			13		nC
Q_{gd}	Gate-Drain Charge			62		nC

Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				75	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				225	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 37.5 A (Note 1)		0.92	1.3	V
		T_J = 125°C		0.85	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 60A, dI_F/dt = 100 A/µs		108	150	ns
I_{rr}	Reverse Recovery Current			4.6	10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

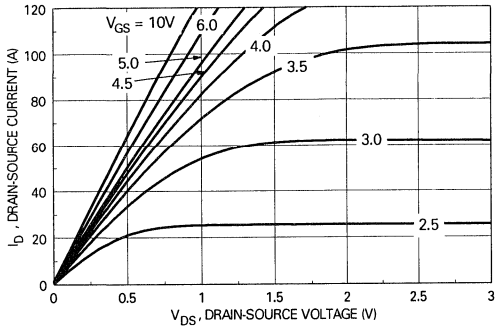

Figure 1. On-Region Characteristics

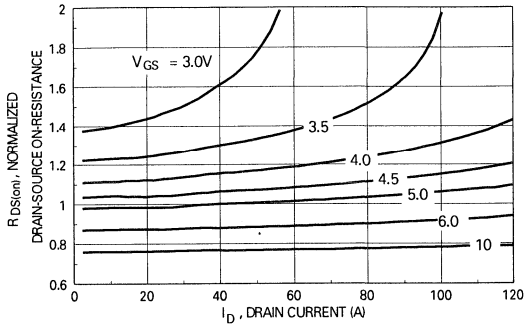

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

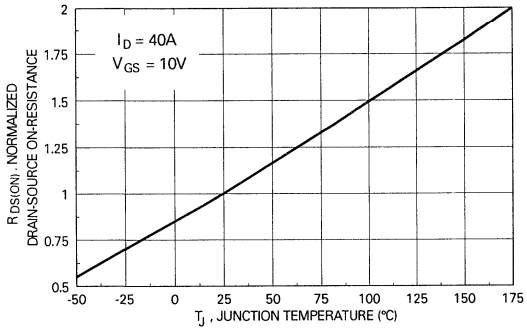

Figure 3. On-Resistance Variation with Temperature

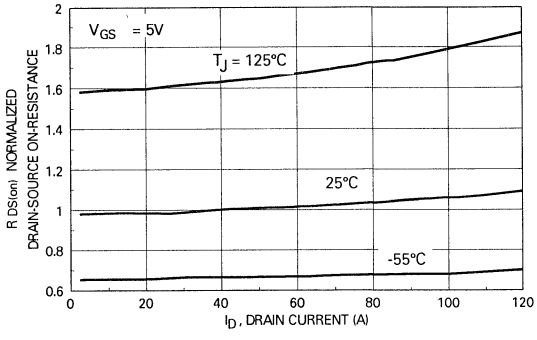

Figure 4. On-Resistance Variation with Drain Current and Temperature

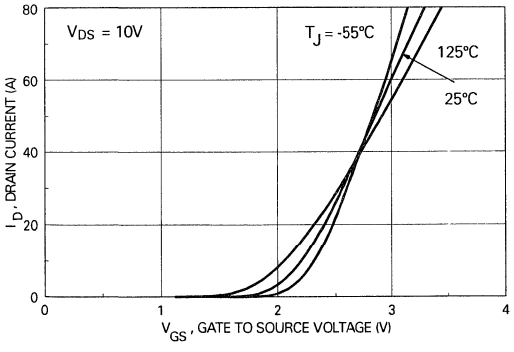

Figure 5. Transfer Characteristics

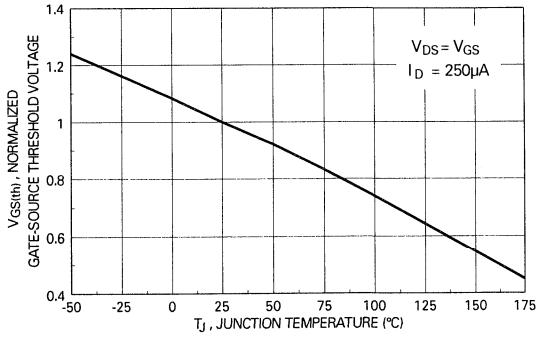

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

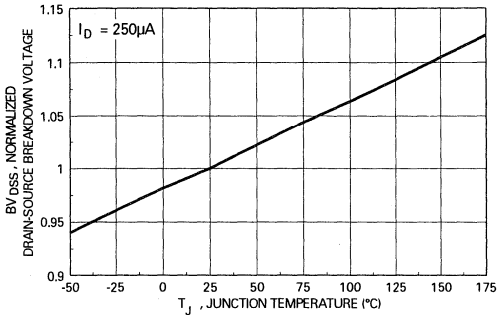

Figure 7. Breakdown Voltage Variation with Temperature

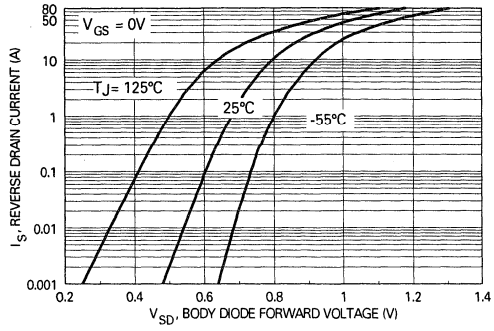

Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

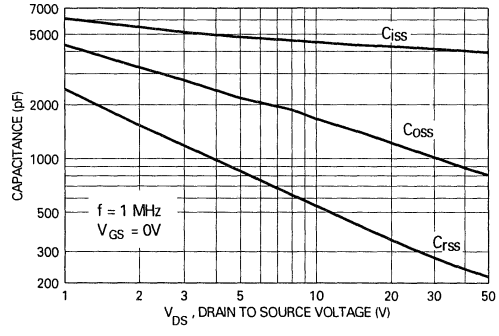

Figure 9. Capacitance Characteristics

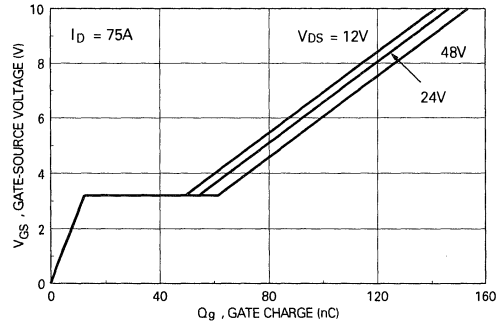

Figure 10. Gate Charge Characteristics

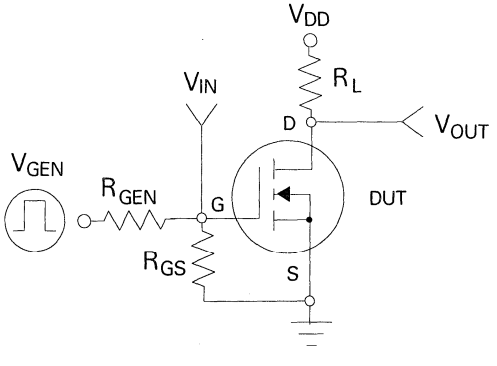

Figure 11. Switching Test Circuit

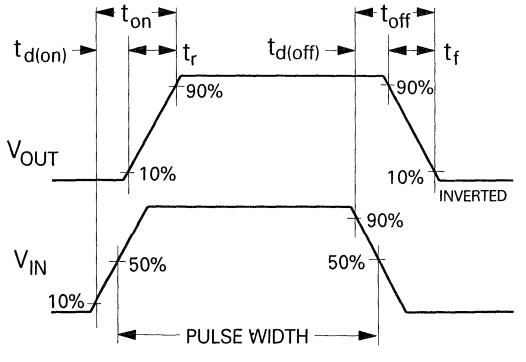

Figure 12. Switching Waveforms

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Typical Electrical Characteristics (continued)

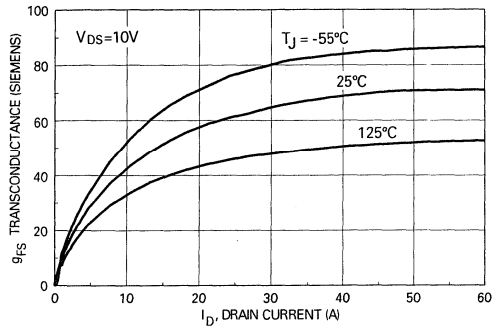


Figure 13. Transconductance Variation with Drain Current and Temperature

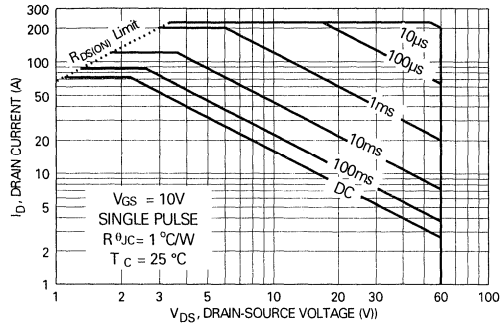


Figure 14. Maximum Safe Operating Area

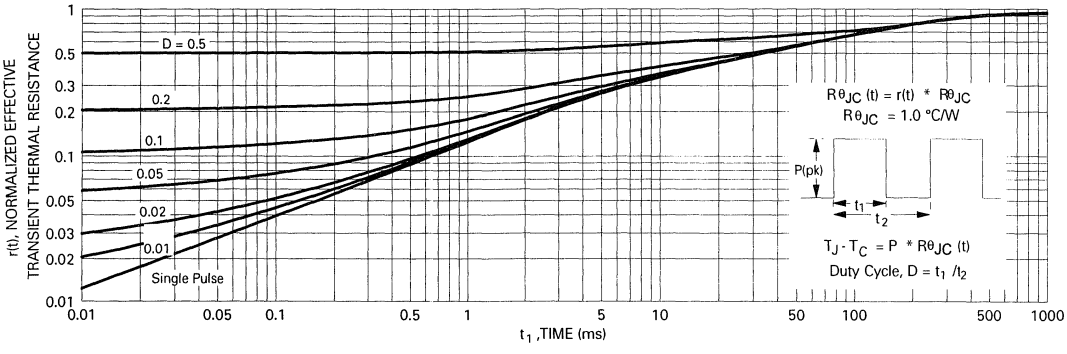


Figure 15. Transient Thermal Response Curve

National Semiconductor™

May 1996

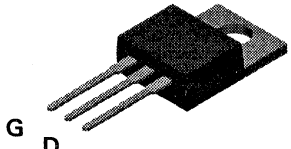
NDP7061 / NDB7061
N-Channel Enhancement Mode Field Effect Transistor

General Description

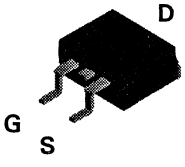
These N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

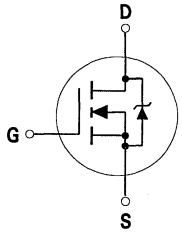
- 64A, 60V. $R_{DS(ON)}$ = 0.016Ω @ V_{GS}=10V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7061	NDB7061	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1$ MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 20		V
	- Nonrepetitive (t_p < 50 μs)	± 40		
I_D	Drain Current - Continuous	64		A
	- Pulsed	190		
P_D	Maximum Power Dissipation @ T_C = 25°C	130		W
	Derate above 25°C	0.87		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275		°C

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Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 30 V, I_D = 64 A			500	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				64	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -20 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	2.9	4	V
		T_J = 125°C	1.4	2.2	3.6	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 35 A		0.013	0.016	Ω
		T_J = 125°C		0.021	0.025	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 10 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 35 A		30		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz		1930		pF
C_{oss}	Output Capacitance			870		pF
C_{rss}	Reverse Transfer Capacitance			310		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 25 V, I_D = 64 A, V_{GS} = 10 V, R_{GEN} = 5 Ω		13	30	nS
t_r	Turn - On Rise Time			98	200	nS
$t_{D(off)}$	Turn - Off Delay Time			36	80	nS
t_f	Turn - Off Fall Time			65	150	nS
Q_g	Total Gate Charge	V_{DS} = 48 V, I_D = 64 A, V_{GS} = 10 V		67	100	nC
Q_{gs}	Gate-Source Charge			11		nC
Q_{gd}	Gate-Drain Charge			37.5		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				64	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				190	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 35 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.8	1.2	
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 64 A, dI_F/dt = 100 A/µs	40	105	150	ns
I_{rr}	Reverse Recovery Current		2	4.5	10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.15	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

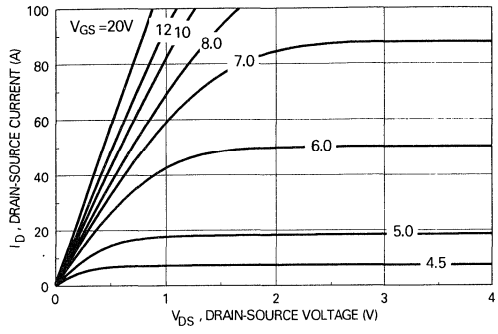

Figure 1. On-Region Characteristics

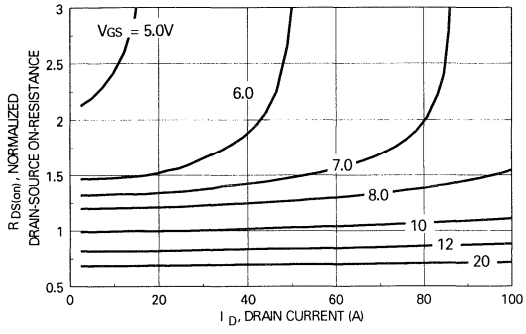

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

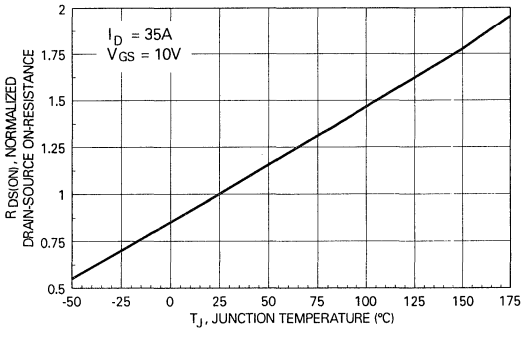

Figure 3. On-Resistance Variation with Temperature

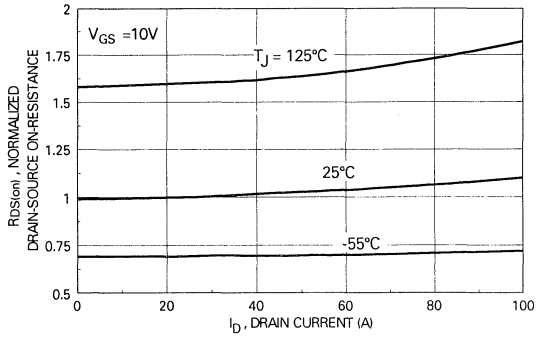

Figure 4. On-Resistance Variation with Drain Current and Temperature

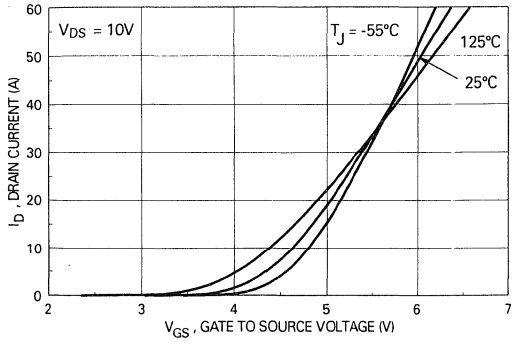

Figure 5. Transfer Characteristics

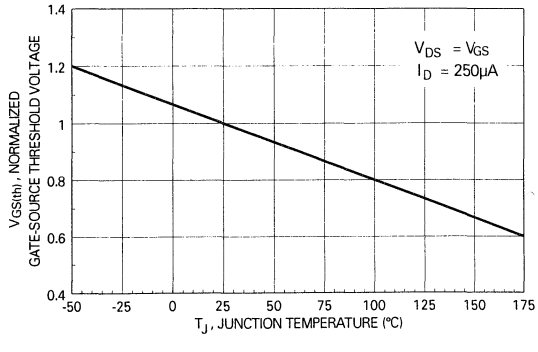

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

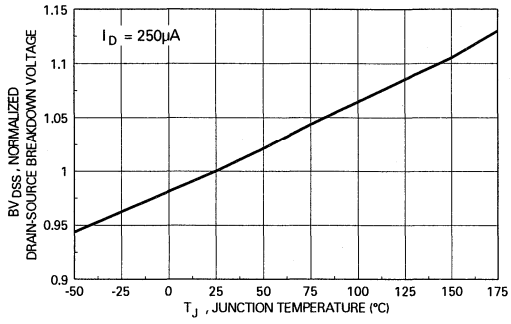

Figure 7. Breakdown Voltage Variation with Temperature

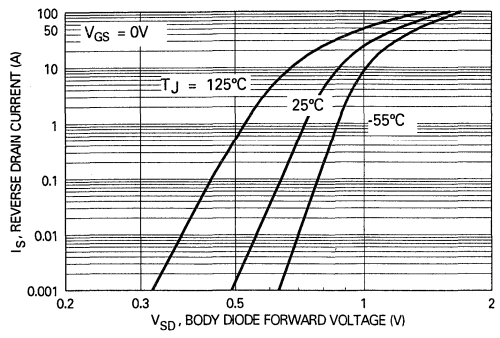

Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

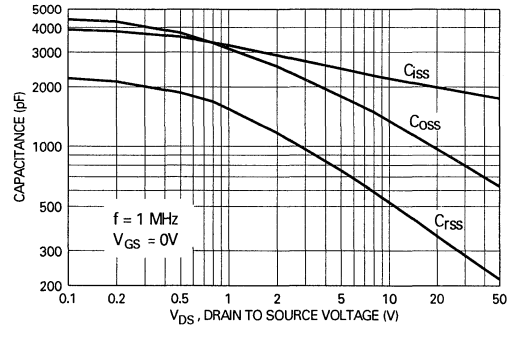

Figure 9. Capacitance Characteristics

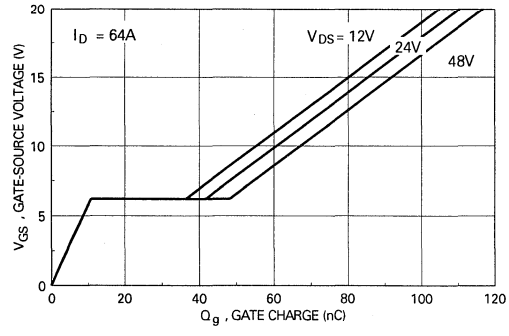

Figure 10. Gate Charge Characteristics

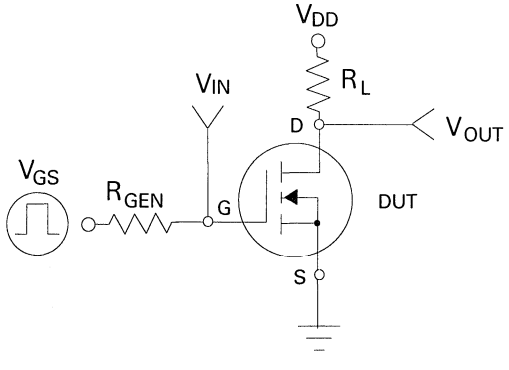

Figure 11. Switching Test Circuit

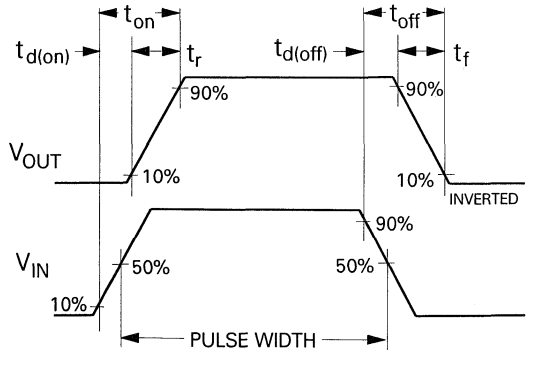

Figure 12. Switching Waveforms

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Typical Electrical Characteristics (continued)

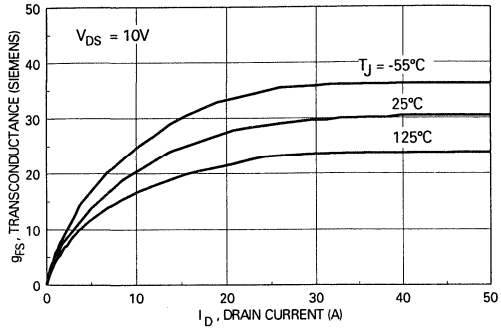


Figure 13. Transconductance Variation with Drain Current and Temperature

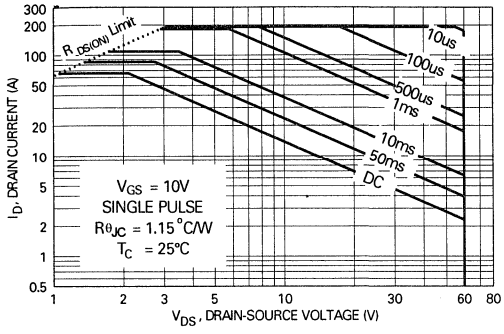


Figure 14. Maximum Safe Operating Area

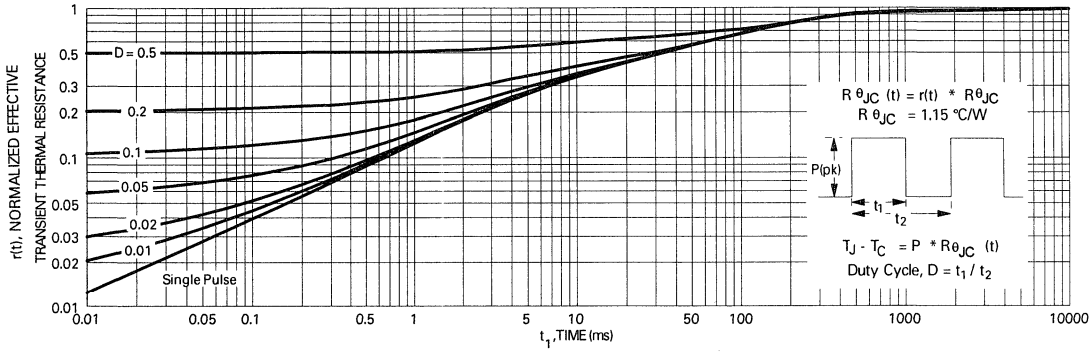


Figure 15. Transient Thermal Response Curve

National Semiconductor™

June 1996

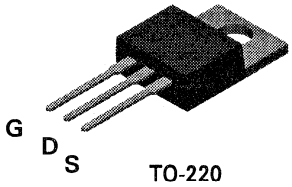
NDP7061L / NDB7061L
N-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

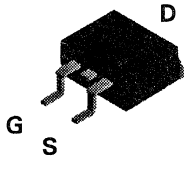
These logic level N-Channel enhancement mode power field effect transistors are produced using National's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

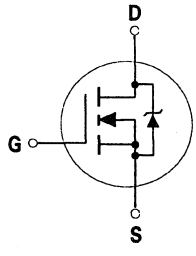
- 60 A, 60 V. $R_{DS(ON)}$ = 0.018 Ω @ V_{GS}= 5 V
  $R_{DS(ON)}$ = 0.013 Ω @ V_{GS}= 10 V.
- Low drive requirements allowing operation directly from logic drivers. $V_{GS(TH)}$ < 2.0V.
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low $R_{DS(ON)}$.
- TO-220 and TO-263 (D^2PAK) package for both through hole and surface mount applications.



TO-220
NDP Series



TO-263AB
NDB Series



Absolute Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter	NDP7061L	NDB7061L	Units
V_{DSS}	Drain-Source Voltage	60		V
V_{DGR}	Drain-Gate Voltage (R_{GS} ≤ 1 MΩ)	60		V
V_{GSS}	Gate-Source Voltage - Continuous	± 16		V
	- Nonrepetitive (t_P < 50 μs)	± 25		
I_D	Drain Current - Continuous	60		A
	- Pulsed	180		
P_D	Maximum Power Dissipation @ T_C = 25°C	130		W
	Derate above 25°C	0.87		W/°C
T_J,T_{STG}	Operating and Storage Temperature Range	-65 to 175		°C

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Electrical Characteristics (T_c = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE AVALANCHE RATINGS (Note 1)						
W_{DSS}	Single Pulse Drain-Source Avalanche Energy	V_{DD} = 30 V, I_D =60 A			500	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				60	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V			10	µA
		T_J = 125°C			1	mA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 16 V, V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -16 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note 1)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1	1.2	2	V
		T_J = 125°C	0.65	0.7	1.5	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 5 V, I_D = 30 A		0.013	0.018	Ω
		T_J = 125°C		0.023	0.032	
		V_{GS} = 10 V, I_D = 30 A		0.011	0.013	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 5 V, V_{DS} = 10 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 30 A		45		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 30 V, V_{GS} = 0 V, f = 1.0 MHz		2600		pF
C_{oss}	Output Capacitance			690		pF
C_{rss}	Reverse Transfer Capacitance			220		pF
SWITCHING CHARACTERISTICS (Note 1)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = 30 V, I_D = 60A, V_{GS} = 5 V, R_{GEN} = 10 Ω R_{GS} = 10 Ω		18	35	nS
t_r	Turn - On Rise Time			430	600	nS
$t_{D(off)}$	Turn - Off Delay Time			63	120	nS
t_f	Turn - Off Fall Time			240	400	nS
Q_g	Total Gate Charge	V_{DS}= 12 V I_D = 60 A, V_{GS} = 5 V		52	75	nC
Q_{gs}	Gate-Source Charge			9		nC
Q_{gd}	Gate-Drain Charge			28		nC

Electrical Characteristics (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRAIN-SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuos Drain-Source Diode Forward Current				60	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current				180	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 30 A (Note 1)		0.9	1.3	V
		T_J = 125°C		0.8	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_F = 60 A, dI_F/dt = 100 A/µs	40		150	ns
I_{rr}	Reverse Recovery Current		2		10	A
THERMAL CHARACTERISTICS						
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case				1.15	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient				62.5	°C/W

Note:
1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics

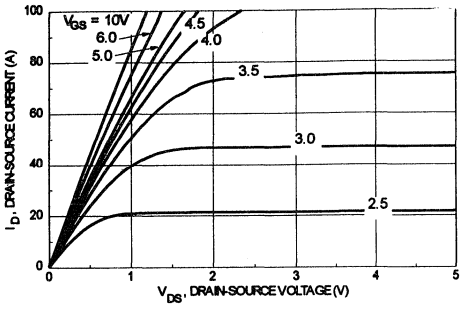

Figure 1. On-Region Characteristics

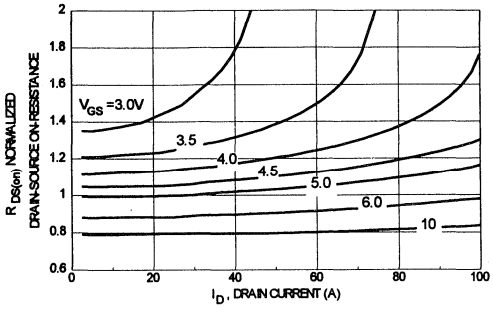

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

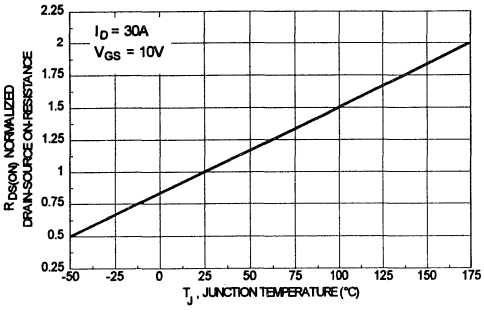

Figure 3. On-Resistance Variation with Temperature

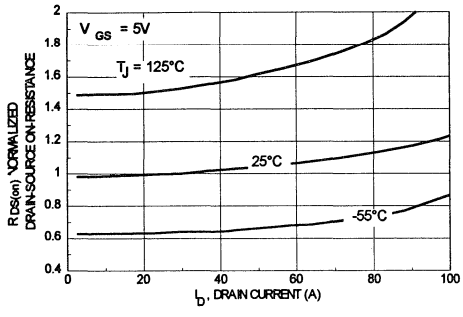

Figure 4. On-Resistance Variation with Drain Current and Temperature

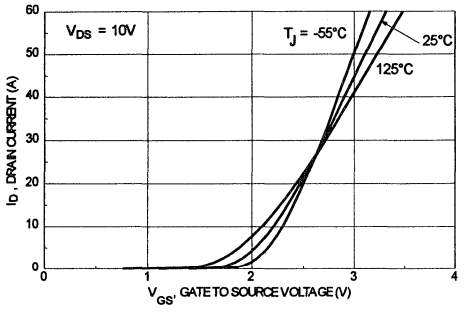

Figure 5. Transfer Characteristics

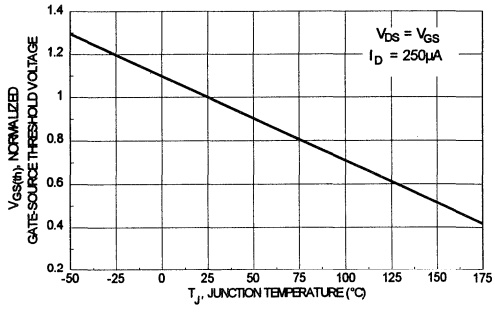

Figure 6. Gate Threshold Variation with Temperature

Typical Electrical Characteristics (continued)

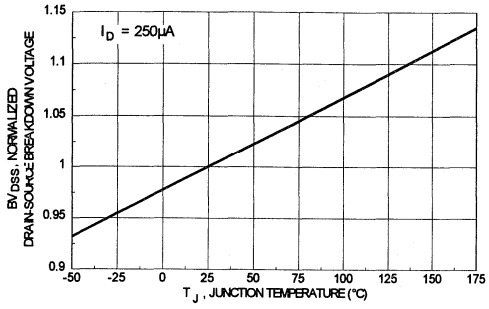

Figure 7. Breakdown Voltage Variation with Temperature

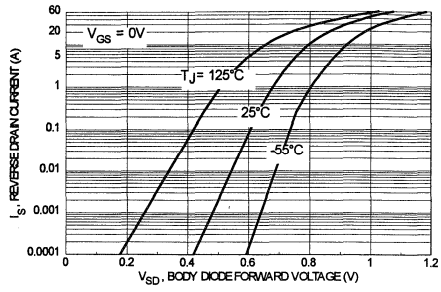

Figure 8. Body Diode Forward Voltage Variation with Current andTemperature

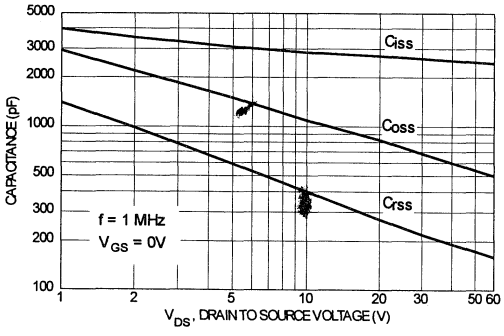

Figure 9. Capacitance Characteristics

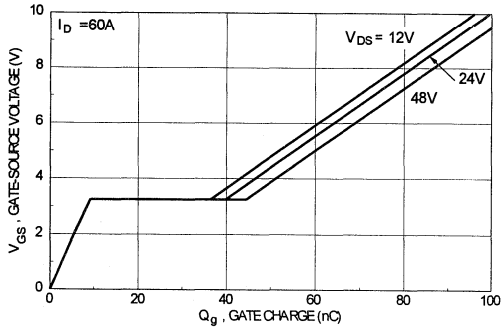

Figure 10. Gate Charge Characteristics

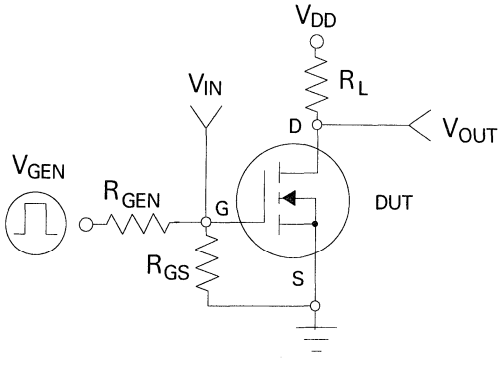

Figure 11. Switching Test Circuit

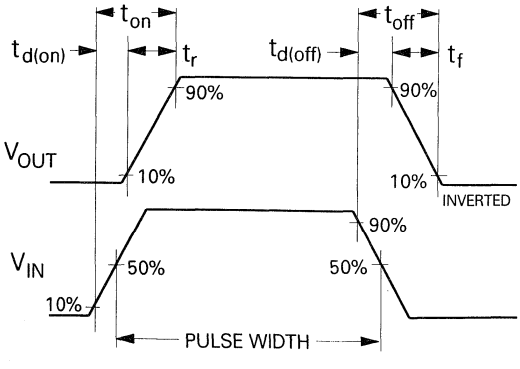

Figure 12. Switching Waveforms

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Typical Electrical Characteristics (continued)

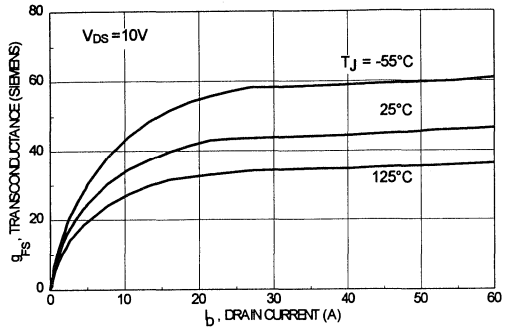

Figure 13. Transconductance Variation with Drain Current and Temperature

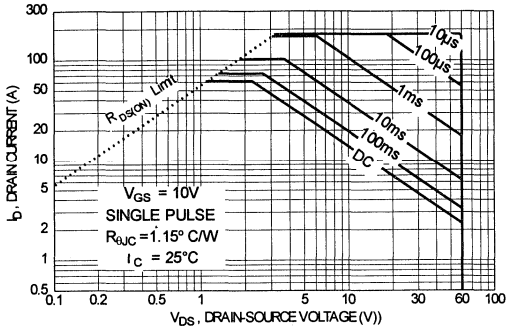

Figure 14. Maximum Safe Operating Area

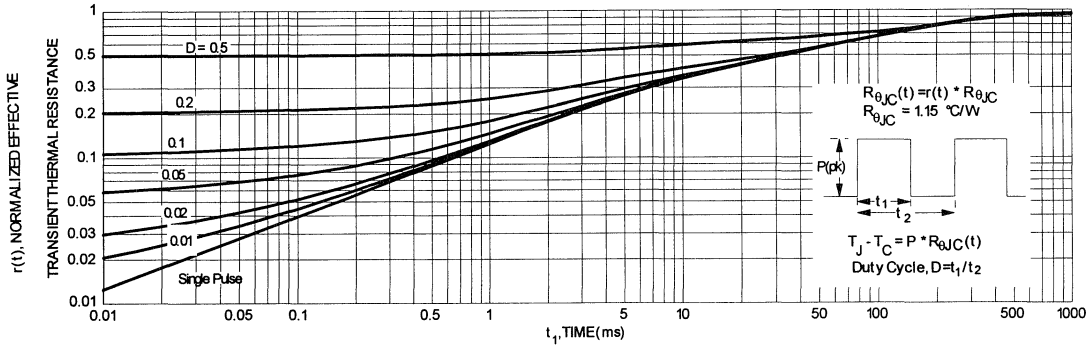

Figure 15. Transient Thermal Response Curve

Section 9
Application Notes

National Semiconductor™

AN558 Introduction to Power MOSFETs and Their Applications

Ralph Locher

INTRODUCTION

The Power MOSFETs that are available today perform the same function as Bipolar transistors except the former are voltage controlled in contrast to the current controlled Bipolar devices. Today MOSFETs owe their ever-increasing popularity to their high input impedance and to the fact that being a majority carrier device, they do not suffer from minority carrier storage time effects, thermal runaway, or second breakdown.

MOSFET OPERATION

An Understanding of the operation of MOSFETs can best be gleaned by the first considering the lateral N-channel MOSFET shown in Figure 1.

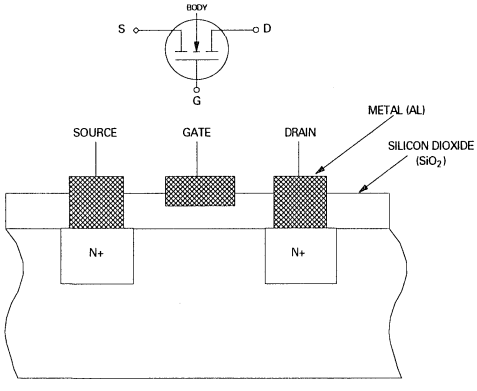

Figure 1. Lateral N-Channel MOSFET Cross-Section

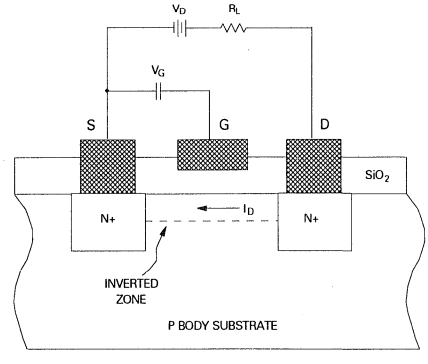

Figure 2. Lateral MOSFET Transistor Biased for Forward Current Conduction

With no electrical bias applied to the gate G, no current can flow in either direction underneath the gate because there will always be a blocking PN junction. When the gate is forward biased with respect to the source S together with an applied drain-source voltage, as shown in Figure 2, the free hole carriers in the p-epitaxial layer are repelled away from the gate area creating a channel, which allows electrons to flow from the source to the drain. Note that since the holes have been repelled from the gate channel, the electrons are the "majority carriers" by default. This mode of operation is called "enhancement" but is easier to think of enhancement mode of operation as the device being "normally off", i.e., the switch blocks the current until it receives a signal to turn on. The opposite is depletion mode, which is normally "on" device.

The advantages of the lateral MOSFET are:

1. Low gate signal power requirement. No gate current can flow into the gate after the small gate oxide capacitance has been charged.
2. Fast switching speeds because electrons can start to flow from drain to source as soon as the channel opens. The channel depth is proportional to the gate voltage and pinches closed as soon as the gate voltage is removed, so there is no storage time effect as occurs in transistors.

The major disadvantages are:

1. High resistance channels. In normal operation, the source is electrically connected to the substrate. With no gate bias, the depletion region extends out from the N+ drain in a pseudo-hemispherical shape. The channel length L cannot be made shorter than the minimum depletion width required to support the rated voltage of the device.
2. Channel resistance may be decreased by creating wider channels but this is costly since it uses up valuable silicon real estate. It also slows down the switching speed of the device by increasing its gate capacitance.

Enter vertical MOSFETs!
The Power MOSFET structure (also known as DMOS) is shown Figure 3.

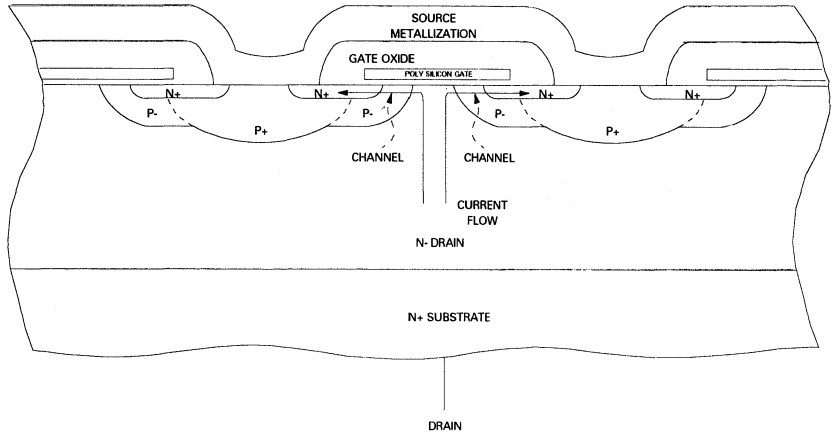

Figure 3. Vertical DMOS Cross-Sectional View

The current path is created by inverting the p-layer underneath the gate by the identical method in the lateral MOSFETs. Source current flows underneath this gate area and then vertically through the drain, spreading out as it flows down. A typical MOSFET consists of many thousands of N+ sources conducting in parallel. This vertical geometry makes possible lower on-state resistances ($R_{DS(ON)}$) for the same blocking voltage and faster switching than the lateral MOSFETs.
There are many vertical construction designs possible, e.g., V-groove and U-groove, and many source geometries, e.g. squares, triangles, hexagons, etc. The many considerations that determine the source geometry are $R_{DS(ON)}$, input capacitance, switching times and transconductance.

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PARASITIC DIODE

Early versions of MOSFETs were susceptible to voltage breakdown due to voltage transients and also had a tendency to turn on under high rates of rise of drain-to-source voltage (dV/dt), both resulting in catastrophic failures. The dV/dt turn-on was due to the inherent parasitic NPN transistor incorporated within the MOSFET, shown schematically in Figure 4a. Current flow needed to charge up junction capacitance C_{DG} acts like base current to turn on the parasitic NPN.
The parasitic NPN action is suppressed by shorting the N+ source to the P+ body using the source metallization. This now creates an inherent PN diode in anti-parallel to the MOSFET transistor (see Figure 4b). Because of its extensive junction area, the current ratings and thermal resistance of this diode does exhibit a very long reverse recovery time and large reverse recovery current due to the long

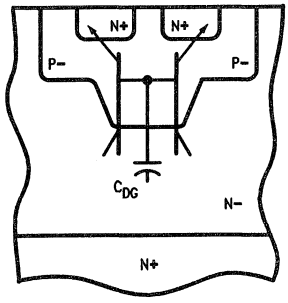


Figure 4a. DMOS Construction Showing Location of the Parasitic NPN Transistor

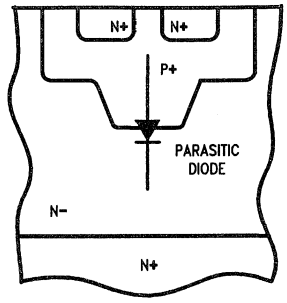


Figure 4b. Parasitic Diode

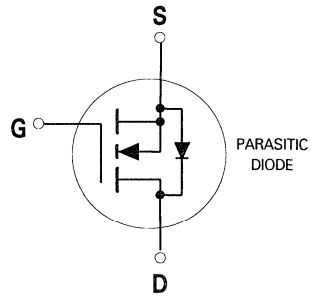


Figure 4c. Circuit Symbol

minority carrier lifetimes in the N-drain layer, which precludes the use of this diodes except for very low frequency applications. e.g., motor control circuit shown in Figure 5. However in high frequency applications, the parasitic diode must be paralleled externally by an ultra-fast rectifier to ensure that the parasitic diode does not turn on. Allowing it to turn will substantially increase the device power dissipation due to the reverse recovery losses within the diode and also leads to higher voltage transients due to the larger reverse recovery current.

CONTROLLING THE MOSFET

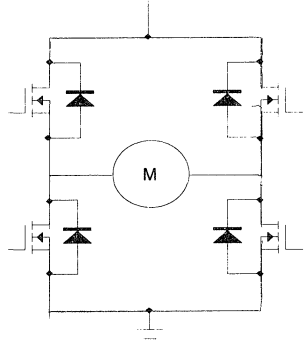


Figure 5. Full-Wave Motor Control Circuit

A major advantage of the Power MOSFET is its very fast switching speeds. The drain current is strictly proportional to gate voltage so that the theoretically perfect device could switch in 50ps - 200ps, the time it takes the carriers to flow from source to drain. Since the MOSFET is a majority carrier device, a second reason why it can outperform the junction transistor is that its turn-off is not delayed by minority carrier storage time in the base. A MOSFET begins to turn off as soon as its gate voltage drops down to its threshold voltage.

SWITCHING BEHAVIOR

Figure 6 illustrates a simplified model for the parasitic capacitances of a Power MOSFET and switching voltage waveforms with a resistive load.
There are several different phenomena occurring during turn-on. Referring to the same figure:

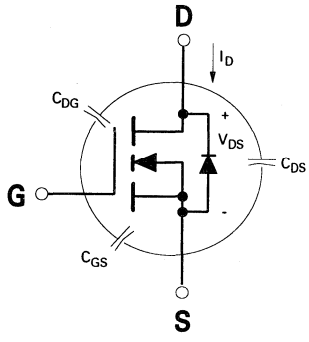


Figure 6a. MOSFET Capacitance Model for Power MOSFET

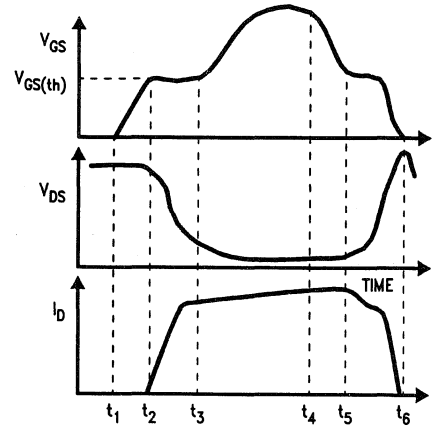


Figure 6b. Switching Waveforms for Resistive Load

Time interval t1<t<t2:

The initial turn-on delay time $t_{d(ON)}$ is due to the length of time it takes V_{GS} to rise exponentially to the threshold voltage $V_{GS(TH)}$. From Figure 6, the time constant can be seen to be $R_S x C_{GS}$. Typical turn-on delay approximation is:

$$t_{d(on)} = R_S \times C_S \times \ln\left(1 - \frac{V_{GS(th)}}{V_{PK}}\right) \qquad (1)$$

Note that since the signal source impedance appears in the t_d equation, it is very important to pay attention to the test conditions used in measuring switching times.
Physically one can only measure input capacitance C_{iss}, which consists of C_{GS} in parallel with C_{DG}. Even though $C_{GS}>>C_{DG}$, the later capacitance undergoes a much larger voltage excursion so its effect on switching time can not be neglected.
Plots of C_{iss}, C_{oss}, and C_{rss} for the National Semiconductor Supersot™ NDS351N are shown in Figure 7 below. The charging and discharging of C_{DG} is analogous to the "Miller" effect that was first discovered with electron tubes and dominates the next switching interval.

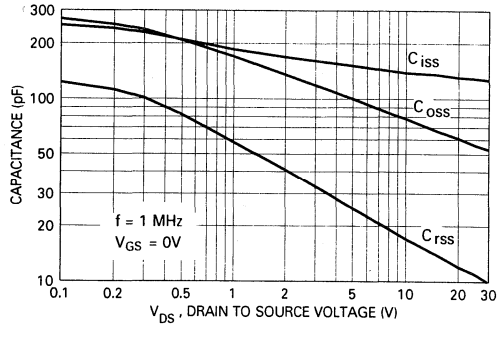


Figure 7. Typical Capacitances of NDS351N

Time interval t2<t<t3:

Since V_{GS} has now achieved the threshold value, the MOSFET begins to draw increasing load current and V_{DS} decreases. C_{DG} must not only discharge but its capacitance value also increases since it is inversely proportional to V_{DS}, namely:

$$C_{DG} = \frac{C_{DG}(0)}{V_{DG}^{n}} \qquad (2)$$

Unless the gate driver can quickly supply the current required to discharged C_{DG}, voltage fall will be slowed with the attendant increases in turn-on time.

Time interval t3<t<t4:

The MOSFET is now on so the gate voltage can rise to the overdrive level.

Turn-off interval t4<t<t6:

Turn-off occurs in reverse order. V_{GS} must drop back close to the threshold value before $R_{DS(ON)}$ will start to increase. As V_{DS} starts to rise, the Miller effect due to C_{DG} re-occurs and impedes the rise of V_{DS} as C_{DG} recharges to V_{CC}.
Specific gate drive circuits for different applications are discussed and illustrated later in this paper.

MOSFET CHARACTERIZATION

The output characteristics (I_D vs V_{DS}) of the National Semiconductor Supersot™ NDS351N are illustrated in Figures 8 and 9. The two distinct regions of operation in Figure 8 have been labeled "linear" and "saturated". To understand the difference, recall that the actual current path in a MOSFET is horizontal through the channel created under the gate oxide and then vertical through the drain. In the linear region of operation, the voltage across the MOSFET channel is not sufficient for the carriers to reach their maximum current density. The static $R_{DS(ON)}$, defined simply as V_{DS}/I_{DS}, is a constant.
As V_{DS} is increased, the carriers reach their maximum drift velocity and the current amplitude cannot increase. Since the device is behaving like a current generator, it is said to have high output impedance. This is the so-called "saturation" regions. One should also note that in comparing MOSFET operation to Bipolar transistor, the linear and saturated regions of the are just the opposite to the MOSFET. The equal spacing between the output I_D curves for constant step in V_{GS} indicates that the transfer characteristics in Figure 9 will be linear in the saturated region.

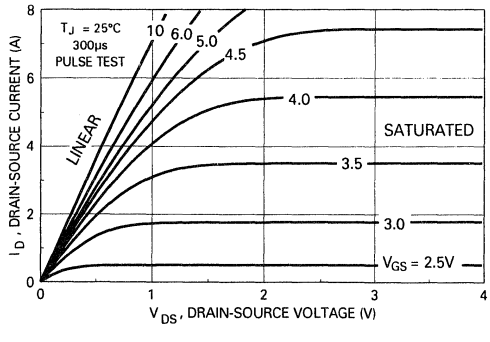


Figure 8. NDS351N Output Characteristics

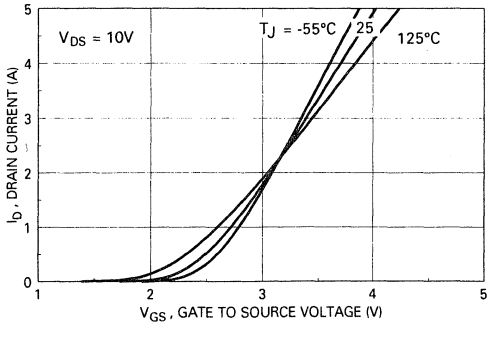


Figure 9. NDS351N Transfer Characteristics

IMPORTANT OF THRESHOLD VOLTAGE

Threshold voltage $V_{GS(th)}$ is the minimum gate voltage that initiates drain current flow. $V_{GS(th)}$ can be easily measured on a Tektronix 576 curve tracer by connecting the gate to the drain and recording the required drain voltage for a specified drain current, typically 250μA. $V_{GS(th)}$ in Figure 9 is 1.6V. While a high value of $V_{GS(th)}$, can apparently lengthen turn-on delay time, a low value for Power MOSFET is undesirable for the following reasons:

1. $V_{GS(th)}$ decreases with increased temperature.
2. The high gate impedance of a MOSFET makes it susceptible to spurious turn-on due to gate noise.
3. One of the more common modes of failure is gate-oxide voltage punch-through. Low $V_{GS(th)}$ requires thinner oxides, which lowers the gate oxide voltage rating.

POWER MOSFET THERMAL MODEL

Like all other power semiconductor devices, MOSFET operate at elevated junction temperature. It is important to observe their thermal limitations in order to achieve acceptable performance and reliability. Specification sheets contain information on maximum junction temperature ($T_{J(max)}$), safe operating areas, current ratings and electrical characteristics as a function of T_J where appropriate. However, since it is still not possible to cover all contingencies, it is still important that the designer perform some junction calculations to ensure that the device operates within specifications.

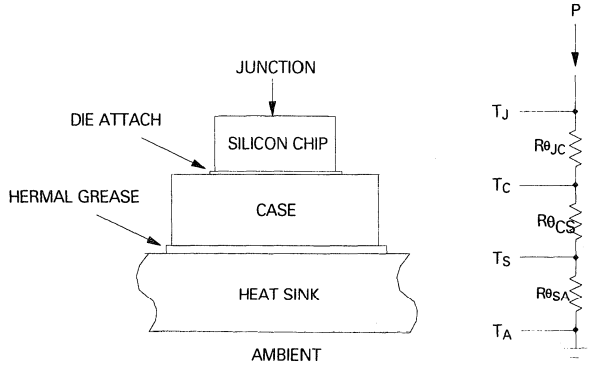


Figure10. MOSFET Steady-State Thermal Resistance Model

Figure 10 shows an elementary, steady-state, thermal model for any power semiconductor and the electrical analogue. The heat generated at the junction flows through the silicon pellet to the case or tab and then to the heat sink. The junction temperature rise above the surrounding environment is directly proportional to this heat flow and the junction-to-ambient thermal resistance. The following equation defined the steady-state thermal resistance $R_{\theta JA}$ between device junction to ambient:

$$R_{\theta JA} = \frac{T_J - T_A}{P} \qquad (3)$$

where:
T_J = average temperature at the device junction (°C)
T_A = average temperature at ambient (°C)
P = average heat flow in watts (W).
Note that for thermal resistance to be meaningful, two temperature reference points must be specified. Units for $R_{\theta JA}$ are °C/W.

The thermal model show symbolically the locations for the reference points of junction temperature, case temperature, sink temperature and ambient temperature. These temperature reference define the following thermal resistances:

$R_{\theta JC}$: Junction-to-Case thermal resistance.

$R_{\theta CS}$: Case-to-Sink thermal resistance.

$R_{\theta SA}$:Sink-to-Ambient thermal resistance.

Since the thermal resistances are in series:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \qquad (4)$$

The design and manufacture of the device determines $R_{\theta JC}$ so that while $R_{\theta JC}$ will vary somewhat from device to device, it is SOLE RESPONSIBILITY of the manufacturer to guarantee a maximum value for $R_{\theta JC}$. Both the user and manufacturer must cooperate in keeping $R_{\theta CS}$ to an acceptable maximum and finally the user has sole responsibility for the external heat sinking.

By inspection of Figure 10, one can write an expression for T_J:

$$T_J = T_A + P \times (R_{\theta JC} + R_{\theta CS} + R_{\theta SA}) \qquad (5)$$

While this appears to be a very simple formula, the major problem using it is due to the fact that the power dissipated by the MOSFET depends upon T_J. Consequently one must use either an iterative or graphical solution to find the maximum $R_{\theta SA}$ to ensure stability. But an explanation of transient thermal resistance is in order to handle the case of pulsed applications.

Use of steady-state thermal resistance is not satisfactory for finding peak junction temperatures for pulsed applications. Plugging in the peak power value results in overestimating the actual junction temperature while using the average power value underestimates the peak junction temperature at the end of the power pulse. The reason for the discrepancy lies in the thermal capacity of the semiconductor and its housing, i.e., its ability to store heat and to cool down before the next pulse.

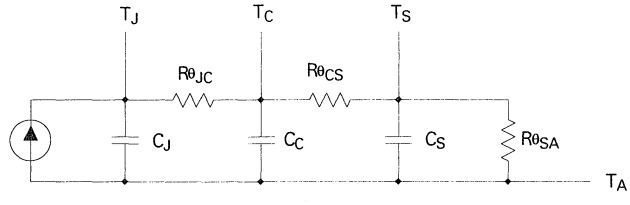


Figure 11. Transient Thermal Resistance Model

The modified thermal model for the MOSFET is shown in Figure 11. The normally distributed thermal capacitances have been lumped into single capacitors labeled C_J, C_c, and C_S. This simplification assumes current is evenly distributed across the silicon chip and that the only significant power losses occur in the junction. When a step pulse of heating power P is introduced at the junction. Figure 12a shows that T_J will rise at an exponential rate to some steady state value dependent upon the response of the thermal network. When the power input is terminated at time t2, T_J will decrease along the curve indicated by Tcool in Figure 12a back to its initial value. Transient thermal resistance at time t is thus defined as:

$$Z_{\theta JC} = \frac{\Delta T_{JC}(t)}{P} \qquad (6)$$

The transient thermal resistance curve approaches the steady-state value at long times and the slope of the curve for short times is inversely proportional to C_J. In order that this curve can be used with

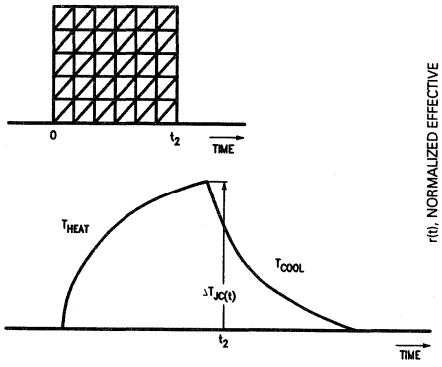


Figure 12a. Junction Temperature Response to a Step Pulse of Heating Power

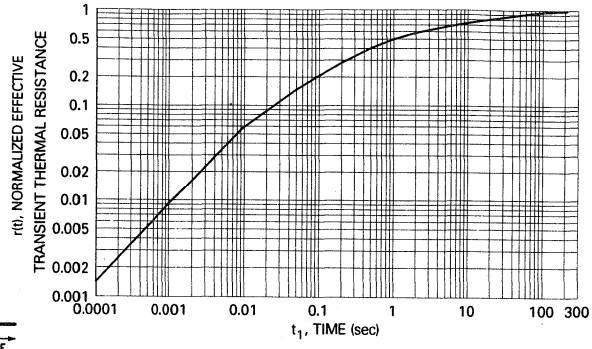


Figure 12b. Transient Thermal Resistance Curve for NDS351N

confidence, it must represent the highest values $Z_{\theta JC}$ for each time interval that can be expected from the manufacturing distribution of the products.

While predicting T_J in response to a series of power pulses becomes very complex, superposition of power pulses offers a rigorous numerical method of using the transient thermal resistance curve to secure a solution. Superposition tests the response of a network to any input function by replacing the input with an equivalent series of superimposed positive and negative step functions. Each step function must start from zero and continue to the time for which T_J is to be computed. For example, Figure 13 illustrates a typical train of heating pulses.

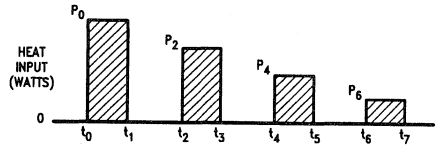


Figure 13a. Heat Input

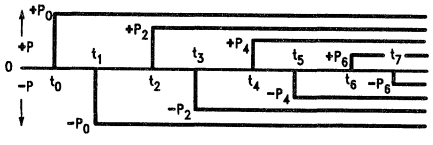


Figure 13b. Equivalent Heat Input by Superposition of Power Pulses

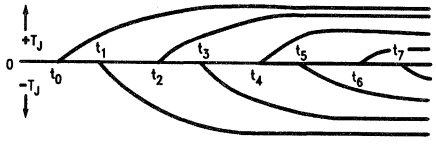


Figure 13c. Junction Temperature Response to Individual Power Pulse

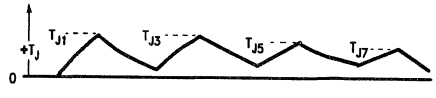


Figure 13d. Use of Superposition to Determine Peak T_J

T_J at time is given by:

$$T_J(t) = T_J(0) + \Sigma P_i \times [Z_{\theta JC}(t_n - t_i) - Z_{\theta JC}(t_n - t_i + 1)] \qquad (7)$$

The typical use condition is to compute the peak junction temperature at thermal equilibrium for a train of equal amplitude power pulses as shown in Figure 14.

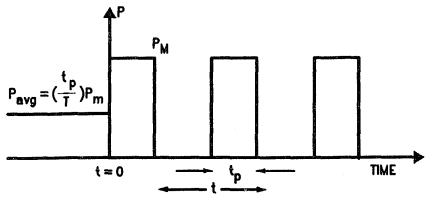


Figure 14a. Train of Power Pulses

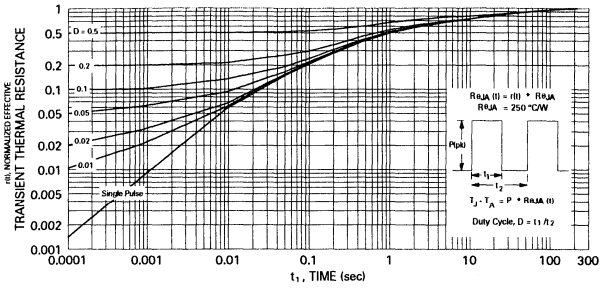


Figure 14b. Normalized r(t) for NDS351N

To further simplify this calculation, the bracketed expression in equation (G) has been plotted for all National Semiconductor Power MOSFETs, as exemplified by the plot of $Z_{\theta JC}$ in Figure 14b. From this curve, one can readily calculate T_J if one knows P_M, $Z_{\theta JC}$ and T_C using the expression:

$$T_J = T_C + P_M \times Z_{\theta JC} \qquad (8)$$

Example: Compute the maximum junction temperature for a train of 1W, 10ms wide heating pulses repeated every 100ms. Assume a case temperature of 55°C.
Duty factor=0.1
From Figure 14b: $Z_{\theta JC}$=0.14*250°C/W=35°C/W
Substituting into Equation (7):
$T_{J(max)}$=55+1*35=90°C

SAFE OPERATING AREA

The Power MOSFET is not subjected to forward or reverse bias second breakdown, which can easily occur in transistors. Second breakdown is a potentially catastrophic condition in transistors caused by thermal hot spots in the silicon as the transistor turns on or off. However in the MOSFET, the carriers travel through the device much as if it were a bulk semiconductor, which exhibits positive temperature coefficient. If current attempts to self-constrict to a localized area, the increasing temperature of the spot will raise the spot resistance due to positive temperature coefficient of the bulk silicon. The ensuing higher voltage drop will tend to redistribute the current away from the hot spot. Figure 15 shows the safe operating area of the National Semiconductor Supersot™ NDS351N device.

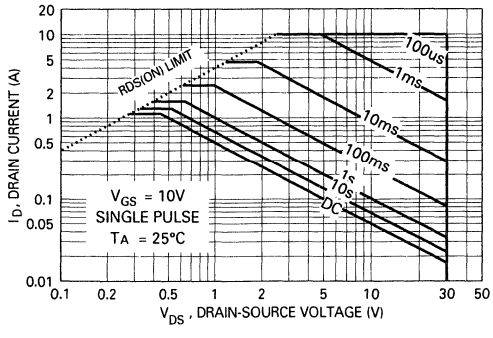


Figure 15. Safe Operating Area of NDS351N

Note that the safe area boundaries are only thermally limited and exhibit no derating for second breakdown. This shows that while the MOSFET transistor is very rugged, it may still be destroyed thermally by forcing it to dissipate too much power.

ON-RESISTANCE $R_{DS(ON)}$

The on-resistance of a Power MOSFET is a very important parameter because it determines how much current the device can carry for low to medium frequency (less than 200kHz) applications. After being turned on, the on-state is defined simply as its on-state voltage divided by on-state current. When conducting current as a switch, the conduction losses P_C are:

$$P_C = I^2_{D(RMS)} \times R_{DS(ON)} \qquad (9)$$

To minimize $R_{DS(ON)}$, the applied gate signal should be large enough to maintain operation in the linear or ohmic region as shown in Figure 8. National Semiconductor SUPERSOT™-3 NDS351N will conduct its rated current for V_{GS}=4.5V, which is also the value used to generate the curves of $R_{DS(ON)}$ vs I_D and T_J that are shown in Figure 16 for the National Semiconductor Supersot NDS351N. Since $R_{DS(ON)}$ is a function of T_J, Figure 16 plots this parameter at varies junction temperatures.
Note that as the drain current rises, $R_{DS(ON)}$ increases once I_D exceeds the rated current value. Because the MOSFET is a majority carrier device, the component of $R_{DS(ON)}$ due to the bulk resistance of the N-silicon in the drain region increases with temperature as well. While this must be taken into account to avoid thermal runaway, it does facilitate parallel operation of MOSFETs. Any imbalance between MOSFETs does not result in current hogging because the device with the most current heat up and ensuing higher on-voltage will divert some current to the other devices in parallel.

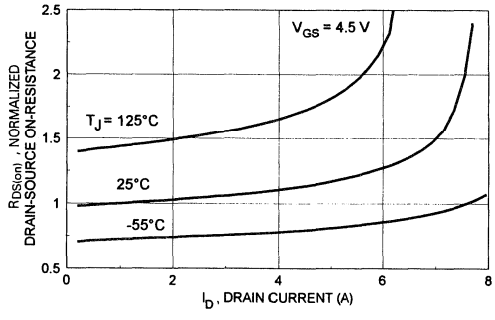


Figure 16. $R_{DS(ON)}$ of NDS351N

9

TRANSCONDUCTANCE

Since MOSFETs are voltage controlled, it has become necessary to resurrect the term transconductance g_{FS}, commonly used in the past with electron tubes. Referring to Figure 8, g_{FS} equals to the change in drain current divided by the change in gate voltage for a constant drain voltage. Mathematically:

$$g_{fs}(Siemens) = \frac{dI_D(A)}{dV_{GS}(V)} \qquad (10)$$

Transconductance varies with operating conditions, starting at 0 for $V_{GS}<V_{GS(th)}$ and peaking at a finite value when the device is fully saturated. It is very small in the ohmic region because the device cannot conduct any more current. Transconductance is useful in designing linear amplifiers and does not have any significance in switching power supplies.

GATE DRIVE CIRCUITS FOR POWER MOSFETs

The drive circuit for a Power MOSFET will affect its switching behavior and its power dissipation. Consequently the type of drive circuitry depends upon the application. If on-state power losses due to $R_{DS(ON)}$, will predominate, there is little point in designing a costly drive circuit. This power dissipation is relatively independent of gate drive as long as the gate-source voltage exceeds the threshold voltage by several volts and an elaborate drive circuit to decrease switching times will only create additional EMI and voltage ringing. In contrast, the drive circuit for a device switching at 200KHz or more will affect the power dissipation since switching losses are a significant part of the total power dissipation.
Compare to a junction transistor, the switching losses in a MOSFET can be made much smaller but these losses must still be taken into consideration. Examples of several typical loads along with the idealized switching waveforms and expressions for power dissipation are given in Figure 17 to 19.

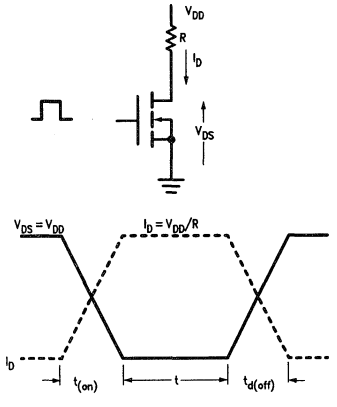


Figure17. Resistive Load Switching Waveforms

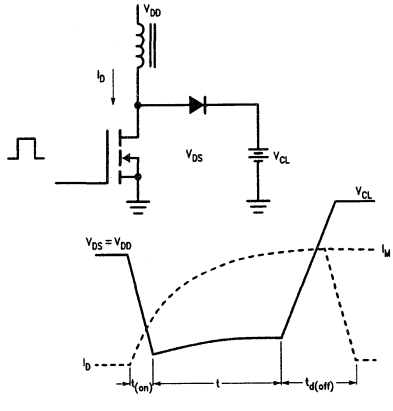


Figure18. Clamped Inductive Load Switching Waveforms

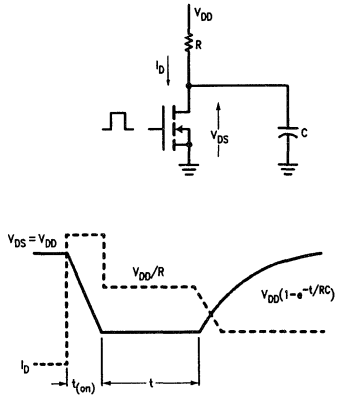


Figure19. Capacitive Load Switching Waveforms

Their power losses can be calculated from the general expression:

$$P_D = (\tfrac{1}{\tau}\int I_D(t)\times V_{DS}(t)dt)\times f_S \qquad (11)$$

where f_S =Switching frequency.
For the idealized waveforms shown in the figures, the integration can be approximated by the calculating areas of triangles:
Resistive loads:

$$P_D = \frac{V_{DD}^2}{R}\left[\frac{t(on)+t(off)}{6} + R_{DS(ON)}\times T\right]\times f_S$$

Inductive Load:

$$P_D = \frac{V_{CL}\times I_m\times t(off)\times f_S}{2} + P$$

where P_C = conduction loss during period T.
Capacitive load:

$$P_D = \left(\frac{C \times V_{2DD}}{2} + \frac{V_{DD}^2 \times R_{DS(ON)}}{R^2} \times T \right) \times f_S$$

Gate losses and blocking losses can usually be neglected. Using these equations, circuit designer is able to estimate the require heat sink. A final heat run in a controlled temperature environment is necessary to ensure thermal stability.
Since a MOSFET is essentially voltage controlled, the only gate current required is that necessary to charge the input capacitance Ciss. In contrast to a 10A transistor, which may require a base current of 2A to ensure saturation, a Power MOSFET can be driven directly by CMOS or open-collector TTL logic circuit similar to that in Figure 20.

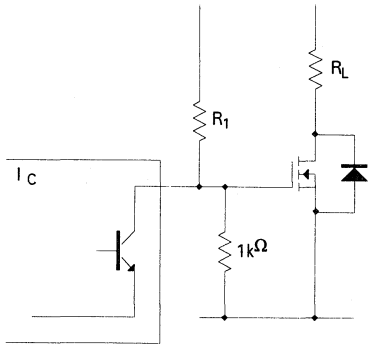


Figure 20. Open Collector TTL Drive Circuit

Turn-on speed depends upon the selection of resistor R1, whose minimum value will be determined by the current sinking rating of the IC. It is essential that an open collector TTL buffer be used since the voltage applied to the gate must exceed the MOSFET threshold voltage. CMOS devices can be used to drive the power device directly since they are capable of operating of 15V supplies.
Interface ICs, originally intended for other applications, can be used to drive the Power MOSFETs, as shown below in Figure 21.

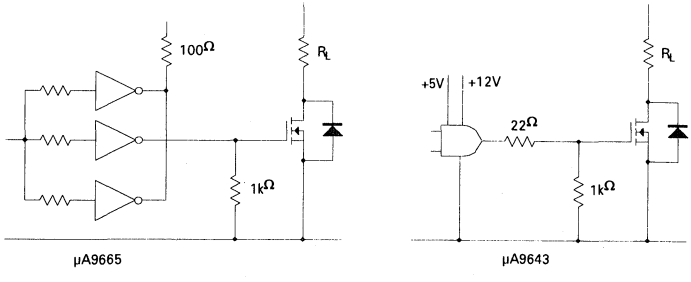


Figure 21. Interface ICs Used to Drive Power MOSFETs

Most frequently switching power supply applications employ a pulse width modulator IC with an NPN transistor output stage. This output transistor is ON when the MOSFET should be ON, hence the type of

drive used with open-collector TTL devices cannot be used. Figures 22 and 23 give examples of typical drive circuits used with PWM ICs.

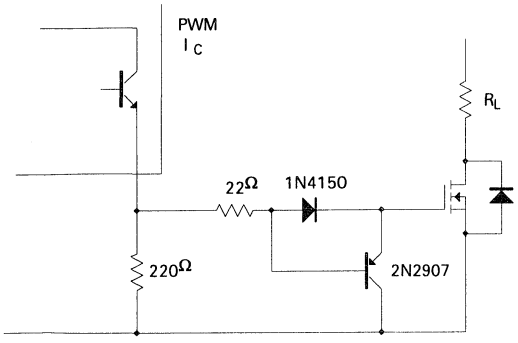


Figure 22. Circuit for PWM IC Driving MOSFET. The PNP Transistor Speeds Up Turn-Off

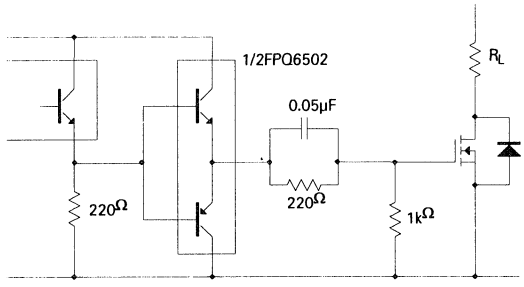


Figure 23. Emitter Follower with Speed-Up Capacitor

Isolation: Off-line switching power supplies use power MOSFETs in a half bridge configuration because inexpensive, high voltage devices with low $R_{DS(ON)}$ are not available.
Since one of the power devices is connected to the positive rail, its drive circuitry is also floating at a high potential. The most versatile method of coupling the drive circuitry is to use a pulse transformer. Pulse transformers are also normally used to isolate the logic circuitry from the MOSFETs operating at high voltage to protect it from a MOSFET failure.

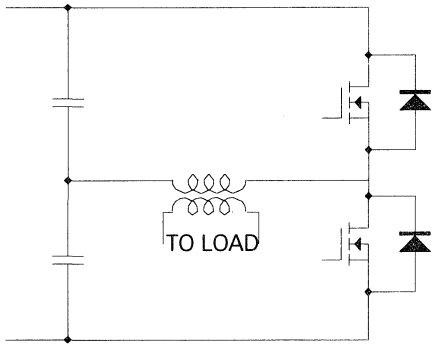


Figure 24. Half-Bridge Configuration

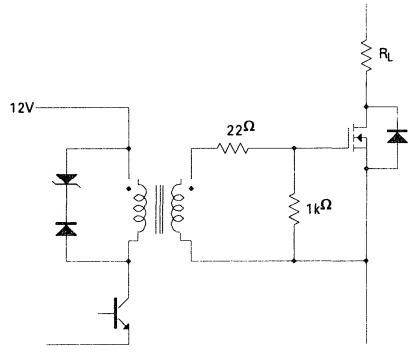


Figure 25. Simple Pulse Transformer Drive Circuit. The Transistor May Be a Part of a PWM IC if Applicable

The zener diodes shown in Figure 25 is included to reset the pulse transformer quickly. The duty cycle can approach 50% with a 12V zener diode. For better performance at turn-off, a PNP transistor can be added as shown in Figure 26.
Figure 27 illustrates an alternate method to reverse bias the MOSFET during turn-off by inserting a capacitor in series with the pulse transformer. The capacitor also ensures that the pulse transformer will not saturate due to DC bias.
Opto-isolators may also be used to drive power MOSFETs but their long switching times make them suitable only for low frequency applications.

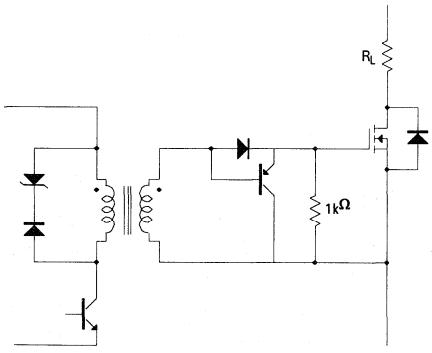


Figure 26. Improved Performance at Turn-Off with a Transistor

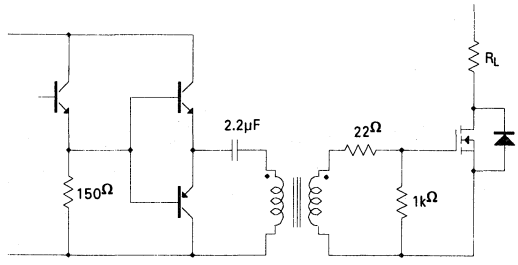


Figure 27. Emitter Follower Driver with Speed-Up Capacitor

SELECTING A DRIVE CIRCUIT

Any of the circuits shown are capable of turning a Power MOSFET on and off. The type of circuit depends upon the application. The current sinking and sourcing capabilities of the drive circuit will determine the switching time and switching losses of the power device. As a rule, the higher the gate current at turn-on and turn-off, the lower the switching losses will be. However, fast drive circuits may produce ringing in the gate circuit and drain circuits. At turn-on, ringing in the gate circuit may produce a voltage transient in excess of the maximum V_{GS} rating, which will puncture the gate oxide and destroy it. To prevent this occurrence, a zener diode of appropriate value may be added to the circuit as shown in Figure 28. Note that the zener should be mounted as close as possible to the device.
At turn-off, the gate voltage may ring back up to the threshold voltage and turn on the device for a short period. There is also the possibility that the drain-source voltage will exceed its maximum rated voltage due to ringing in the drain circuit. A protective RC snubber circuit or zener diode may be added to limit drain voltage to a safe level.

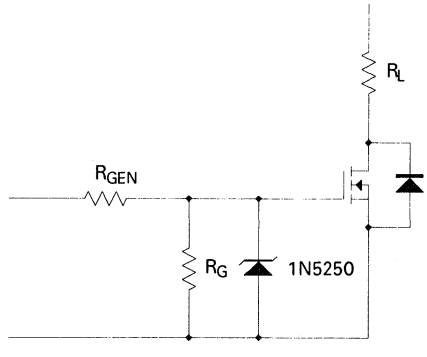


Figure 28. Zener Diode to Prevent Excessive Gate-Source Voltages

Maximum Power Enhancement Techniques for SuperSOT™-3 Power MOSFETs

Alan Li , Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong

1. Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of the SuperSOT™-3 Power MOSFET offered by National Semiconductor. This effort allows the user to take full advantage of the exceptional performance features of National's state-of-the-art Power MOSFET which offers very low on-resistance and improved junction-to-case ($R_{\theta JC}$) thermal resistance. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the drain lead of the Power MOSFET is mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

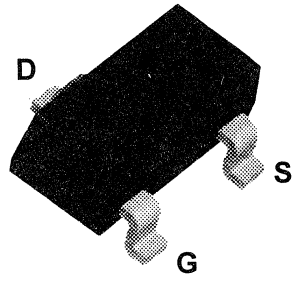


Figure 1. SuperSOT™-3 Power MOSFET has the same package dimensions as the SOT-23 but the maximized copper lead frame reduces the junction-to-case thermal resistance $R_{\theta JC}$ to 75°C/W.

2. Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and the junction-to-ambient thermal resistance.

$$P_{Dmax} = (T_{Jmax} - T_A) / R_{\theta JA} \qquad (2.1)$$

The term junction refers to the point of thermal reference of the semiconductor. Equation 2.1 can also be applied to the transient-state:

$$P_{Dmax}(t) = [T_{Jmax} - T_A] / R_{\theta JA}(t) \quad (2.2)$$

where P_{Dmax} (t) and $R_{\theta JA}(t)$ are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}(t)$ increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details.

Nevertheless, National provides a Discrete SPICE Thermal Model (LIT#570240-002) for general thermal evaluation. User may find these models helpful in determining the dynamic power and temperature limits in the application.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and $R_{\theta CA}$ case-to-ambient thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad (2.3)$$

The case thermal reference of the SuperSOT™-3 Power MOSFET is defined as the point of contact between the drain lead of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint. On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

3. Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 Oz copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in figure 2 and table 1. Layouts 1 to 6 have the copper pad sizes from 0.001 to 0.4 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.02 to 0.4 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.02 to 0.4 square inches divided equally on both sides of the board.

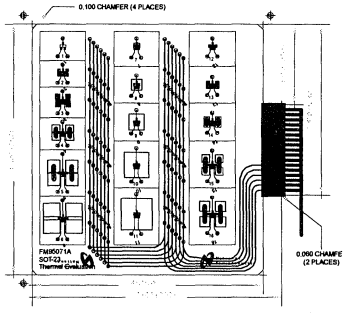


Figure 2. Top Side of the 4.5"x5" SuperSOT™-3 Thermal Board. Complete scale drawings is shown in section 5.

Layout	2 Oz Copper Mounting Pad Area (in^2)	Relative Placement on Board
1-6	0.001, 0.02, 0.05, 0.1, 0.25, 0.4	Top
7-11	0.02, 0.05, 0.1, 0.25, 0.4	Bottom
12-16	0.02, 0.05, 0.1, 0.25, 0.4	1/2 Top and 1/2 Bottom

Table 1: Thermal Board Configurations

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to appendix B for details.

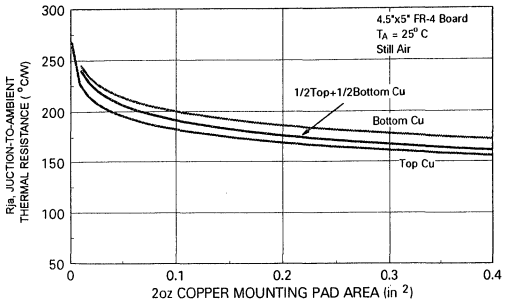


Figure 3. SuperSOT™-3 Junction-to-Ambient thermal resistance versus copper mounting pad area and its surface placement.

Plots in figure 3 show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 270 to 160°C/W in the range from 0.001 to 0.4 square inches. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 2 to 15°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into equation 2.1, the steady-state maximum power dissipation curves can be obtained and are shown in figure 4.

A 30% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.001 to 0.02 in^2, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

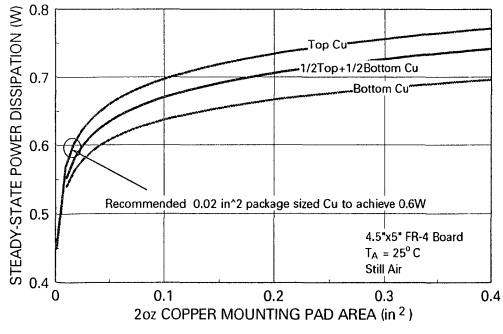


Figure 4. Maximum Power Dissipation Curves for SuperSOT™-3. 0.02 in^2 2 Oz copper mounting pad area, layout 2, is recommended to achieve approximately 0.6W.

4. Conclusion

National Semiconductor has attempted to define the thermal performance of the SuperSOT™-3 Power MOSFET, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

1. Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
2. Placement of the copper pads on the top side of the board gives the best thermal performance.
3. The most cost effective approach of designing layout 2 0.02 square inches copper pad directly under the package without occupying additional board space, can increase the maximum power from approximately 0.46 to 0.6W.
4. Maximum thickness of the copper pad should be used for cost performance trade off.

5. Thermal Board Layout

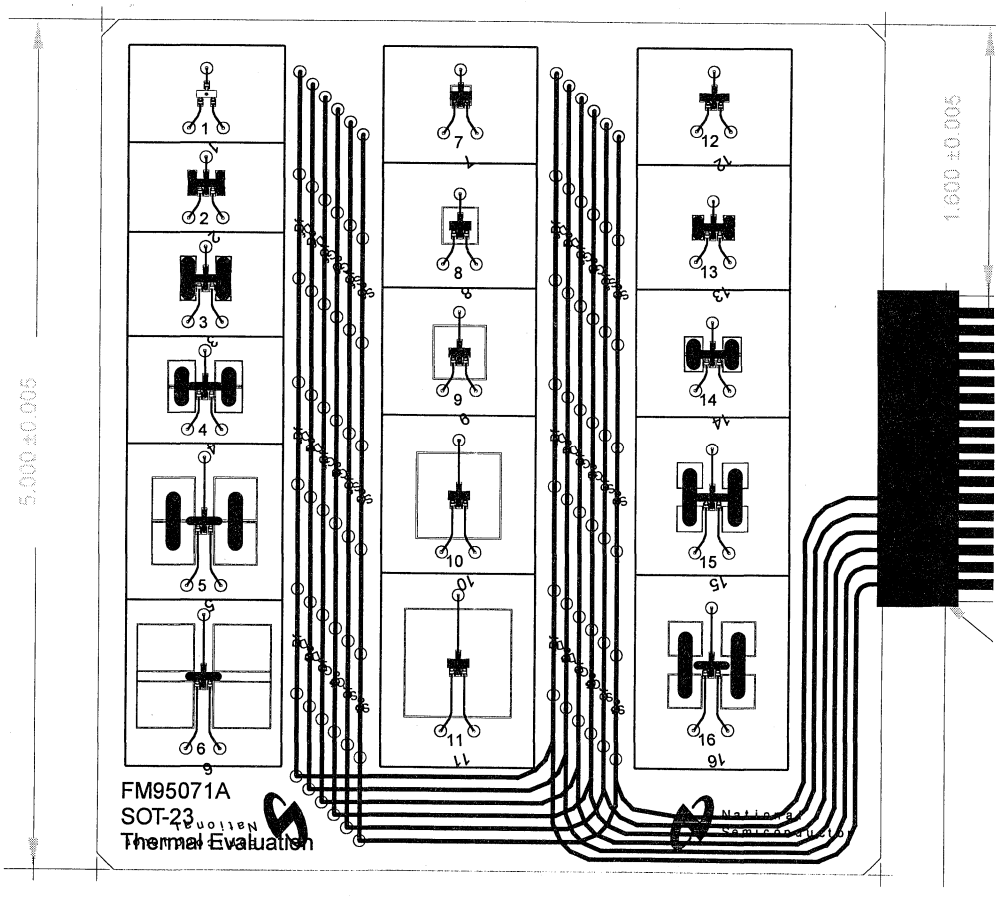


Figure 5. SuperSOT™-3 (SOT-23) Thermal Board Top and Bottom View. Scale 1:1 in letter size paper.

Maximum Power Enhancement Techniques for SuperSOT™-6 Power MOSFETs

Alan Li , Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong

1. Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of the SuperSOT™-6 Power MOSFET offered by National Semiconductor. This effort allows the user to take full advantage of the exceptional performance features of National's state-of-the-art Power MOSFET which offers very low on-resistance and improved junction-to-case ($R_{\theta JC}$) thermal resistance. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the drain leads of the Power MOSFET are mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

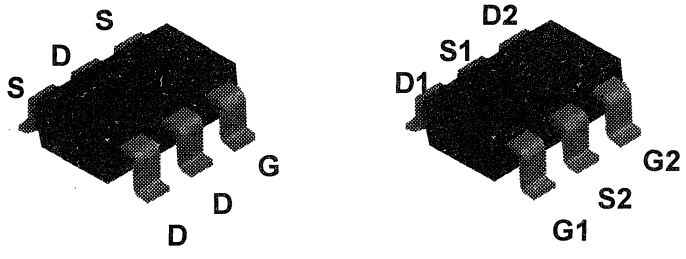


Figure 1. SuperSOT™-6 Power MOSFET achieves junction-to-case thermal resistance $R_{\theta JC}$ of 30°C/W for single device and 60°C/W for dual devices.

2. Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and the junction-to-ambient thermal resistance.

$$P_{Dmax} = (T_{Jmax} - T_A) / R_{\theta JA} \qquad (2.1)$$

The term junction refers to the point of thermal reference of the semiconductor. Equation 2.1 can also be applied to the transient-state:

$$P_{Dmax}(t) = [T_{Jmax} - T_A] / R_{\theta JA}(t) \quad (2.2)$$

where P_{Dmax} (t) and $R_{\theta JA}(t)$ are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}(t)$ increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details. Nevertheless, National provides a Discrete SPICE Thermal Model (LIT#570240-002) for general thermal evaluation. User may find these models helpful in determining the dynamic power and temperature limits in the application.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and $R_{\theta CA}$ case-to-ambient thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad (2.3)$$

The case thermal reference of the SuperSOT™-6 Power MOSFET is defined as the point of contact between the drain leads of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint. On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

3. Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 Oz copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in figure 2 and table 1. For single device, layouts 1 to 6 have the copper pad sizes from 0.003 to 0.4 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.03 to 0.4 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.02 to 0.4 square inches divided equally on both sides of the board. For dual devices, layouts 1, 2, and 5 have copper sizes from 0.0015 to 0.125 sqaure inches on the top side of the board.

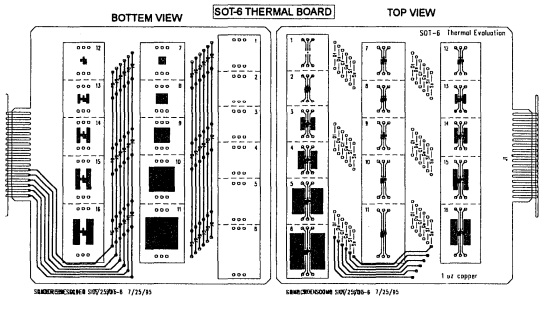


Figure 2. Both Sides of the 4.5"x5" SuperSOT™-6 Thermal Board. Complete scale drawings is shown in section 5.

Layout	2 Oz Copper Mounting Pad Area (in^2)	Relative Placement on Board
1-6	0.003, 0.01, 0.05, 0.1, 0.25, 0.4	Top*
7-11	0.03, 0.06, 0.1, 0.25, 0.4	Bottom*
12-16	0.02, 0.06, 0.1, 0.25, 0.4	1/2 Top and 1/2 Bottom*
1, 2, 5	0.0015, 0.05, 0.125	Top**

Table 1: Thermal Board Configurations.
Note: *Single device, **Dual devices

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to appendix B for details.

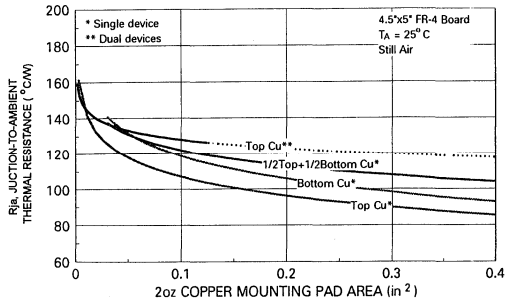


Figure 3. SuperSOT™-6 Junction-to-Ambient thermal resistance versus copper mounting pad area and its surface placement.

Plots in figure 3 show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 160 to 90°C/W in the range from 0.003 to 0.4 square inches for single device. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 10 to 15°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into equation 2.1, the steady-state maximum power dissipation curves can be obtained and are shown in figure 4.

A 10% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.003 to 0.01 in^2, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

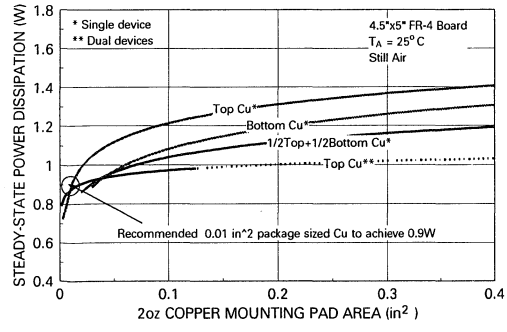


Figure 4. Maximum Power Dissipation Curves for SuperSOT™-6. For single device, layout 2 0.01 in^2 2 Oz copper mounting pad area is recommended to achieve approximately 0.9W.

4. Conclusion

National Semiconductor has attempted to define the thermal performance of the SuperSOT™-6 Power MOSFET, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

1. Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
2. Placement of the copper pads on the top side of the board gives the best thermal performance.
3. The most cost effective approach of designing layout 2 0.01 square inches copper pad directly under the package without occupying additional board space, can increase the maximum power from approximately 0.8 to 0.9W.
4. Maximum thickness of the copper pad should be used for cost performance trade off.

5. Thermal Board Layout

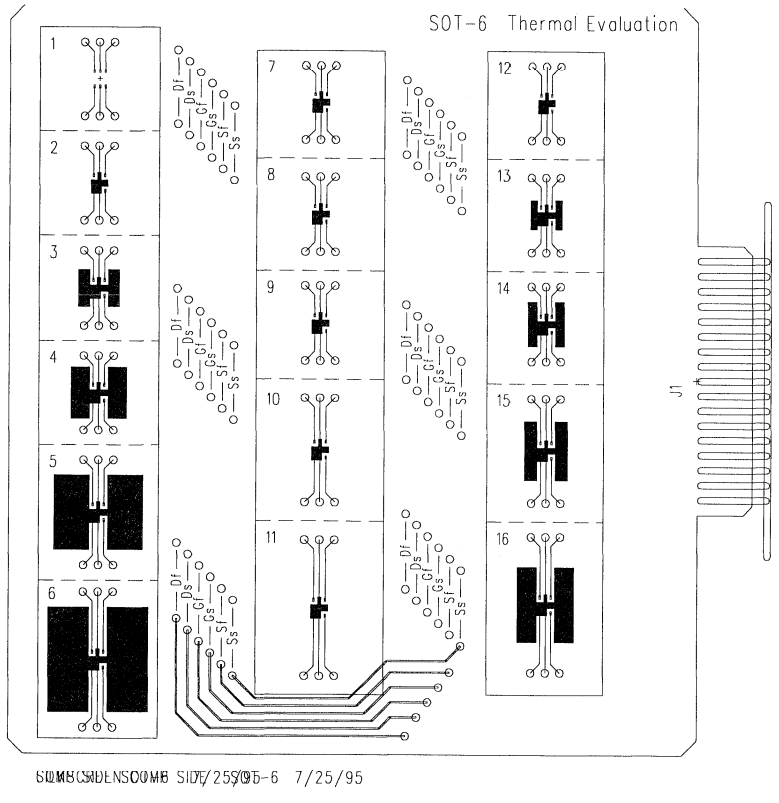


Figure 5. SuperSOT™-6 Thermal Board Top View. Scale 1:1 on letter size paper

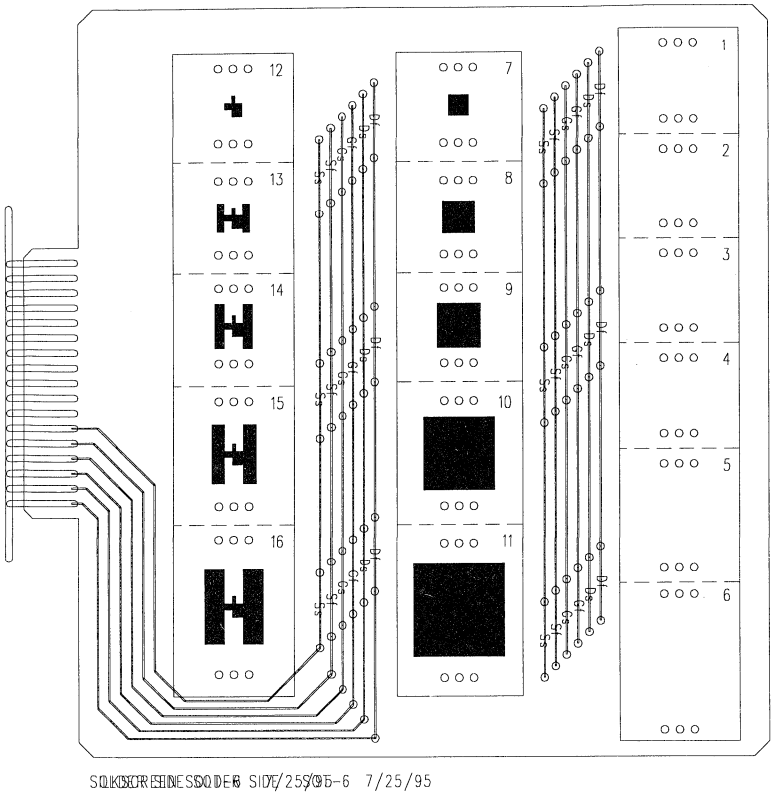


Figure 6. SuperSOT™-6 Thermal Board Bottom View. Scale 1:1 on letter size paper.

Maximum Power Enhancement Techniques for SuperSOT™-8 Power MOSFETs

Alan Li , Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong

1. Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of the SuperSOT™-8 Power MOSFET offered by National Semiconductor. This effort allows the user to take full advantage of the exceptional performance features of National's state-of-the-art Power MOSFET which offers very low on-resistance and improved junction-to-case ($R_{\theta JC}$) thermal resistance. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the drain leads of the Power MOSFET are mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

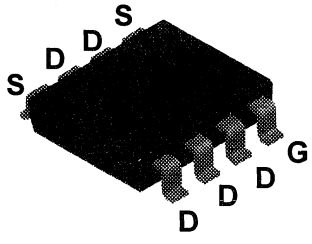


Figure 1. SuperSOT™-8 Power MOSFET achieves junction-to-case thermal resistance $R_{\theta JC}$ of 20°C/W.

2. Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and the junction-to-ambient thermal resistance.

$$P_{Dmax} = (T_{Jmax} - T_A) / R_{\theta JA} \qquad (2.1)$$

The term junction refers to the point of thermal reference of the semiconductor. Equation 2.1 can also be applied to the transient-state:

$$P_{Dmax}(t) = [T_{Jmax} - T_A] / R_{\theta JA}(t) \quad (2.2)$$

where P_{Dmax} (t) and $R_{\theta JA}$(t) are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}$(t) increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details. Nevertheless, National provides a Discrete SPICE Thermal Model (LIT#570240-002) for general thermal evaluation. User may find these models helpful in determining the dynamic power and temperature limits in the application.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and $R_{\theta CA}$ case-to-ambient thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad (2.3)$$

The case thermal reference of the SuperSOT™-8 Power MOSFET is defined as the point of contact between the drain leads of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint. On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

3. Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 Oz copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in figure 2 and table 1. Layouts 1 to 6 have the copper pad sizes from 0.005 to 0.4 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.052 to 0.4 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.052 to 0.4 square inches divided equally on both sides of the board.

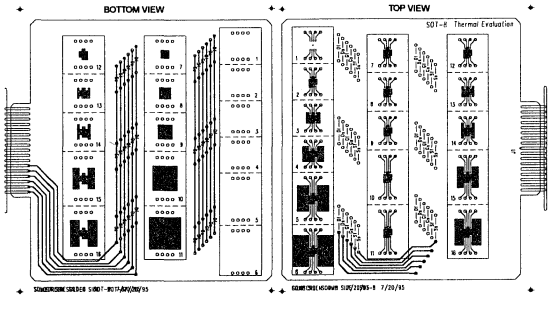


Figure 2. Both Sides of the 4.5"x5" SuperSOT™-8 Thermal Board. Complete scale drawings is shown in section 5.

Layout	2 Oz Copper Mounting Pad Area (in^2)	Relative Placement on Board
1-6	0.005, 0.026, 0.05, 0.1, 0.25, 0.4	Top
7-11	0.052, 0.078, 0.1, 0.25, 0.4	Bottom
12-16	0.052, 0.078, 0.1, 0.25, 0.4	1/2 Top and 1/2 Bottom

Table 1: Thermal Board Configurations.

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to appendix B for details.

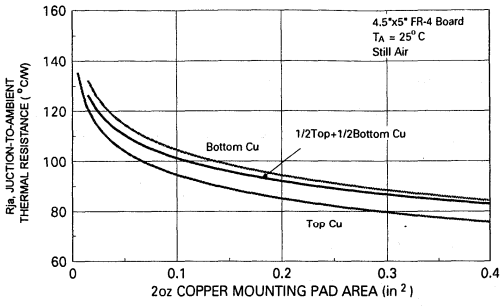


Figure 3. SuperSOT™-8 Junction-to-Ambient thermal resistance versus copper mounting pad area and its surface placement.

Plots in figure 3 show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 135 to 75°C/W in the range from 0.005 to 0.4 square inches for single device. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 3 to 10°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into equation 2.1, the steady-state maximum power dissipation curves can be obtained and are shown in figure 4.

A 20% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.005 to 0.026 in^2, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

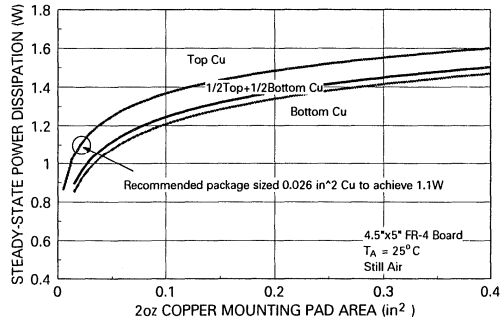


Figure 4. Maximum Power Dissipation Curves for SuperSOT™-8. 0.026 in² 2 Oz copper mounting pad area, layout 2, is recommended to achieve approximately 1.1W.

4. Conclusion

National Semiconductor has attempted to define the thermal performance of the SuperSOT™-8 Power MOSFET, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

1. Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
2. Placement of the copper pads on the top side of the board gives the best thermal performance.
3. The most cost effective approach of designing layout 2 0.026 square inches copper pad directly under the package without occupying additional board space, can increase the maximum power from approximately 0.9 to 1.1W.
4. Maximum thickness of the copper pad should be used for cost performance trade off.

5. Thermal Board Layout

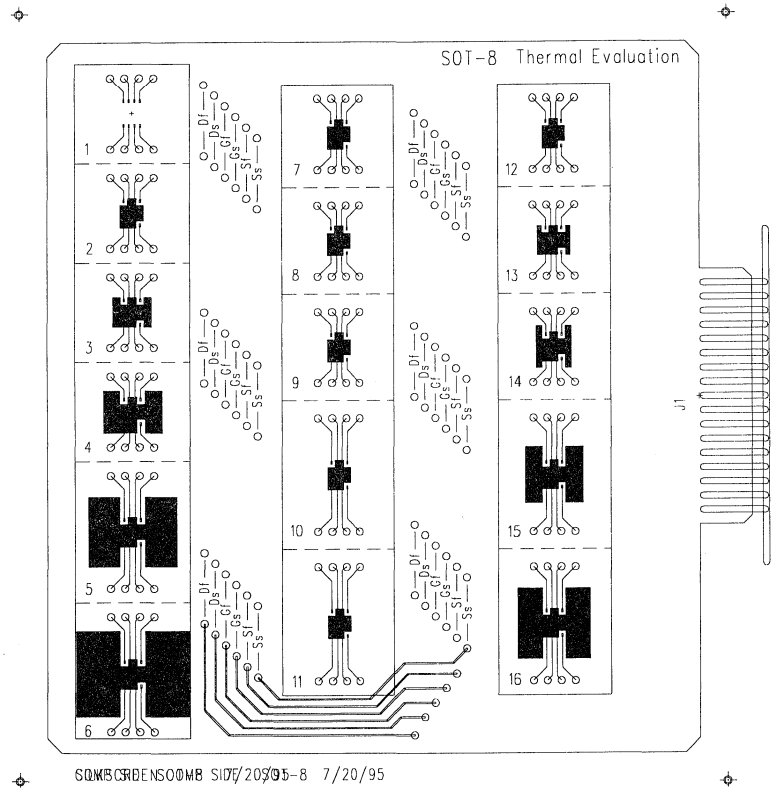


Figure 5. SuperSOT™-8 Thermal Board Top View. Scale 1:1 on letter size paper

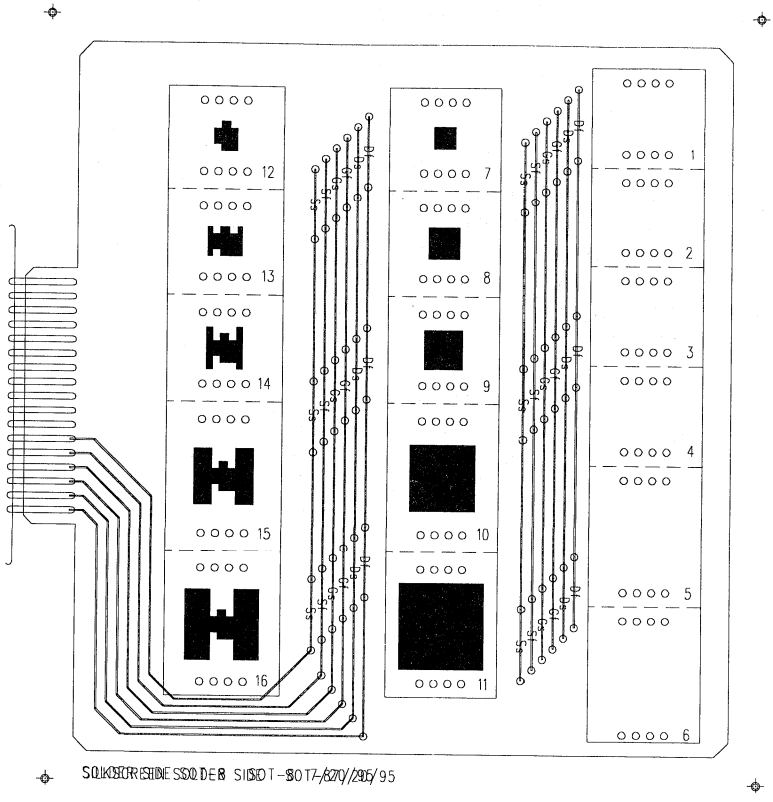


Figure 6. SuperSOT™-8 Thermal Board Bottom View. Scale 1:1 on letter size paper.

Maximum Power Enhancement Techniques for SOT-223 Power MOSFETs

Alan Li , Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong

1. Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of the SOT-223 Power MOSFET offered by National Semiconductor. This effort allows the user to take full advantage of the exceptional performance features of National's state-of-the-art Power MOSFET which offers very low on-resistance and improved junction-to-case ($R_{\theta JC}$) thermal resistance. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the drain leads of the Power MOSFET are mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

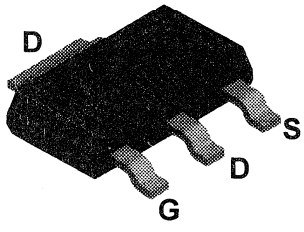


Figure 1. SOT-223 Power MOSFET achieves junction-to-case thermal resistance $R_{\theta JC}$ of 12°C/W.

2. Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and the junction-to-ambient thermal resistance.

$$P_{Dmax} = (T_{Jmax} - T_A) / R_{\theta JA} \qquad (2.1)$$

The term junction refers to the point of thermal reference of the semiconductor. Equation 2.1 can also be applied to the transient-state:

$$P_{Dmax}(t) = [T_{Jmax} - T_A] / R_{\theta JA}(t) \quad (2.2)$$

where P_{Dmax} (t) and $R_{\theta JA}$(t) are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}$(t) increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details. Nevertheless, National provides a Discrete SPICE Thermal Model (LIT#570240-002) for general thermal evaluation. User may find these models helpful in determining the dynamic power and temperature limits in the application.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and $R_{\theta CA}$ case-to-ambient thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad (2.3)$$

The case thermal reference of the SOT-223 Power MOSFET is defined as the point of contact between the drain leads of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint. On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

3. Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 Oz copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in figure 2 and table 1. Layouts 1 to 6 have the copper pad sizes from 0.0123 to 1 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.2 to 1 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.132 to 1 square inches divided equally on both sides of the board.

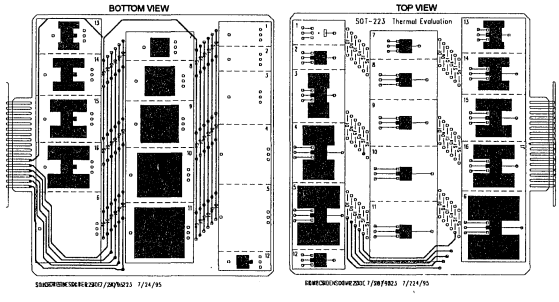


Figure 2. Both Sides of the 4.5"x5" SOT-223 Thermal Board. Complete scale drawings is shown in section 5.

Layout	2 Oz Copper Mounting Pad Area (in^2)	Relative Placement on Board
1-6	0.0123, 0.066, 0.3, 0.53, 0.76, 1	Top
7-11	0.2, 0.4, 0.6, 0.8, 1	Bottom
12-16	0.132, 0.35, 0.568, 0.784, 1	1/2 Top and 1/2 Bottom

Table 1: Thermal Board Configurations.

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to appendix B for details.

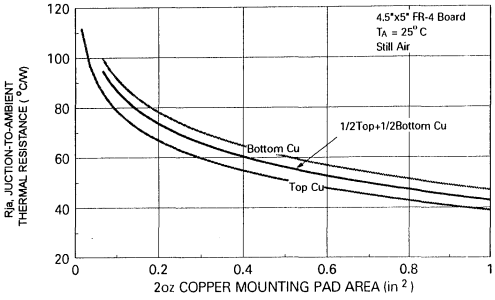


Figure 3. SOT-223 Junction-to-Ambient thermal resistance versus copper mounting pad area and its surface placement.

Plots in figure 3 show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 110 to 40°C/W in the range from 0.0123 to 1 square inches for single device. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 10 to 15°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into equation 2.1, the steady-state maximum power dissipation curves can be obtained and are shown in figure 4.

A 18% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.0123 to 0.066 in^2, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

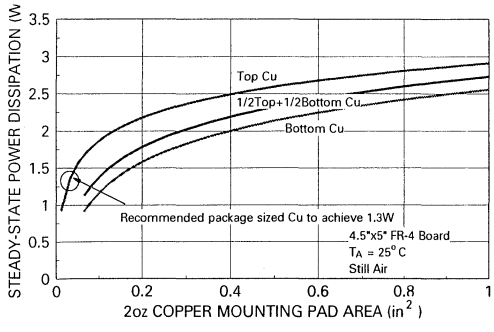


Figure 4. Maximum Power Dissipation Curves for SOT-223. 0.066 in^2 2 Oz copper mounting pad area, layout 2, is recommended to achieve approximately 1.3W.

4. Conclusion

National Semiconductor has attempted to define the thermal performance of the SOT-223 Power MOSFET, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

1. Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
2. Placement of the copper pads on the top side of the board gives the best thermal performance.
3. The most cost effective approach of designing layout 2 0.066 square inches copper pad directly under the package without occupying additional board space, can increase the maximum power from approximately 1.1 to 1.3W.
4. Maximum thickness of the copper pad should be used for cost performance trade off.

5. Thermal Board Layout

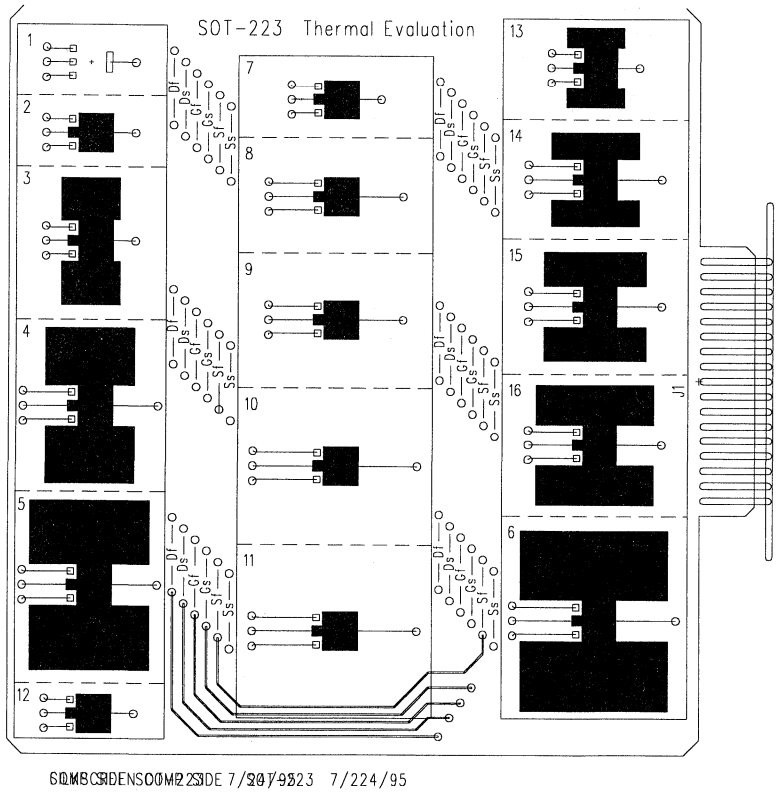


Figure 5. SOT-223 Thermal Board Top View. Scale 1:1 on letter size paper

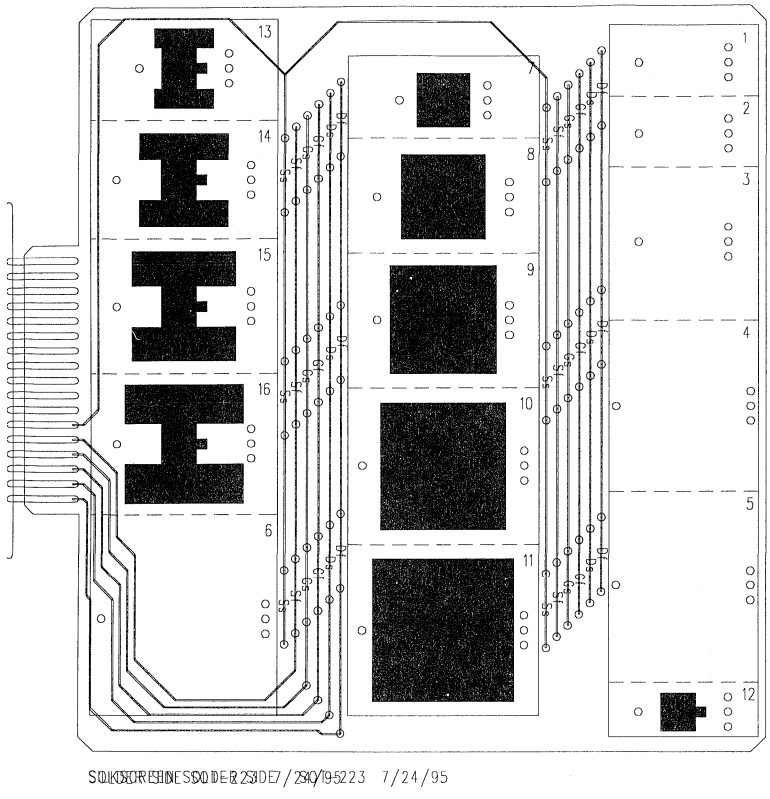


Figure 6. SOT-223 Thermal Board Bottom View. Scale 1:1 on letter size paper.

Maximum Power Enhancement Techniques for SO-8 Power MOSFETs

Alan Li , Brij Mohan, Steve Sapp, Izak Bencuya, Linh Hong

1. Introduction

As packages become smaller, achieving efficient thermal performance for power applications requires that the designers employ new methods of meliorating the heat flow out of devices. Thus the purpose of this paper is to aid the user in maximizing the power handling capability of the SO-8 Power MOSFET offered by National Semiconductor. This effort allows the user to take full advantage of the exceptional performance features of National's state-of-the-art Power MOSFET which offers very low on-resistance and improved junction-to-case ($R_{\theta JC}$) thermal resistance. Ultimately the user may achieve improved component performance and higher circuit board packing density by using the thermal solution suggested below.

In natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the drain leads of the Power MOSFET are mounted directly onto the pad. The pad acts as a heatsink to reduce thermal resistance and leads to improved power performance.

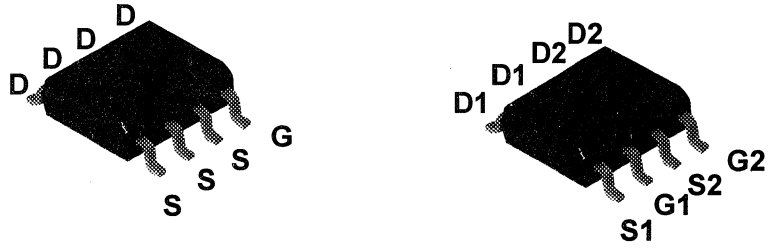


Figure 1. SO-8 Power MOSFET has junction-to-case thermal resistance $R_{\theta JC}$ of 25°C/W for single device and 40°C/W for dual devices.

2. Theory

When a device operates in a system under the steady-state condition, the maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and the junction-to-ambient thermal resistance.

$$P_{Dmax} = (T_{Jmax} - T_A) / R_{\theta JA} \qquad (2.1)$$

The term junction refers to the point of thermal reference of the semiconductor. Equation 2.1 can also be applied to the transient-state:

$$P_{Dmax}(t) = [T_{Jmax} - T_A] / R_{\theta JA}(t) \quad (2.2)$$

where P_{Dmax} (t) and $R_{\theta JA}(t)$ are time dependent. By using the transient thermal resistance curves shown in the data sheet, a transient temperature change can be calculated. The transient thermal behavior is a complicated subject because $R_{\theta JA}(t)$ increases non-linearly with time and the conditions of the power pulse. A more thorough treatment of transient power analysis is beyond the scope of this document and the reader can refer to [13] for details. Nevertheless, National provides a Discrete SPICE Thermal Model (LIT#570240-002) for general thermal evaluation. User may find these models helpful in determining the dynamic power and temperature limits in the application.

$R_{\theta JA}$ has two distinct elements, $R_{\theta JC}$ junction-to-case and $R_{\theta CA}$ case-to-ambient thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA} \qquad (2.3)$$

The case thermal reference of the SO-8 Power MOSFET is defined as the point of contact between the drain leads of the package and the mounting surface.

$R_{\theta CA}$ is influenced by many variables such as ambient temperature, board layout, and cooling method. Due to the lack of an industry standard, the value of $R_{\theta CA}$ is not easily defined and can affect $R_{\theta JA}$ significantly. In addition, the case reference may be defined differently by various manufacturers. Under such conditions, it becomes difficult to define $R_{\theta CA}$ from the component manufacturer standpoint. On the other hand, $R_{\theta JC}$ is independent of users' conditions and can be accurately measured by the component manufacturer.

Therefore, in this paper an effort has been made to define a procedure which can be used to quantify the junction-to-ambient thermal resistance $R_{\theta JA}$ which is more useful to the circuit board designer.

3. Result

The scope of the investigation has been limited to the size of copper mounting pad and its relative surface placement on the board. In still air with no heatsink, the application of these heat dissipation methods is the most cost effective thermal solution. A total of sixteen different combinations of 2 Oz copper pad sizes and their placement were designed to study their influence on $R_{\theta JA}$ thermal resistance. The configurations of the board layout are shown in figure 2 and table 1. For single device, layouts 1 to 6 have the copper pad sizes from 0.006 to 1 square inches on the top side of the board (top side is defined as the component side of the board). Layouts 7 to 11 have copper pad sizes from 0.12 to 1 square inches on the bottom side of the board. Layouts 12 to 16 have copper pad sizes from 0.08 to 1 square inches divided equally on both sides of the board. For dual devices, layouts 1 to 6 have copper sizes from 0.003 to 0.5 sqaure inches on the top side of the board.

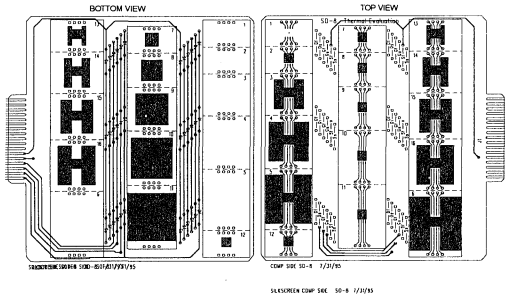


Figure 2. Both Sides of the 4.5"x5" SO-8 Thermal Board. Complete scale drawings is shown in section 5.

Layout	2 Oz Copper Mounting Pad Area (in^2)	Relative Placement on Board
1-6	0.006, 0.04, 0.28, 0.52, 0.76, 1	Top*
7-11	0.12, 0.22, 0.48, 0.74, 1	Bottom*
12-16	0.08, 0.22, 0.48, 0.74, 1	1/2 Top and 1/2 Bottom*
1-6	0.003, 0.02, 0.14, 0.26, 0.38, 0.5	Top**

Table 1: Thermal Board Configurations.
Note: *Single device, **Dual devices

$R_{\theta JA}$ was calculated from the relationship between power and the change of junction temperature. If readers are interested in the test conditions and method, they are encouraged to refer to appendix B for details.

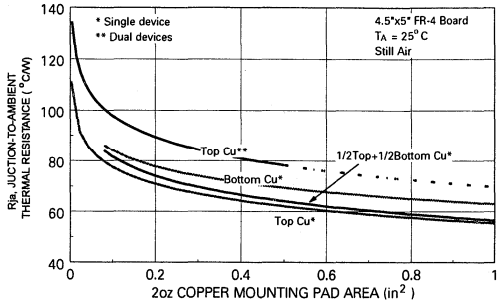


Figure 3. SO-8 Junction-to-Ambient thermal resistance versus copper mounting pad area and its surface placement.

Plots in figure 3 show the relationship of $R_{\theta JA}$ versus the copper mounting pad area and its surface placement on the board. It is apparent that increasing copper mounting pad area considerably lowers $R_{\theta JA}$ from approximately 120 to 50°C/W in the range from 0.006 to 1 square inches for single device. In addition, placing all the copper on the top side of the board further reduces $R_{\theta JA}$ by 5 to 10°C/W when compared with the other two placements.

By substituting the thermal resistance, ambient temperature, and the maximum junction temperature rating into equation 2.1, the steady-state maximum power dissipation curves can be obtained and are shown in figure 4.

A 20% increase in the power handling can be achieved by increasing the copper pad area on top of the board from 0.006 to 0.04 in^2, layout 2. This thermal pad fits directly under the package, so that no additional board space is required. For maximum performance, it is recommended to put extra copper on the bottom of the board connected to the top pad by through-hole thermal vias.

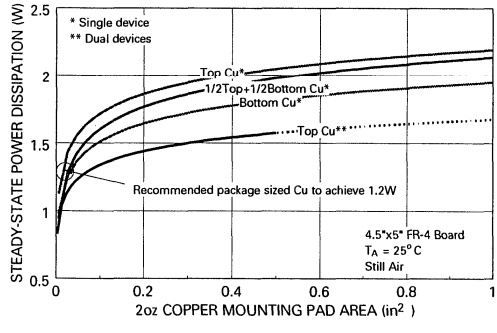


Figure 4. Maximum Power Dissipation Curves for SO-8. For single device, layout 2 0.04 in^2 2 Oz copper mounting pad area is recommended to achieve approximately 1.2W. For dual devices, 0.02 in^2 is recommended to achieve approximately 1W.

4. Conclusion

National Semiconductor has attempted to define the thermal performance of the SO-8 Power MOSFET, from a systems point of view. It has been demonstrated that significant thermal improvement can be achieved in the maximum power dissipation through the proper design of copper mounting pads on the circuit board. The results can be summarized as follows:

1. Enlarged copper mounting pads, on either one or both sides of the board, are effective in reducing the case-to-ambient thermal resistance $R_{\theta CA}$.
2. Placement of the copper pads on the top side of the board gives the best thermal performance.
3. For single device, the most cost effective approach of designing layout 2 0.04 square inches copper pad directly under the package without occupying additional board space, can increase the maximum power from approximately 1 to 1.2W. For dual devices, 0.02 square inches copper pad can increase power from 0.9 to 1W.
4. Maximum thickness of the copper pad should be used for cost performance trade off.

5. Thermal Board Layout

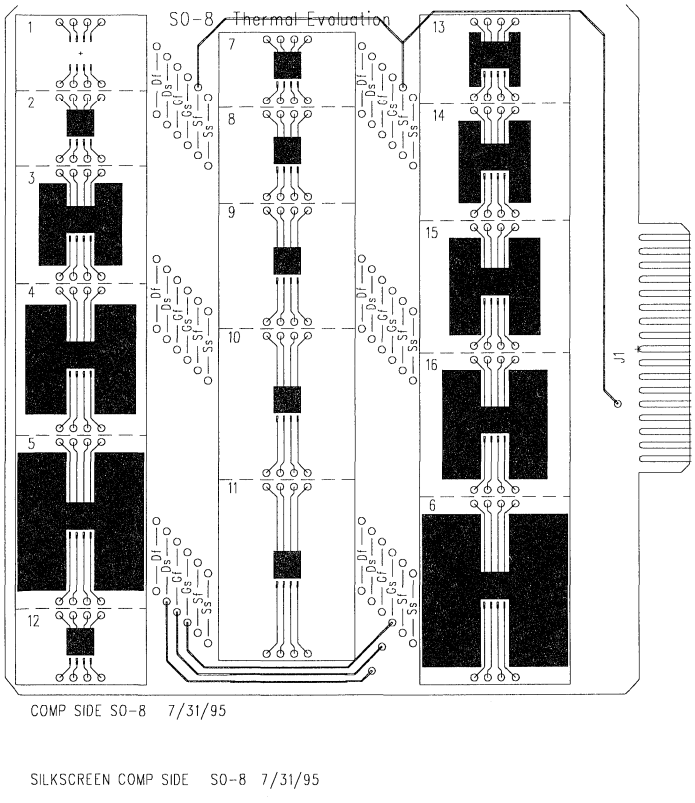


Figure 5. SO-8 Single Device Thermal Board Top View. Scale 1:1 on letter size paper

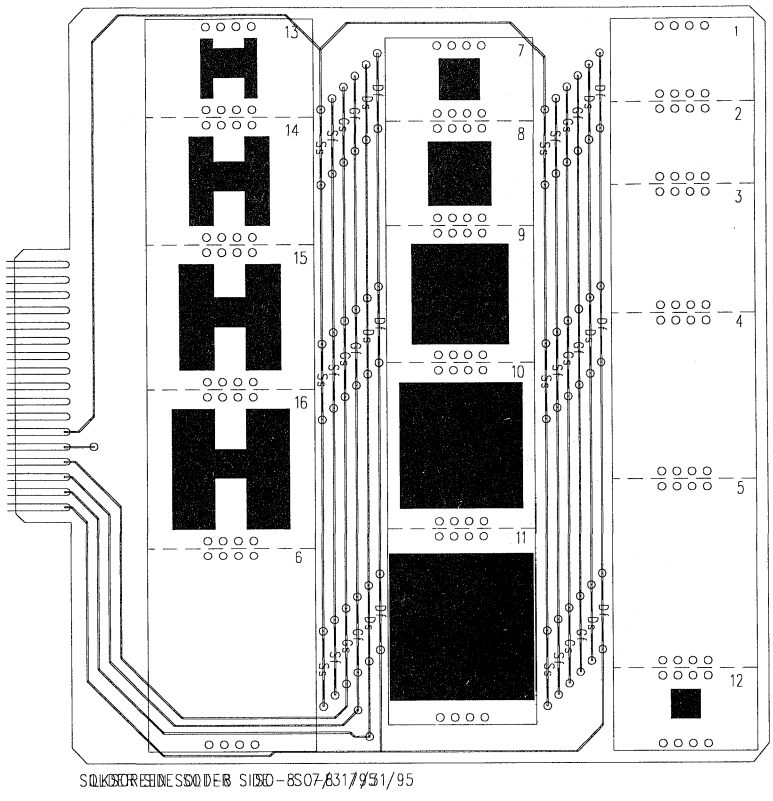


Figure 6. SO-8 Single Device Thermal Board Bottom View. Scale 1:1 on letter size paper.

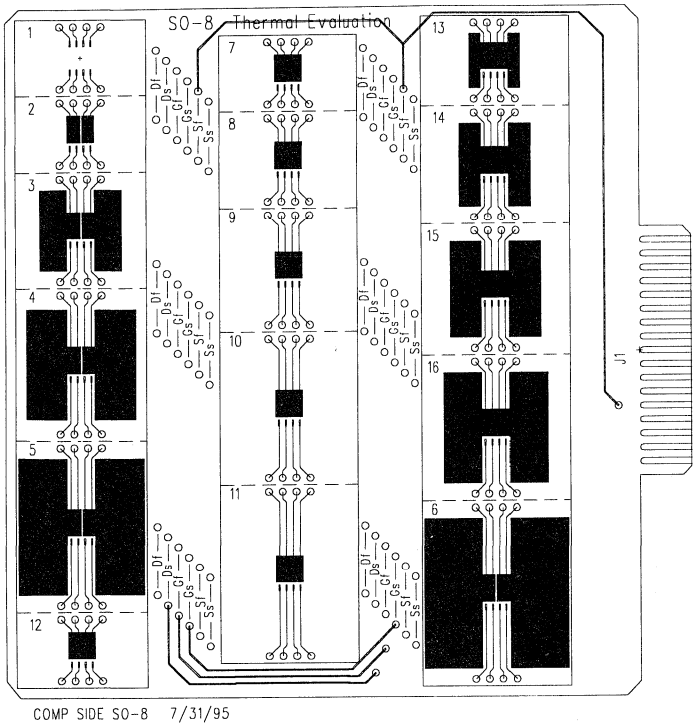
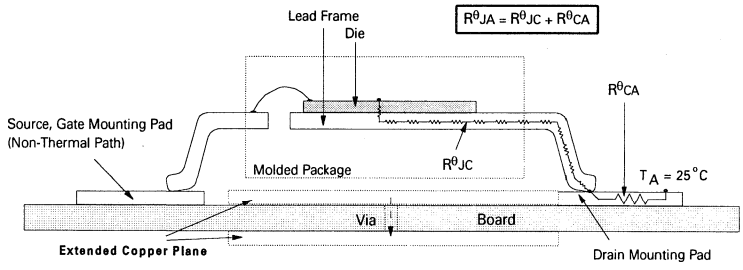


Figure 7. SO-8 Dual Device Thermal Board Top View. Scale 1:1 on letter size paper. Note only layouts 1 to 6 are used for thermal characterization.

Appendix A

Heat Flow Theory Applied to Power MOSFET

When a Power MOSFET operates with an appreciable current, its junction temperature is elevated. It is important to quantify its thermal limits in order to achieve acceptable performance and reliability. This limit is determined by summing the individual parts consisting of a series of temperature rises from the semiconductor junction to the operating environment. A one dimensional steady-state model of conduction heat transfer is demonstrated in figure 1. The heat generated at the device junction flows through the die to the die attach pad, through the lead frame to the surrounding case material, to the printed circuit board, and eventually to the ambient environment. There are also secondary heat paths. One is from the package to the ambient air. The other is from the drain lead frame to the detached source and gate leads then to the printed circuit board. These secondary heat paths are assumed to be negligible contributors to the heat flow in this analysis.



$R^{\theta}JC$ (Component Variables)

- Leadframe Size & Material
- No. of Conduction Pins
- Die Size
- Die Attach Material
- Molding Compound Size & Material

$R^{\theta}CA$ (Applications Variables)

- Mounting Pad Size, Material, & Location
- Placement of Mounting Pad
- PCB Size & Material
- Traces Length & Width
- Adjacent Heat Sources
- Volume of Air
- Air Flow
- Ambient Temperature
- Shape of Mounting Pad

Figure 1: Cross-sectional view of a Power MOSFET mounted on a printed circuit board. Note that the case temperature is measured at the point where the drain lead(s) contact with the mounting pad surface.

The increase of junction temperature above the surrounding environment is directly proportional to dissipated power and the thermal resistance. The steady-state junction-to-ambient thermal resistance, $R_{\theta JA}$, is defined as

$$R_{\theta JA} = (T_J - T_A) / P$$

where T_J is the average temperature of the device junction. The term junction refers to the point of thermal reference of the semiconductor device. T_A is the average temperature of the ambient environment. P is the power applied to the device which changes the junction temperature.

$R_{\theta JA}$ is a function of the junction-to-case $R_{\theta JC}$ and case-to-ambient $R_{\theta CA}$ thermal resistance

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where the case of a Power MOSFET is defined at the point of contact between the drain lead(s) and the mounting pad surface. $R_{\theta JC}$ can be controlled and measured by the component manufacturer independent of the application and mounting method and is therefore the best means of comparing various suppliers component specifications for thermal performance. On the other hand, it is difficult to quantify $R_{\theta CA}$ due to heavy dependence on the application. Before using the data sheet thermal data, user should always be aware of the test conditions and justify the compatibility in the application.

Appendix B

Thermal Measurement

Prior to any thermal measurement, a K factor must be determined. It is a linear factor related to the change of intrinsic diode voltage with respect to the change of junction temperature. From the slope of the curve shown in figure 2, K factor can be determined. It is approximately 2.2mV/°C for most Power MOSFET devices.

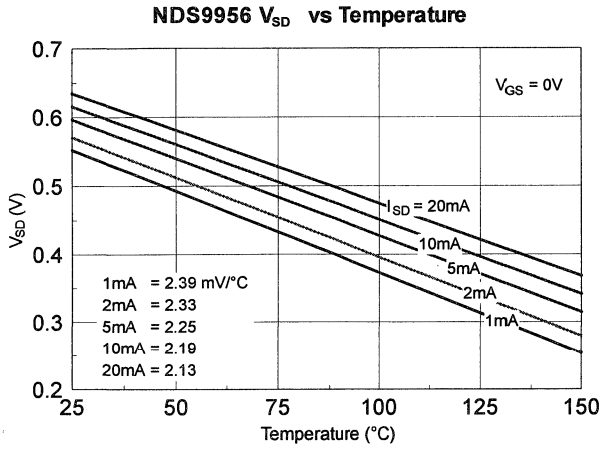


Figure 2. K factors, slopes of a V_{SD} vs temperature curves, of a typical Power MOSFET

After the K factor calibration, the drain-source diode voltage of the device is measured prior to any heating. A pulse is then applied to the device and the drain-source diode voltage is measured 30us following the end of the power pulse. From the change of the drain-source diode voltage, the K factor, input power, and the reference temperature, the time dependent single pulsed junction-to-reference thermal resistance can be calculated. From the single pulse curve on figure 3, duty cycle curves can be determined. Note: a curve set in which $R_{\theta JA}$ is specified indicates that the part was characterized using the ambient as the thermal reference. The board layout specified in the data sheet notes will help determine the applicability of the curve set.

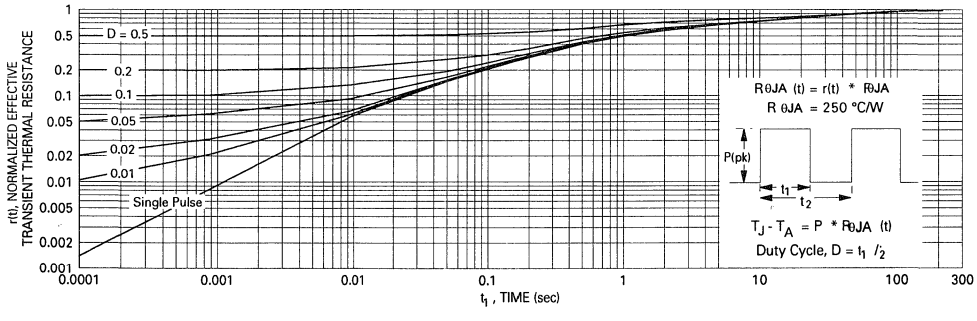


Figure 3. Normalized Transient Thermal Resistance Curves

B.1 Junction-to-Ambient Thermal Resistance Measurement

Equipment and Setup:

- Tesec DV240 Thermal Tester
- 1 cubic foot still air environment
- Thermal Test Board with 16 layouts defined by the size of the copper mounting pad and their relative surface placement. For layouts with copper on the top and bottom planes, there are 0.02 inch copper plated vias (heat pipes) connecting the two planes. See figure 2 and table 1 on the thermal application note for board layout and description. The conductivity of the FR-4 PCB used is 0.29 W/m-C. The length is 5.00 inches ± 0.005; width 4.50 inches ± 0.005; and thickness 0.062 inches ± 0.005. 2Oz copper clad PCB.

The junction-to-ambient thermal measurement was conducted in accordance with the requirements of MIL-STD-883 and MIL-STD-750 with the exception of using 2 Oz copper and measuring diode current at 10mA.

A test device is soldered on the thermal test board with minimum soldering. The copper mounting pad reaches the remote connection points through fine traces. Jumpers are used to bridge to the edge card connector. The fine traces and jumpers do not contribute significant thermal dissipation but serve the purpose of electrical connections. Using the intrinsic diode voltage measurement described above, the junction-to-ambient thermal resistance can be calculated.

B.2 Junction-to-Case Thermal Resistance Measurement

Equipment and Setup:

- Tesec DV240 Thermal Tester
- large aluminum heat sink
- type-K thermocouple with FLUKE 52 K/J Thermometer

The drain lead(s) is soldered on a 0.5 x 1.5 x 0.05 copper plate. The plate is mechanically clamped to a heat sink which is large enough to be considered ideal. Thermal grease is applied in-between the two planes to provide good thermal contact. Theoretically the case temperature should be held constant regardless of the conditions. Thus a thermocouple is used and fixed at the point of contact between the drain lead(s) and the copper plate surface, to account for any heatsink temperature change. Using the intrinsic diode voltage measurement described earlier, the junction-to-case thermal resistance can be obtained. A plot of junction-to-case thermal resistance for various packages is shown in figure 4. Note $R_{\theta JC}$ can vary with die size and the effect is more prominent as $R_{\theta JC}$ decreases.

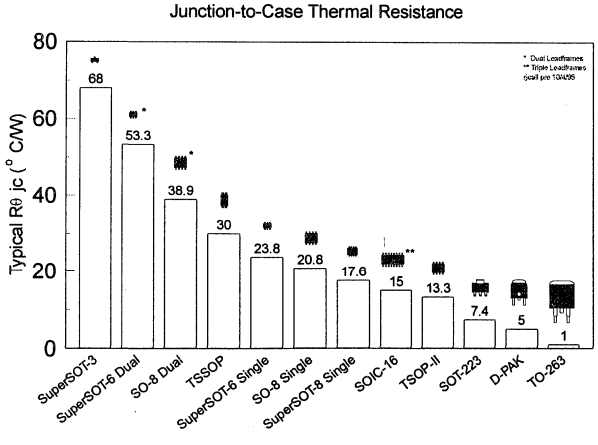


Figure 4. Junction-to-case thermal resistance $R_{\theta JC}$ of various surface mount Power MOSFET packages.

References

[1] K. Azar, S.S. Pan, J. Parry, H. Rosten, "Effect of Circuit Board Parameters on Thermal Performance of Electronic Components in Natural Convection Cooling," IEEE 10th annual Semi-Therm Conference, Feb. 1994.

[2] A. Bar-Cohen, & A.D. Krauss, "Advances in Thermal Modeling of Electronic Components & Systems," Vol 1, Hemisphere Publishing, Washington, D.C., 1988.

[3] R.T. Bilson, M.R. Hepher, J.P. McCarthy, "The Impact of Surface Mounted Chip Carrier Packaging on Thermal Management in Hybrid Microcircuit," Thermal Management Concepts in Microelectronics Packaging, International Society for Hybrid Microelectronics, 1984.

[4] R.A. Brewster, R.A. Sherif, "Thermal Analysis of A Substrate with Power Dissipation in the Vias," IEEE 8th Annual Semi-Therm Conf., Austin, Tx , Feb. 1992.

[5] D. Edwards, "Thermal Enhancement of IC Packages, " IEEE 10th Annual Semi-Therm Conf., San Jose, Ca, Feb. 1994.

[6] S.S. Furkay, "Convective Heat Transfer in Electronic Equipment: An Overview," Thermal Management Concepts, 1984.

[7] C. Harper, Electronic Packaging & Interconnection Handbook, McGraw-Hill, NY, 1991, Ch. 2.

[8] Y.M. Kasem, R.K. Williams, "Thermal Design Principles and Characterization of Miniaturized Surface-Mount Packages for Power Electronics," IEEE 10th annual Semi-Therm Conf., San Jose, Ca, Feb. 1994.

[9] V. Manno, N.R. Kurita, K. Azar, "Experimental Characterization of Board Conduction Effect," IEEE 9th Annual Semi-Therm Conf., 1993.

[10] J.W. Sofia, "Analysis of Thermal Transient Data with Synthesized Dynamic Models for Semiconductor Devices," IEEE 10th Annual Semi-Therm Conf., San Jose, Ca, Feb. 1994.

[11] G.R. Wagner, "Circuit Board Material/Construction and its Effect on Thermal Management," Thermal Management Concepts, 1984.

[12] M. Wills, "Thermal Analysis of Air-Cooled Cbs," Electron Prod., pp. 11-18, May 1983.

[13] Motorola Application Note AN-569.

Section 10

Quality and Reliability Assurance

Quality and Reliability Assurance

QUALITY

Most discrete products from National Semiconductor are available in two forms:

1) Industrial / Commercial identified by a standard part number having various commonly-known prefixes and tested to a published National Semiconductor, JEDEC, Proelectron or other specification.

2) Customer-specific identified by an assigned "stamp-off" number, and tested and marked as determined by the customer for their specific requirements. This may range from a custom-marked industrial/commercial part to product meeting various additional/ special electrical needs specified at -40 and 125 °C.

Device lots are subjected to 100% processing at final test to the datasheet or other applicable electrical specifications reflected on internal documentation. All products are then transferred to QA where they are subjected to sample electrical testing, usually to the same electrical specifications, and additional mechanical inspection requirements.

RELIABILITY

Discrete Power & Signal Technologies utilizes two programs to insure reliability performance of various products delivered to our customers. They are the **1) Reliability Qualification Program** for new product and product manufacturing variations/locations, and the **2) Reliability Audit Program** applicable to existing qualified products, with the goal of continuous improvement.

Reliability Qualification Program

A standard procedure was developed and put in place defining the reliability requirements for product qualification. Tests used are indicated in **Table 1.** The scope includes all new products, products from new manufacturing facilities, changes in manufacturing locations, and major engineering changes on existing products. Major changes may include, but are not limited to:

- New product -- either in a new device design, new package design, or new fab technology
- New assembly location -- new assembly subcontractor, vendor, product transfer site
- Major process changes -- wafer fabrication process, manufacturing assembly process
- Package -- new or change in package design such as mold compound formulation
- Lead frames -- change in material composition, design, trim and form process
- Die layout / recipe -- wafer fabrication (i.e., new mask), epitaxy layer
- Fab location -- new fabrication site, new wafer vendor

Tests	Conditions	Timepoints	Sample Size
Autoclave (ACLV)	15 PSIG, 121°C	96, 168 Hours	77
High Temperature Storage Life (HTSL)	T_A = 150°C	168, 500, 1K Hours	77
High Temperature Reverse Bias (HTRB)	T_A = 150°C	168, 500, 1K Hours	77
High Temperature Gate Bias (HTGB)	T_A = 150°C	168, 500, 1K Hours	77
Temperature Humidity Bias (THBT)	T_A = 150°C RH = 85%	168, 500, 1K Hours	77
Power Cycle (PRCL)	ΔT_J = 150°C	5K, 10K Cycles	77
Temperature Cycle (TMCL)	T_A = -65 to +150°C	100, 500 Cycles	77

Table 1: RELIABILITY REQUIREMENTS FOR DISCRETE SEMICONDUCTOR DEVICES

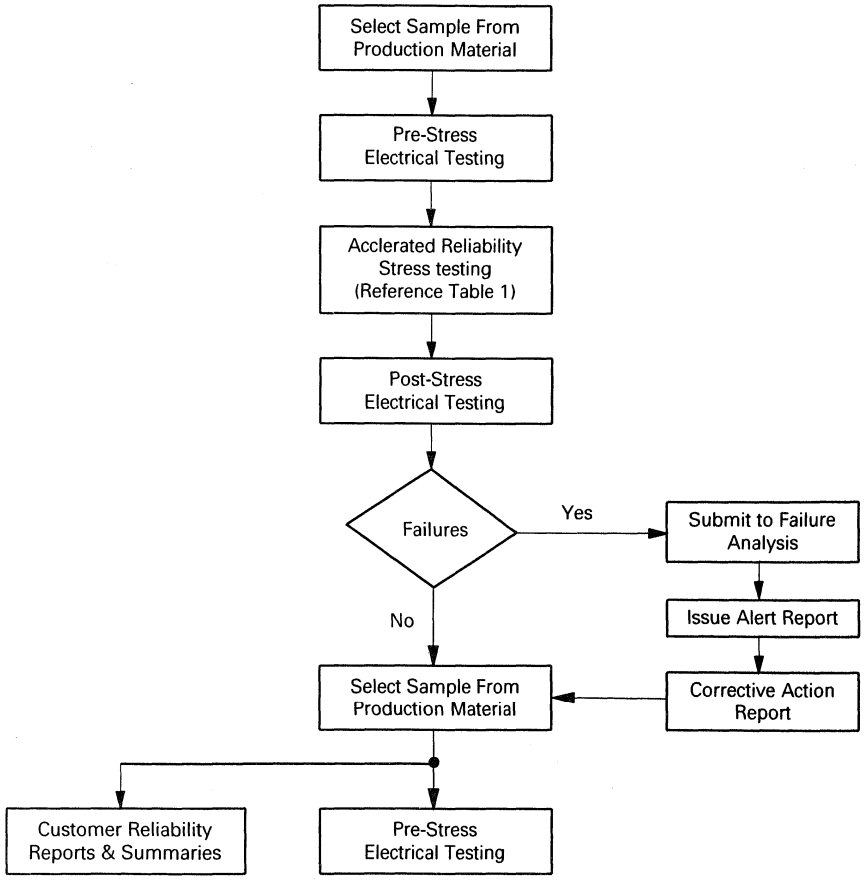


Figure 1: RELIABILITY ASSURANCE AUDIT PROGRAM TEST FLOW

Reliability Audit Program

Existing Products are evaluated on a routine basis to insure the reliability performance of products delivered to our valued customers. Two audit programs are in place to meet our customer reliability performance requirements. These include a **Fast Reaction Program** and a **Long Term Audit Program.** Both programs are tested per a generic family basis. The FRP refers to evaluating products at 48-168hr reliability stress tests while LTA refers to continued stress testing of products to 100hrs or equivalent duration. Tests used are listed in **Table 1.**

Examples of generic families would include: package iterations wherein the manufacturing process is benign to the die inside, type of die topography (overlay, non-overlay, MOS, etc.), primary polarity alignment, die recipe depths and concentrations, target BVs, etc. At any time, there is at least one iteration of each generic family designation in production undergoing long term reliability testing. Criteria includes pre- and postcomparisons of parametric distribution shapes in addition to GNG limits.

RELIABILITY VIS-A-VIS QUALITY

The words "reliability" and "quality" are often used interchangeably, as though they connote identical facets of a product's merit. However, reliability and quality are different, and discrete component users must understand the essential difference between the two concepts in order to properly evaluate the various vendors' programs for product integrity.

The concept of quality gives us information about the population of faulty components among good components, and generally relates to the number of faulty components that arrive at a user's facility. Viewed in another way, quality can instead relate to the number of faulty components that escape detection at the component vendor's facility.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty components that escape detection. QC does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) determines the stringency of the sampling. As the AQL decreases, it becomes more difficult for bad parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given time period.

QUALITY IMPROVEMENT

When purchasing a component or a system, it is expected that each item delivered has been thoroughly tested and will perform according to datasheet or detailed specifications.

Additional programs can be implemented to improve quality. To be effective, a program must not only reduce escapes but also be tailored specifically to detect and remove the types of residual defects that are predicated by process and line monitor control data. The proper analysis and application of this data is a primary objective at National. With emphasis on "ship-to-stock" programs and the need to measure quality levels in ppm's, National Semiconductor has taken a leadership role in an on-going effort to strive for "zero defects."

In Discretes, the benefits derived as a result of this increased emphasis includes the following:

- Escapes caused by mishandling are reduced significantly.
- Residual thermo-mechanical defects not detected during normal room temperature testing or high temperatures buy-off are removed.
- Anomalous high temperature parametric effects that may have been created during wafer fabrication or in subsequent manufacturing are removed.
- An AQL of 0.05% is guaranteed.

RELIABILITY THROUGH DESIGN

With increased component density in modern electronic products has come an increased concern with component failures in such products. Virtually all equipment manufacturers thoroughly exercise their products before shipment. This is designed to stimulate, as closely as possible, field operating conditions. A high failure rate of discrete components at this level can dramatically increase manufacturing costs.

The most important factor affecting a component's reliability is its construction; i.e., the materials used and the method by which they are fabricated and assembled.

ON-GOING RELIABILITY IMPROVEMENT PROBLEM

Transistor reliability improvement at National Semiconductor is a continuous program.

Implementation of a program for field reliability improvement requires knowledge of field ambient and electrical environments and their influence on device performance. National's broad experience in commercial reliability programs has led to the development of an extensive in-house reliability monitoring program that permits us to monitor device performance under combinations of the following stresses:

- Thermal
- Thermo-Mechanical
- Mechanical
- Voltage
- Humidity

The data generated by these monitors is continually ranked and analyzed to determine appropriate corrective action necessary for any failure mechanisms noted. Rigorous analysis of SPC data that is routinely generated at critical stages of the fabrication and manufacturing process is integrated into the corrective actions loop. This continuous cycle of testing, analysis and corrective action assures the continued improvement of transistor field reliability.

Test Descriptions

The following tests are fequently used for screening, acceptance and evaluation of semiconductor devices.

A. Steady State Operating Life (SSOL or OPL)
The purpose of this test is to evaluate the bulk stability of the die and to generate defects resulting from manufacturing aberrations that are manifested as time and stress-dependent failures.

Conditions: T_A = 25°C, PD = max rated power

B. Intermittent Operating Life (IOPL or PRCL)
Sometimes referred to as the "power cycle." The purpose of this test is the same as Operating Life in addition to checking the integrity of both wire and die bonds by means of thermal stressing.

Conditions: T_A = 25°C, PD as required to obtain a specified Dtemperature

C. High Temperature Storage Life (HTS)
The purpose of this test is to generate time/temperature failure mechanisms and to evaluate long-term storage stability.

Conditions: T_A = 150°C, no bias applied

D. High Temperature Reverse Bias (HTRB)
The purpose of this test is to align mobile ions by means of temperature and voltage stresses to form a high-current leakage path between two or more terminals.

Conditions: T_A = 150°C, V_{CB} = 80% max rated V_{CB}

E. Temperature Humidity Bias (THBT)
The purpose of this test is to evaluate the moisture resistance of non-hermetic components. The addition of voltage bias accelerates the corrosive effect after moisture penetration has taken place. With time, this is a catastrophically destructive test.

Conditions: T_A = 150°C, RH = 85%

F. High Temperature High Humidity, High Reverse Bias (H3TRB)
This is an accelerated test. It's effect is to evaluate the individual items related to HTRB and various forms of moisture-resistance testing simultaneously. With time, this is a catastrophically destructive test.

Conditions: T_A = 150°C, RH = 85%, V_{CB} = 80% max rated V_{CB}

G. Autoclave (ACLV)
Sometimes referred to as "pressure cooker," the purpose of this test is to evaluate the moisture resistance of non-hermetic components under pressure/temperature conditions.

Conditions: T_A = 121°C, P = 1 atmosphere (15 psig)

H. Temperature Cycle Air-to-Air (TMCL)
The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and the transition between temperature extremes, and to expose excessive thermal mismatch between materials.

Conditions: Mil-Std-750, Method 1051, -65°C to 150°C, 15 seconds dwell time at each temperature

I. Thermal Shock Liquid-to-Liquid (THSK)
This test is an accelerated version of temperature cycle.

Conditions: Mil-Std-750, Method 1056, -0°C to 100°C, 15 seconds dwell time at each temperature

J. Terminal Strength
The purpose of this test is to evaluate the ability of the device terminals to withstand the lead forming and tension associated with component installation into a circuit.

Conditions: Mil-Std-750, Method 2036, Condition E

K. Solderability
The purpose of this test is to determine the solderability of the device terminals.

Conditions: Mil-Std-750, Method 2026

L. Salt Atmosphere (Corrosion)
The purpose of this test is to accelerate the corrosion effects of an environment in which salt (NaCl) is present.

Conditions: Mil-Std-750, Method 1041

M. Mechanical Stress Test
Vibration, shock and constant acceleration tests are infrequently used since they rarely generate failures in small-signal transistors. However, they are still specified for acceptance of military product.

Glossary of Quality and Reliability Terms

Acceptance Quality Level (AQL) - A measure of quality for which a given lot will be accepted most of the time. This is usually established at a probability of acceptance equal to 95%.

Acceptance Number (Ac) - The largest number of defectives in an inspection sample under consideration that will permit acceptance of the lot.

Average Outgoing Quality (AOQ) - The average quality of outgoing product after 100% screening of rejected lots. This is usually measured in parts per million (PPM)

Average Outgoing Quality Limit (AOQL) - The maximum average outgoing quality that is possible for a given sampling plan.

Defect - Any deviation of a device that does not conform to specified requirements.

Defective - Any device which contains one or more defects.

Double Sampling - Sampling inspection in which the inspection of the first sample leads to a decision to accept, to reject, or to take a second sample. The inspection of a second sample, when required, always leads to a decision to accept or to reject.

Failure - The inability of a device to perform a specified function within previously-established limits.

Failure Rate - The statistical probability of a failure occurring within a stated period of time. The failure rate of semiconductor devices is generally given in percent per thousand hours.

Infant Mortality - Premature failures occurring at a failure rate substantially greater than that observed during subsequent life prior to wear-out.

Lot - A group of devices from which samples are drawn and inspected to determine compliance with acceptance criteria (inspection lot).

Lot Tolerance Percent Defective (LTPD) - A measure of quality for which a given lot will be rejected most of the time. A single lot sampling concept that statistically ensures rejection of 90% of all lots having a greater percent defective than the specified LPTD.

Mean Time Between Failures (MTBF) - The average number of total unit operating hours after a device has failed that would occur before the next device failure would be expected to occur.

Operating Characteristic Curve (OC curve) - A graph of the probability of acceptance as a function of the lot quality or process average quality, whichever is applicable.

Percent Defective - The number of defective devices in a lot divided by the total number of devices in that lot, multiplied by 100.

Probability of Acceptance (Pa) - The fractional probability that a lot will be accepted, usually expressed as a decimal.

Process Average Quality - The expected quality of product from a given process, usually estimated from first sample results of previous inspection lots.

Quality - A measure of the degree to which a product conforms to specification and workmanship requirements.

Rejection Number (Re) - The smallest number of defectives in an inspection sample under consideration that will prevent acceptance of the lot.

Reliability - A measure of the performance of a product over a specified period of time.

Sample - One or more devices selected at random from an inspection lot to represent that lot for acceptance purposes.

Sampling Plan - A specific plan which defines the sample size and the criteria for accepting or rejecting a lot.

Screening Tests - Tests employing nondestructive environmental, electrical, thermal and/or mechanical stresses, for the purpose of identifying anomalous devices.

Single Sampling - Sampling inspection in which a decision to accept or reject is reached after the inspection of a single sample.

Wearout Failures - Those failures which occur as a result of normal deterioration processes.

100% Inspection - Inspection of every device, in which each device is accepted or rejected individually for the characteristic concerned.

Section 11

Ordering Information

Ordering Information for Discrete Products

The Discrete Division "*Discrete POWER and Signal Technologies*" offers 3 product families. They are: **Diodes, Transistors** and **DMOS**. These families can be purchased in bulk or tape and reel/ammo packaging. We offer the most popular style of packaging for each family of products as "standard". A variety of non-standard options are also available. You will find each of these options outlined in the flow code section.

The flow codes listed in this table are specially selected as the most popular. Please contact your nearest National Semiconductor representative when ordering devices with "flow codes."

DMOS products are available in surface mount and through hole packaging. All our surface mount packages come standard as tape and reel. Our taping meets the EIA 481 specification and our carrier tape is "conductive cavity".

Through-hole DMOS

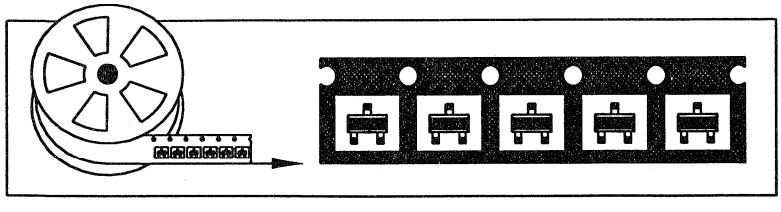
1 Radial tape and reel (TO-92/TO-226)
2 Radial tape and ammo (TO-92/TO-226)
3 Bulk with or without leadform in a box (TO-92/TO-226)
4 Bulk in a tube, 45 pcs. per tube (TO-220)

Surface-mount DMOS

1 Conductive cavity carrier tape on 7" or 13" reels
(SO-8, SuperSOT™-3, SuperSOT™-6, SuperSOT™-8, SOT-23, SOT-223, SOIC-16, TO-263)

Ordering information and Flow code options:

1 Surface-mount packages (SOT-23(TO-236)/SuperSOT™-3)
Part automatically comes 3K per reel - 7" reel. No flow code needed.

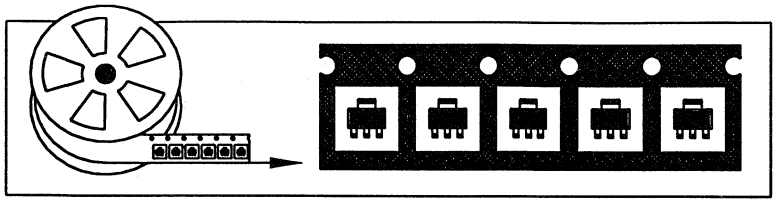


Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
L99Z	3K	7" dia.	8mm wide	Conductive cavity	No marking on device
D87Z	10K	13" dia.	8mm wide	Conductive cavity	
S62Z	3K	bag	none	none	Bulk

Ordering Information (continued)

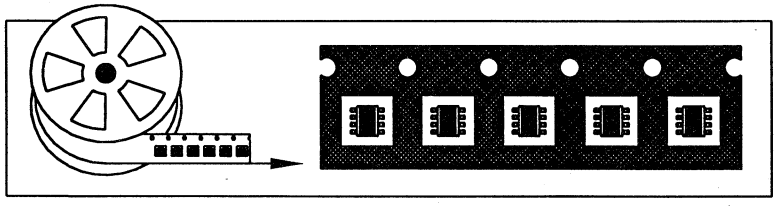
Ordering information and Flow code options:

2 Surface-mount packages (SOT-223(TO-261))
Part automatically comes 2.5K per reel - 13" reel. No flow code needed.



Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
L99Z	2.5K	13" dia.	12mm wide	Conductive cavity	No marking on device
D84Z	500pc	7" dia.	12mm wide	Conductive cavity	
S62Z	2.5K	Bag	None	None	Bulk

3 Surface-mount packages (SO-8/SuperSOT™-8)
Part automatically comes 2.5K per reel - 13" reel. No flow code needed.

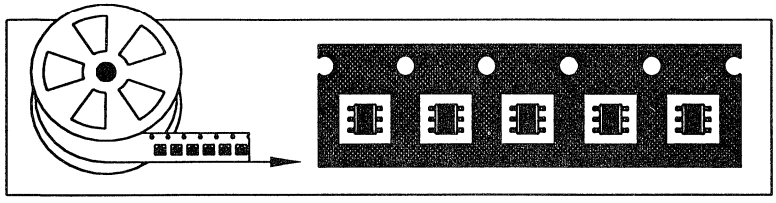


Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
L99Z	2.5K	13" dia.	12mm wide	Conductive cavity	No marking on device
D84Z	500	7" dia.	12mm wide	Conductive cavity	
L86Z	98pc	Rail	Note: for Jfet, qty is 100 pc per rail.		
S62Z	495pc	Bag	None	None	Bulk

Ordering Information (continued)

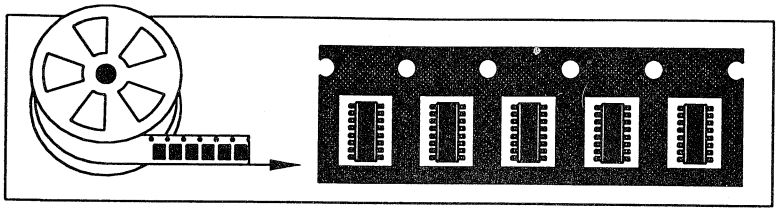
Ordering information and Flow code options:

4 Surface-mount packages (SuperSOT™-6)
Part automatically comes 2.5K per reel - 13" reel. No flow code needed.



Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
L99Z	3K	7" dia.	8mm wide	Conductive cavity	No marking on device
D87Z	10	13" dia.	8mm wide	Conductive cavity	
S62Z	3K	Bag	None	None	Bulk

5 Surface-mount package (SO-16)
Part automatically comes 2.5K per reel - 13" reel. No flow code needed.

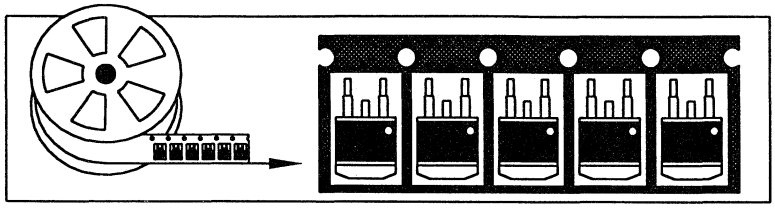


Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
L99Z	2.5K	13" dia.	16mm wide	Conductive cavity	No marking on device
D84Z	500pc	7" dia.	16mm wide	Conductive cavity	
L86Z	100pc	Rail			
S62Z	2.5K	Bag	None	None	Bulk

Ordering Information (continued)

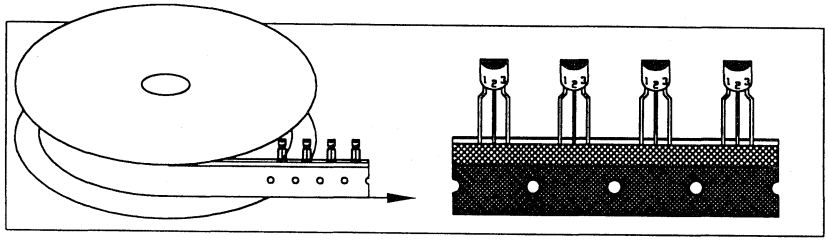
Ordering information and Flow code options:

6 Surface-mount package (TO-263AB)
Part automatically comes 2.5K per reel - 13" reel. No flow code needed.



Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
L99Z	800pc	13" dia.	24mm wide	Conductive cavity	No marking on device
L86Z	Tube/Rail 45pcs per. rail				
S62Z	800pc	Bag	None	None	Bulk

7 TO-92/TO-226
Product **automatically comes in bulk** - 2K per box. No flow code needed.
Radial tape and reel

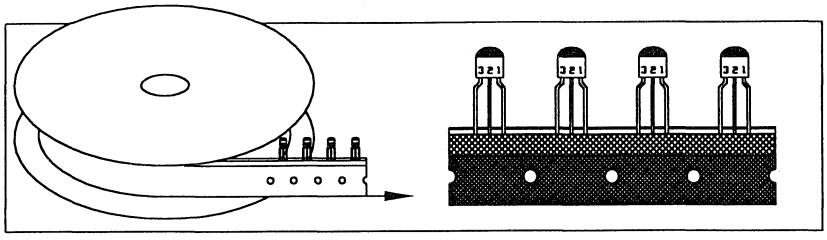


Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
D26Z	2K	13" dia.	18mm wide	Radial	Round side toward adhesive. (Equiv. to RA)

Ordering Information (continued)

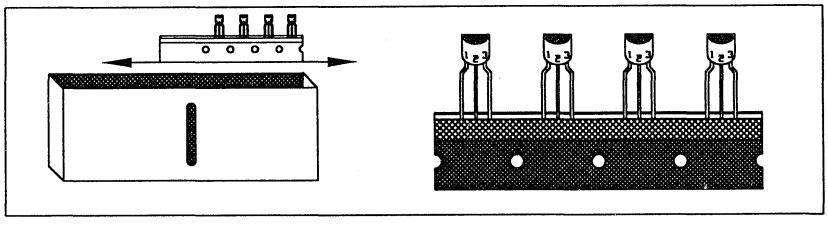
Ordering information and Flow code options:

8 TO-92/TO-226
Product **automatically comes in bulk** - 2K per box. No flow code needed.
Radial tape and reel



Flow code	Qty.	Reel size	Tape size	Tape Style	Notes
D27Z	2K	13" dia.	18mm wide	Radial	Flat side toward adhesive. (Equiv. to RE)

9 TO-92/TO-226
Radial tape and ammo

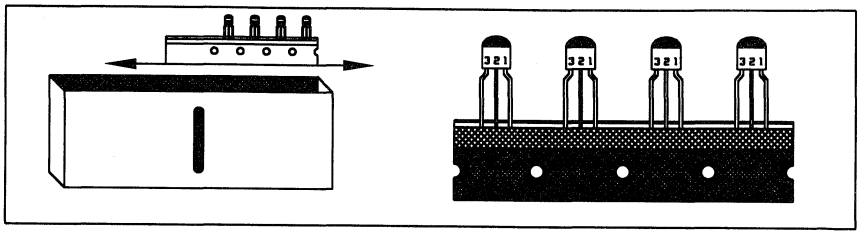


Flow code	Qty.	Box size	Tape size	Tape Style	Notes
D75Z	2K	12 3/4 x 6 x 1 3/4	18mm	Radial	Round side toward adhesive. (Equiv. to RP). Options D26Z, D28Z, D10Z, D11Z can all be pulled from this box. Option dependent on which corner the product is pulled from.

Ordering Information (continued)

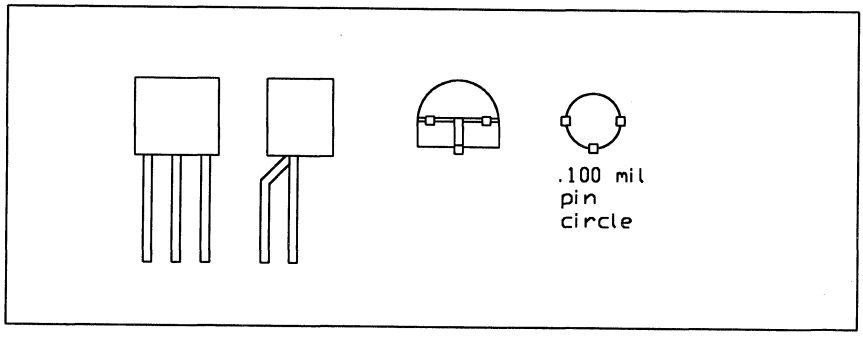
Ordering information and Flow code options:

10 TO-92/TO-226
Radial tape and ammo



Flow code	Qty.	Box size	Tape size	Tape Style	Notes
D74Z	2K	12 3/4 x 6 x 1 3/4	18mm	Radial	Flat side toward adhesive. (Equiv. to RM). Options D27Z, D29Z, D81Z, D89Z can all be pulled from this box. Option dependent on which corner the product is pulled from.

11 Leadforming TO-92/TO-226

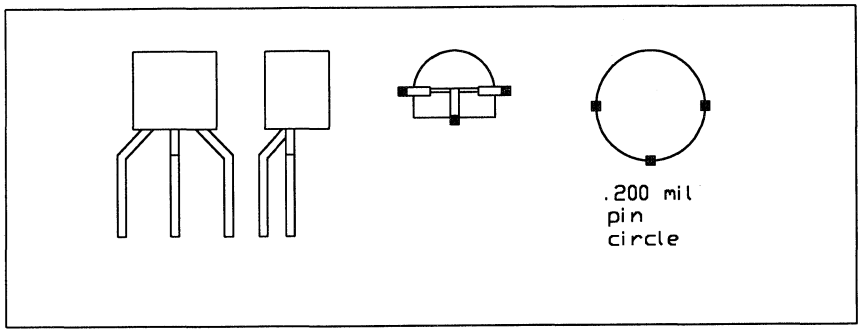


Flow code	Qty.	Notes
J18Z	2K	Center lead toward the flat side to form TO-18 pin circle - .100 mils.

Ordering Information (continued)

Ordering information and Flow code options:

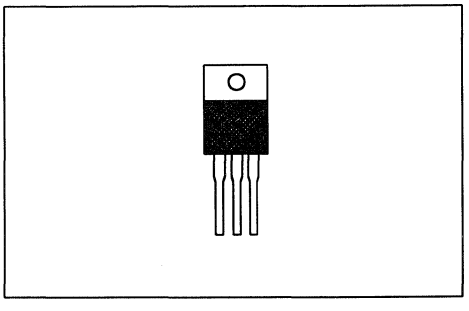
12 Leadforming TO-92/TO-226



Flow code	Qty.	Notes
J05Z	2K	Center lead toward the flat side to form TO-5 pin circle - .200 mils.

13 TO-220

Product comes in bulk - order increments of 45pc.



Flow code	Qty.	Notes
J69Z	45	Center lead toward front to form .200 mil pin circle.

Section 12

Package Outlines and Leadform Options

Package Outlines and Leadform Options

- Dimensions are: inches / [millimeters]
- Numbers in parentheses following package titles are NS internal package codes.
- Dimensions and package codes shown are applicable at time of printing. Factory should be consulted to confirm dimensions, packages codes and other information.

NS Package Code	JEDEC Code	NS Package Code	JEDEC Code
S1	SOIC 8-Lead SMD	37	TO-220
S3	SOIC 16-Lead SMD	45	TO-263AB (D^2Pak)
31	SuperSOT™-6 (Dual)	47	SOT-223 (TO-261)
32	SuperSOT™-3	49	SOT-23 (TO-236AB)
33	SuperSOT™-6 (Single)	92	TO-92 Plastic (TO-226AA)
34	SuperSOT™-8 (Single)	95	TO-226AE (Tall TO-92)
35	SuperSOT™-8 (Dual)		

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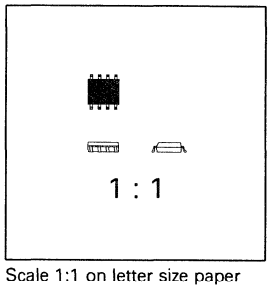
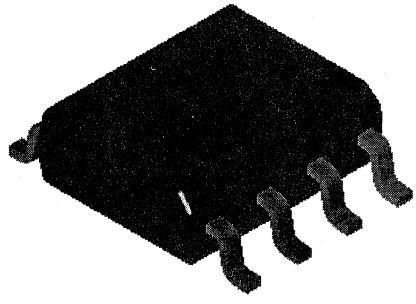
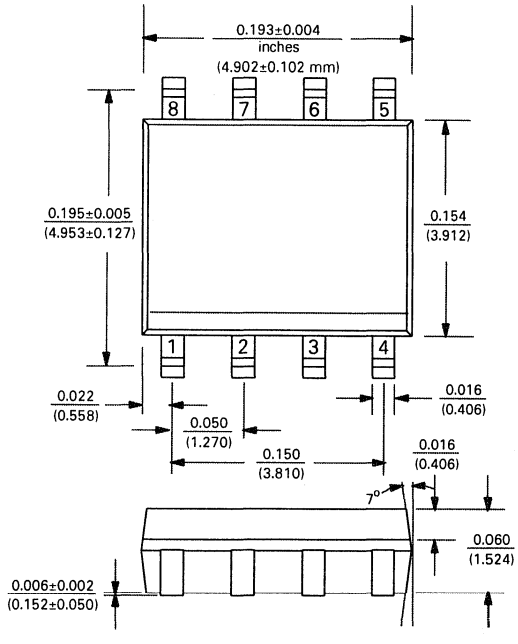
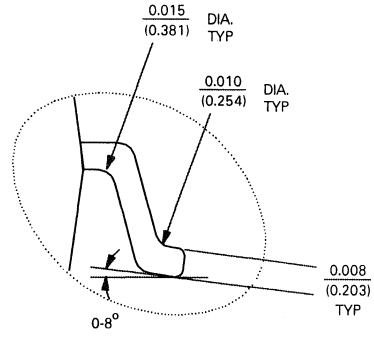
SO-8 (NS PKG Code S1)

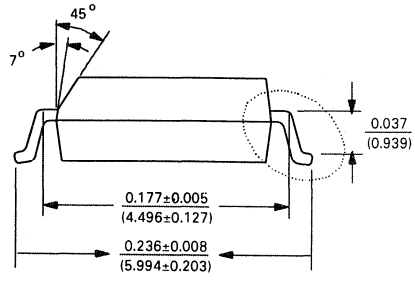


Scale 1:1 on letter size paper









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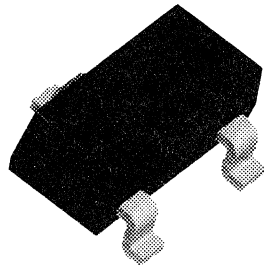
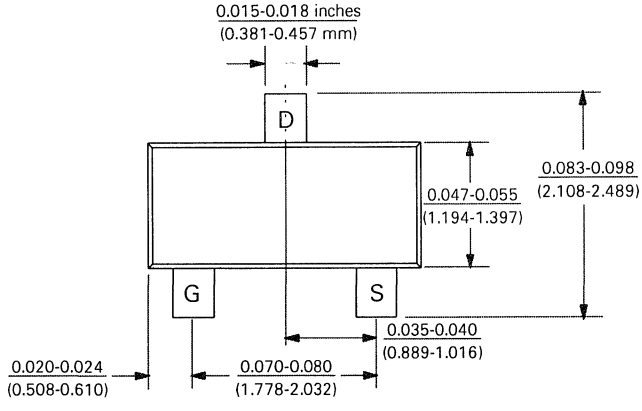
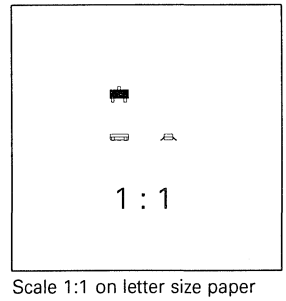
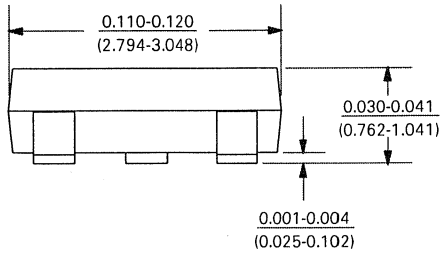
SuperSOT™-3 (NS PKG Code 32) / SOT-23 (NS PKG Code 49)

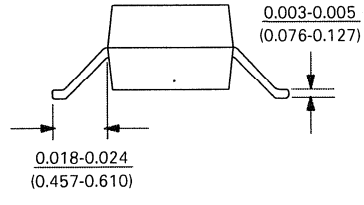






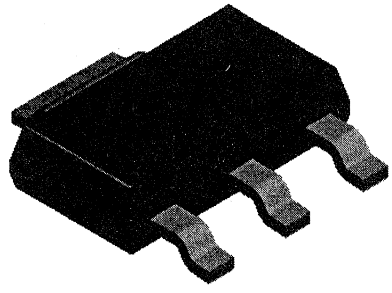
Scale 1:1 on letter size paper

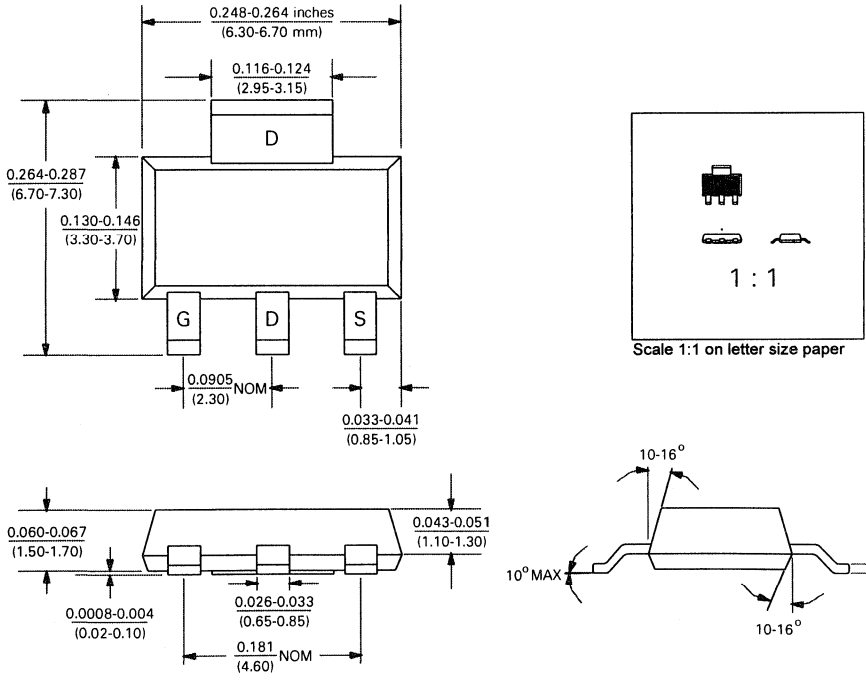




National Semiconductor™

SOT-223 (NS PKG Code 47)





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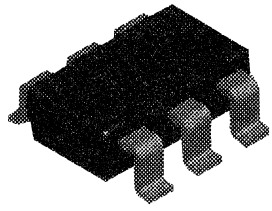
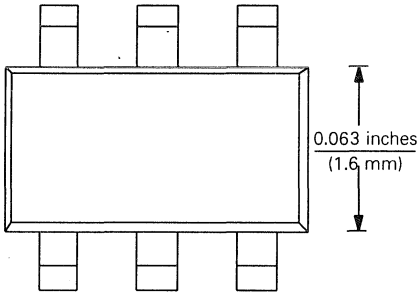
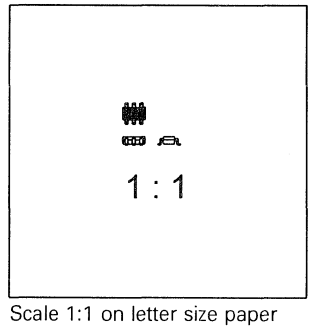
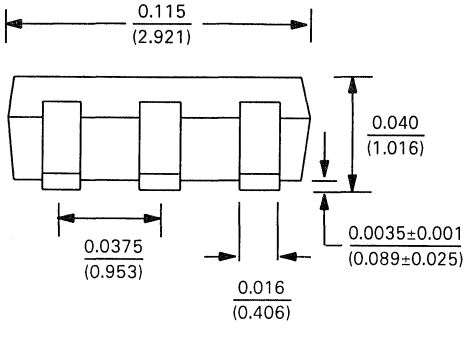
SuperSOT™-6 (NS PKG Code 33)

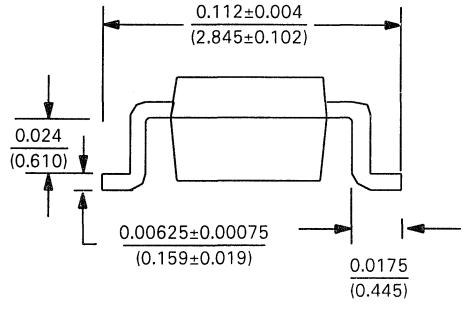






Scale 1:1 on letter size paper





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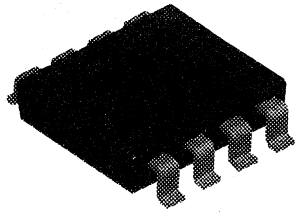
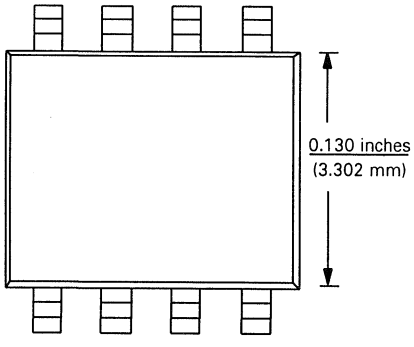
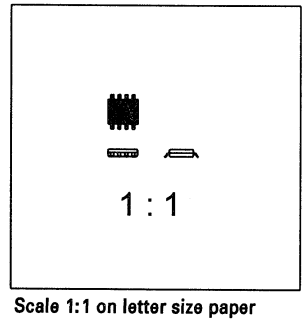
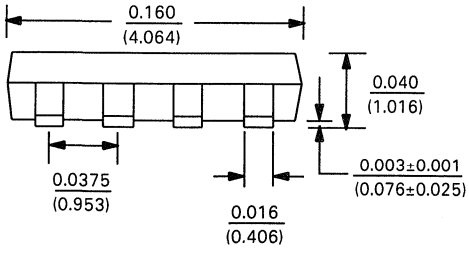
SuperSOT™-8 (NS PKG Code 34)

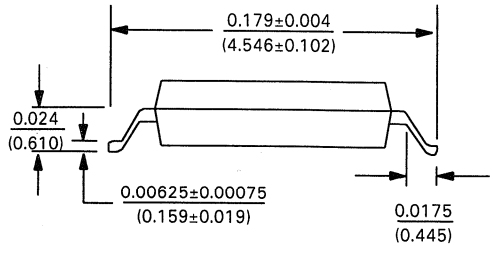






Scale 1:1 on letter size paper





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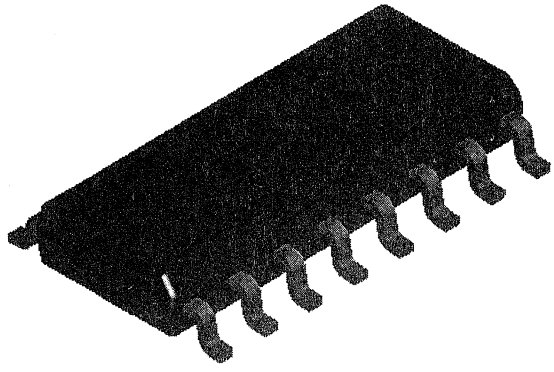
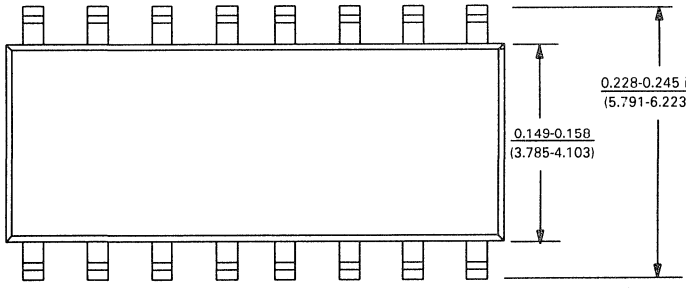
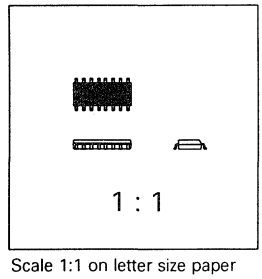
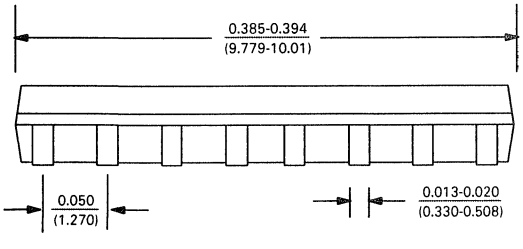
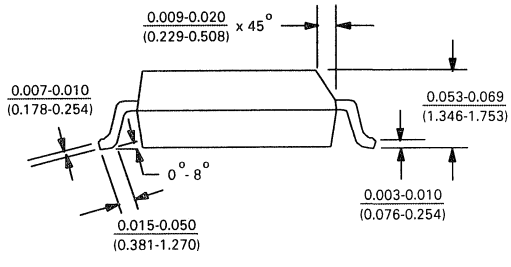






Scale 1:1 on letter size paper





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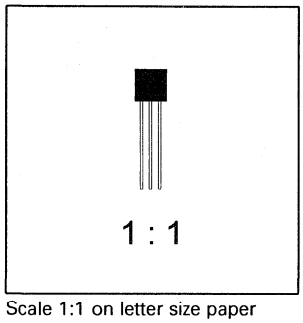
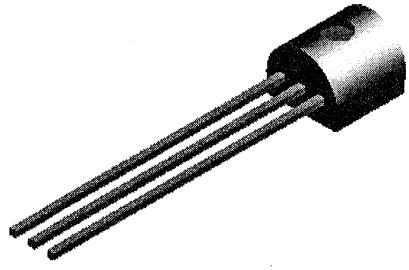
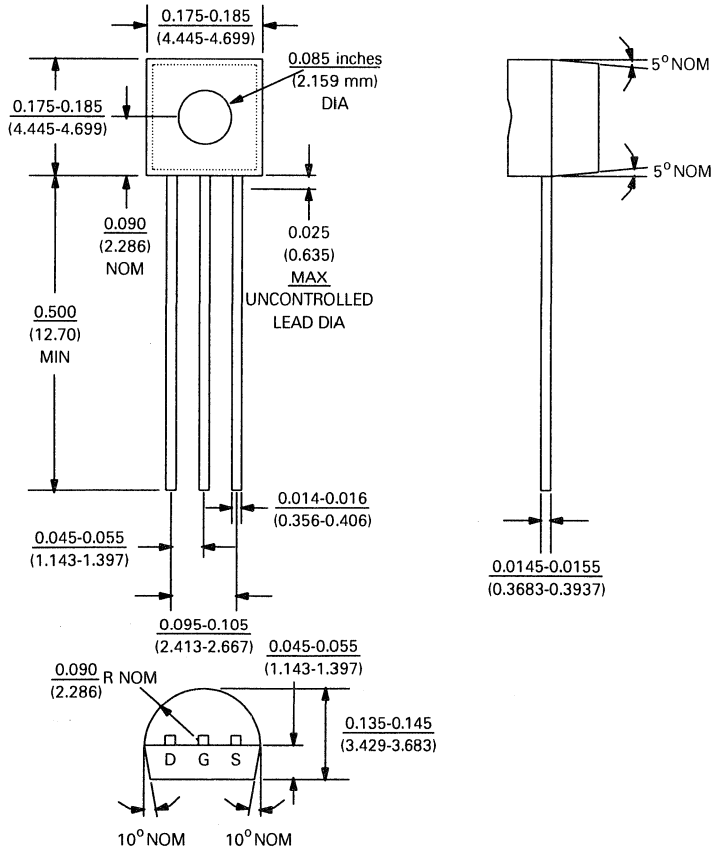


Scale 1:1 on letter size paper





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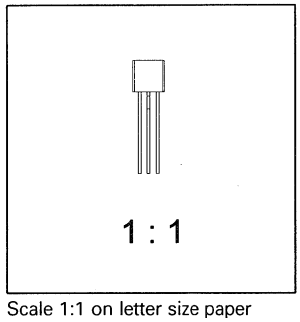
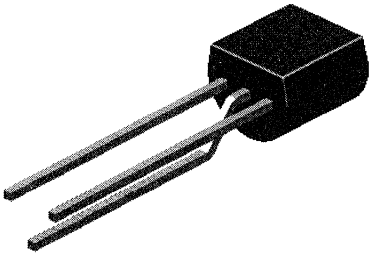
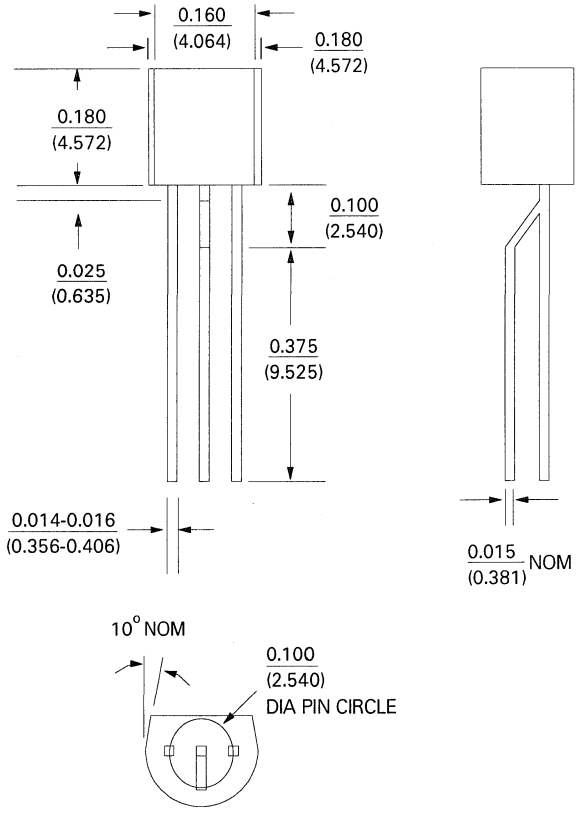
TO-92 (NS PKG Code 97)

-18 Standard lead Form



Scale 1:1 on letter size paper





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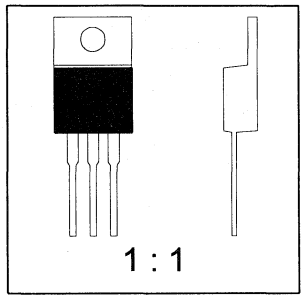
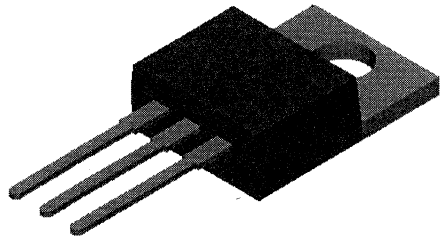
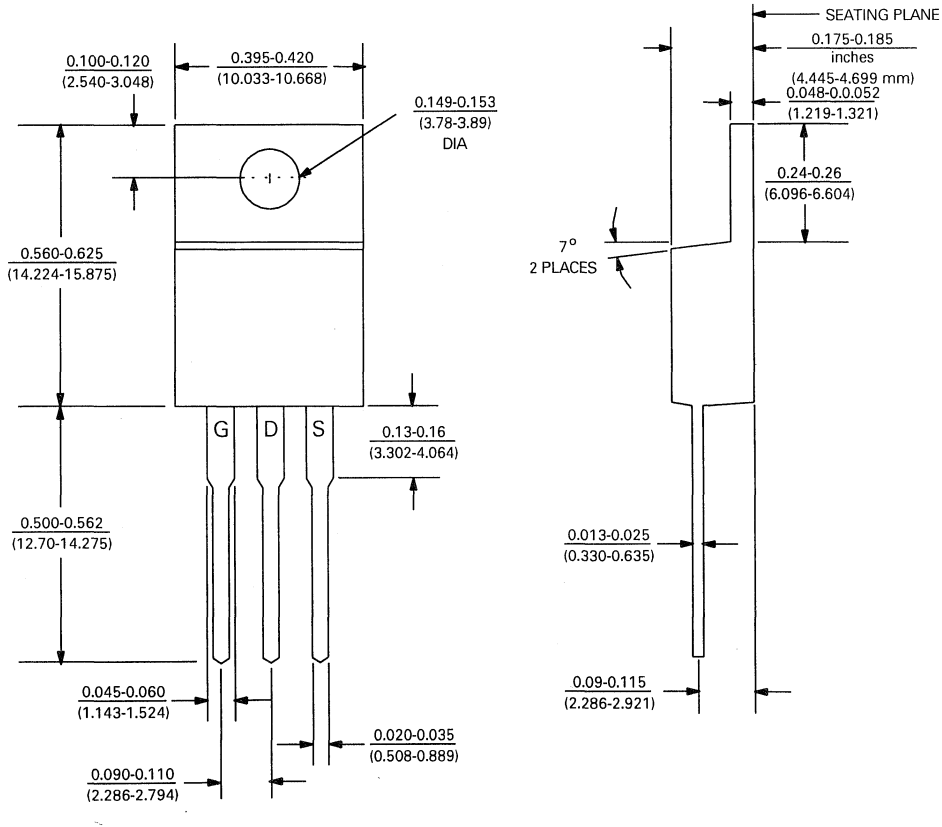
TO-220 (NS PKG Code 37)



Scale 1:1 on letter size paper





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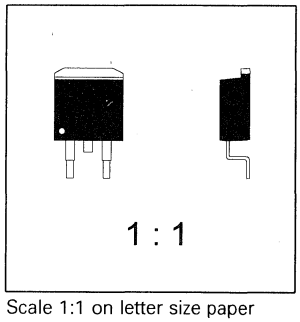
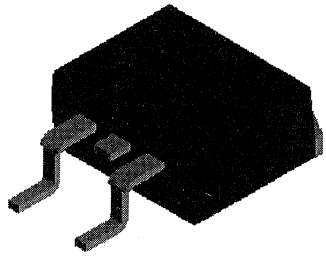
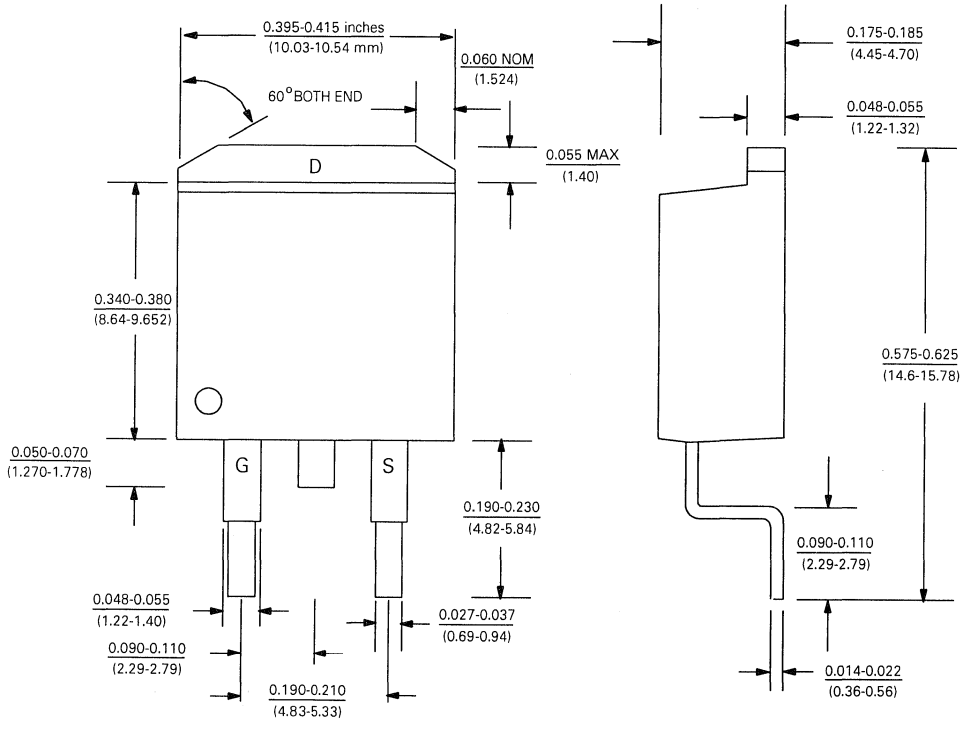


Scale 1:1 on letter size paper





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